

AN3B

Pager

APPLICATIONS HANDBOOK



APPLICATIONS HANDBOOK

Philips
Semiconductors



PHILIPS

Pager Applications Handbook AN3B

This book was prepared by the Application Laboratory of
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QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

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CHAPTER 1

SELECTION GUIDE

Selection guide

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Selection guide

PAGER RECEIVERS

UAA2033T	off-set pager receiver (maintenance only)
UAA2050T	low power digital VHF paging receiver
UAA2080T, H	advanced pager receiver

IC03
IC03

PAGER DECODERS

PCA5000AT	paging decoder
PCF5001T	POCSAG paging decoder

IC03
IC03

DIGITAL DATA FILTER

OM4031	digital post-detection filter for FSK data receivers data sheet; to be integrated in future issue
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IC03

RF MIXERS AMPLIFIERS

SA600	low noise gain stage and mixer 1 GHz.
SA601	low voltage LNA and mixer 1 GHz.
SA620	RF gain stage, VCO and mixer 1 GHz.

IC03
IC17
IC03

RF WIDEBAND TRANSISTORS

BFG505	9 GHz wideband transistor Also for other RF wideband transistors
--------	---

SC14
SC14

MICROCONTROLLERS, GENERAL

80C31	CMOS single-chip 8-bit microcontroller	(ROM-less)	IC20
80C625	idem	(8K x 8 ROM)	IC20
87C625	idem	(8K x 8 EPROM)	IC20

MICROCONTROLLERS, LOW VOLTAGE/LOW POWER

83CL410	CMOS single-chip 8-bit μ C with IIC	(4K x 8 ROM)	IC20
83CL781	idem	(16K x 8 ROM)	IC20
83CL782	idem, 12 MHz at 3.1 V	(16K x 8 ROM)	IC20
PCF84C430	single-chip 8-bit microcontroller with LCD driver		IC14

Selection guide

LOW VOLTAGE, LOW POWER IIC LCD DISPLAY DRIVERS

DATA HANDBOOK

PCF2116	1-4 lines, up to 24 char./line; MUX	1 : 16 - 1 : 32	IC12
PCF8566	96-segment LCD driver; MUX	1 : 1 - 1 : 4	IC12
PCF8568	16-lines row driver; MUX	1 : 8 - 1 : 32	IC02
PCF8569	40-lines column driver; MUX	1 : 8 - 1 : 16	IC02
PCF8576	160-segment-LCD driver; MUX	1 : 1 - 1 : 4	IC12
PCF8577	64-segment LCD driver; MUX	1 : 1 - 1 : 2	IC12
PCF8578	row/column LCD dot matrix driver;	1 : 8 - 1 : 32	IC12
PCF8579	4-lines column driver; MUX	1 : 8 - 1 : 32	IC02

LOW VOLTAGE, LOW POWER STATIC RAMS

PCD5101	256 x 4 bit	IC10
PCD5114	1024 x 4 bit	IC10
PCF8570	256 x 8 bit, IIC-bus	IC12
PCF8571	128 x 8 bit, IIC-bus	IC12
PCF8581/C	128 x 8 bit, EEPROM, IIC-bus	IC10
PCF8582	256 x 8 bit, EEPROM, IIC-bus	IC10
PCF8583	256 x 8 bits IIC-bus, clock calender	IC12

HIGH-SPEED CMOS LOGIC

74HCTXXX	high speed CMOS logic family	IC06
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SMALL SIGNAL TRANSISTORS

BC546/556/557	general purpose, small signal transistors Also for other general purpose transistors	SC04 SC01
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SMALL SIGNAL DIODES

1N4148	high speed switching diode	SC01
BAT85	Schottky barrier switching diode (very low Vf) Also for other small signal diodes	SC01 SC01

QUARTZ CRYSTALS

General information and selection guide on quartz crystals	PA07
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Selection guide

PASSIVE COMPONENTS

DATA HANDBOOK

General information on resistors and capacitors, fixed and variable, standard and SMD; book series

PAxx

BATTERIES

General information on batteries: Business Group on Batteries, Lighting Division.

CHAPTER 2

GENERAL

General

page

II-1

General

QUALITY

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

quality assurance

based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates

partnerships with customers

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes

partnerships with suppliers

ship-to-stock, statistical process control and ISO 9000 audits

quality improvement programme

continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- incoming material management through partnerships with suppliers
- in-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

- A germanium or other material with a band gap of 0.6 to 1 eV
- B silicon or other material with a band gap of 1 to 1.3 eV
- C gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more
- R compound materials, e.g. cadmium sulphide.

General

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements. In the following list low power types are defined by $R_{th\ j-mb} > 15\text{ K/W}$ and power types by $R_{th\ j-mb} \leq 15\text{ K/W}$.

- A diode; signal, low power
- B diode; variable capacitance
- C transistor; low power, audio frequency
- D transistor; power, audio frequency
- E diode; tunnel
- F transistor; low power, high frequency
- G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under '*Serial number*'
- H diode; magnetic sensitive
- L transistor; power, high frequency
- N photocoupler
- P radiation detector; e.g. high sensitivity photo-transistor; with special third letter
- Q radiation generator; e.g. LED, laser; with special third letter
- R control or switching device; e.g. thyristor, low power; with special third letter
- S transistor; low power, switching
- T control and switching device; e.g. thyristor, power; with special third letter
- U transistor; power, switching
- W surface acoustic wave device
- X diode; multiplier, e.g. varactor, step recovery
- Y diode; rectifying, booster
- Z diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for

industrial or professional equipment.⁽¹⁾ The letter has no fixed meaning, except in the following cases:

- A for triacs, after second letter 'R' or 'T'
- F for emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.
- L for lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.
- O for opto-triacs, after second letter 'R'
- T for 3-state bicolour LEDs, after second letter 'Q'
- W for transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

- AA112: germanium, low power signal diode (consumer type)
- ACY32: germanium, low power AF transistor (industrial type)
- BD232: silicon, power AF transistor (consumer type)
- CQY17: GaAs, light-emitting diode (industrial type)
- RPY84: CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

⁽¹⁾ When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

General

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

- A 1%
- B 2%
- C 5%
- D 10%
- E 20%

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R . The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or -39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM} , or the rated repetitive peak off-state voltage, V_{DRM} , whichever is the lower. Reversed polarity

with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.⁽¹⁾

Solitary circuits

The first letter divides solitary circuits into:

- S solitary digital circuits
- T analog circuits

⁽¹⁾ A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

General

U mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.⁽¹⁾

Microprocessors

The first two letters identify microprocessors and related circuits:

- MA microcomputer or central processing unit
- MB slice processor (functional slice of microprocessor)
- MD related memories
- ME other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

- NH hybrid circuits
- NL logic circuits
- NM memories
- NS analog signal processing using switched capacitors
- NT analog signal processing using charge-transfer devices
- NX imaging devices
- NY other related circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range:

- A temperature range not specified below
- B 0 to + 70 °C
- C -55 to +125 °C
- D -25 to + 70 °C
- E -25 to + 85 °C
- F -40 to + 85 °C
- G -55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same

basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

- C cylindrical
- D ceramic dual in-line (CERDIL, Cerdip)
- F flat pack (two leads)
- G flat pack (four leads)
- H quad flat pack (QFP)
- L chip on tape (foil)
- P plastic dual in-line (DIL)
- Q quad in-line (QUIL)
- T mini pack (SOL, SO, VSO)
- U uncased chip

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

- C cylindrical
- D dual in-line (DIL)
- E power DIL (with external heatsink)
- F flat pack (leads on two sides)
- G flat pack (leads on four sides)
- H quad flat pack (QFP)

⁽¹⁾ The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

General

K diamond (TO-3 family)
M multiple in-line (except dual, triple and quad)
Q quad in-line (QUIL)
R power QUIL (with external heatsink)
S single in-line (SIL)
T triple in-line
W leaded chip carrier (LCC)
X leadless chip carrier (LLCC)
Y pin grid array (PGA)

SECOND LETTER (MATERIAL)

C metal-ceramic
G glass-ceramic
M metal
P plastic

Examples

PCF1105WP: digital IC; PC family; operating temperature range -40 to $+85$ °C; serial number 1105; plastic leaded chip carrier.

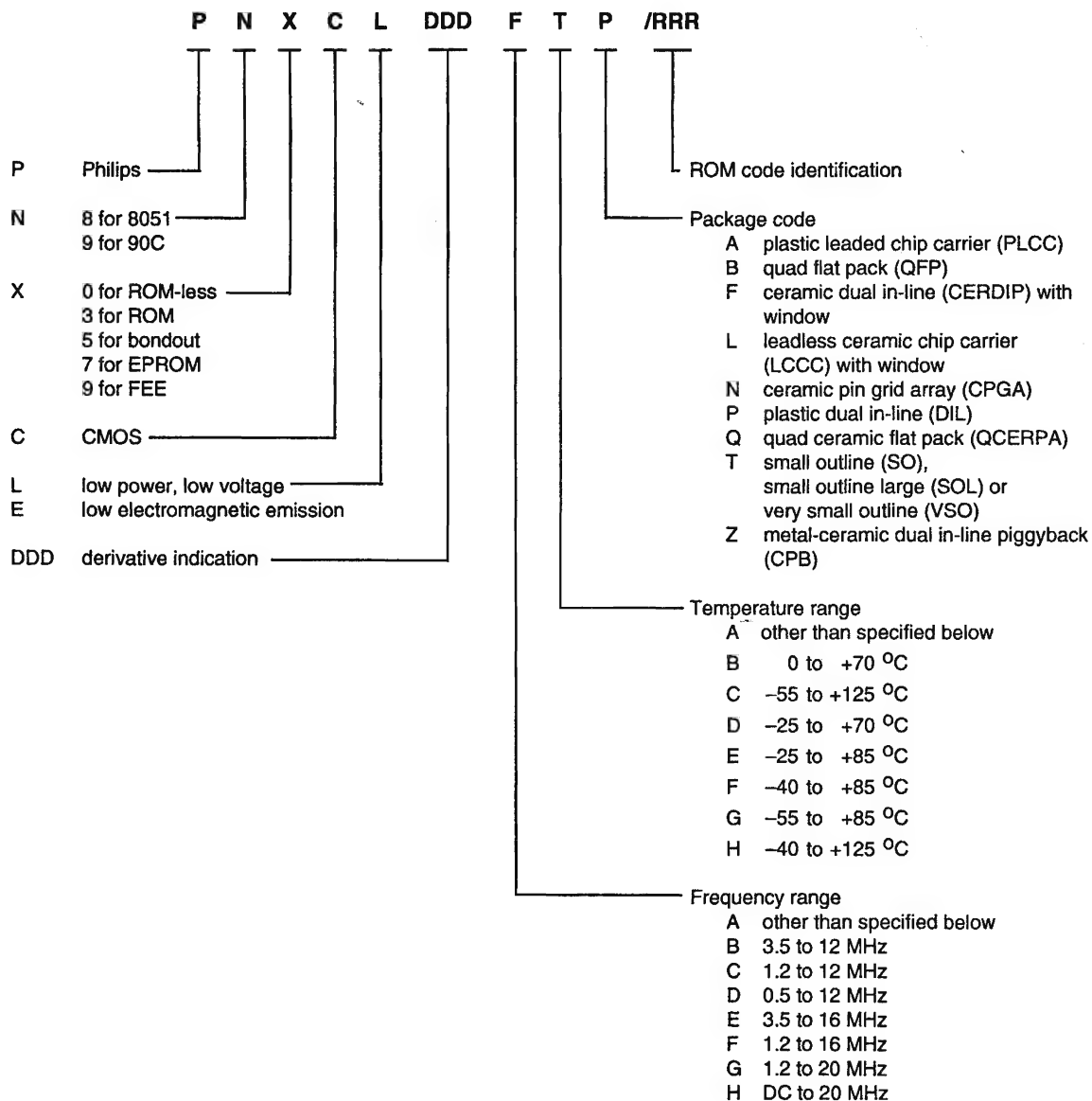
GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to $+70$ °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range -55 to $+125$ °C; serial number 2000.

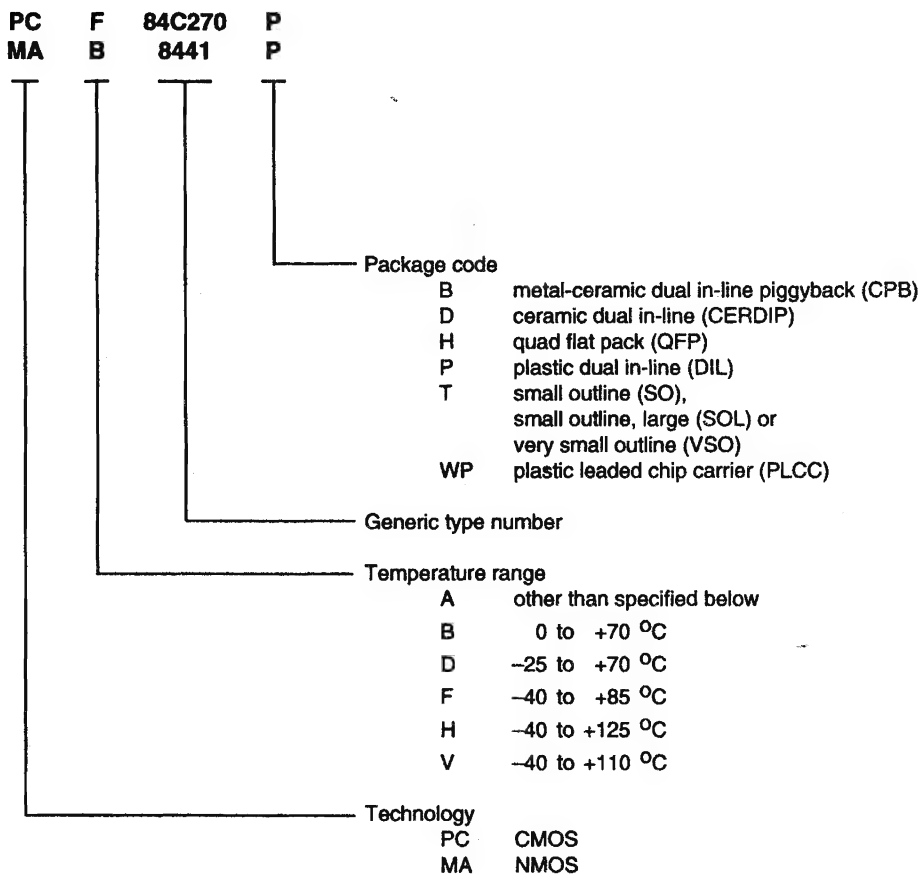
General

TYPE NUMBERING of 8051 and 90C MICROCONTROLLER DERIVATIVES



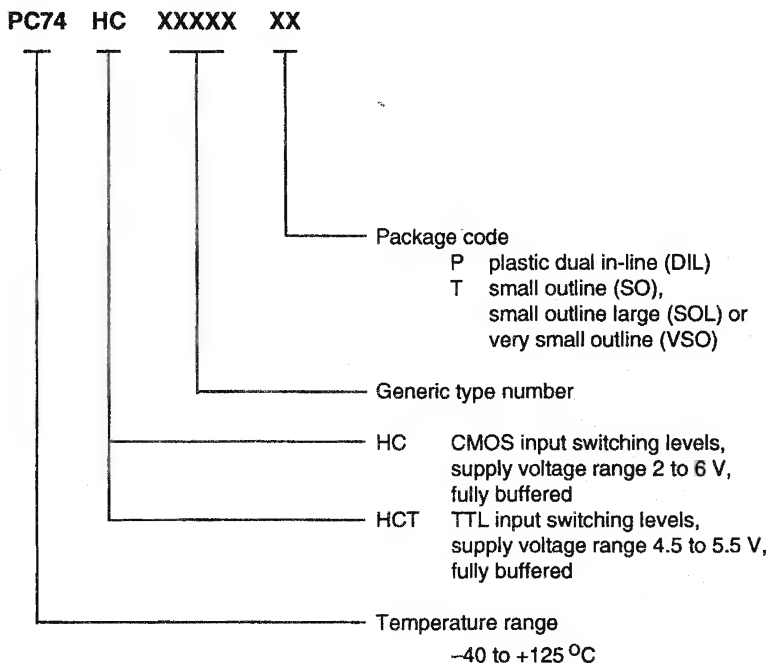
General

TYPE NUMBERING of 8048 MICROCONTROLLER DERIVATIVES



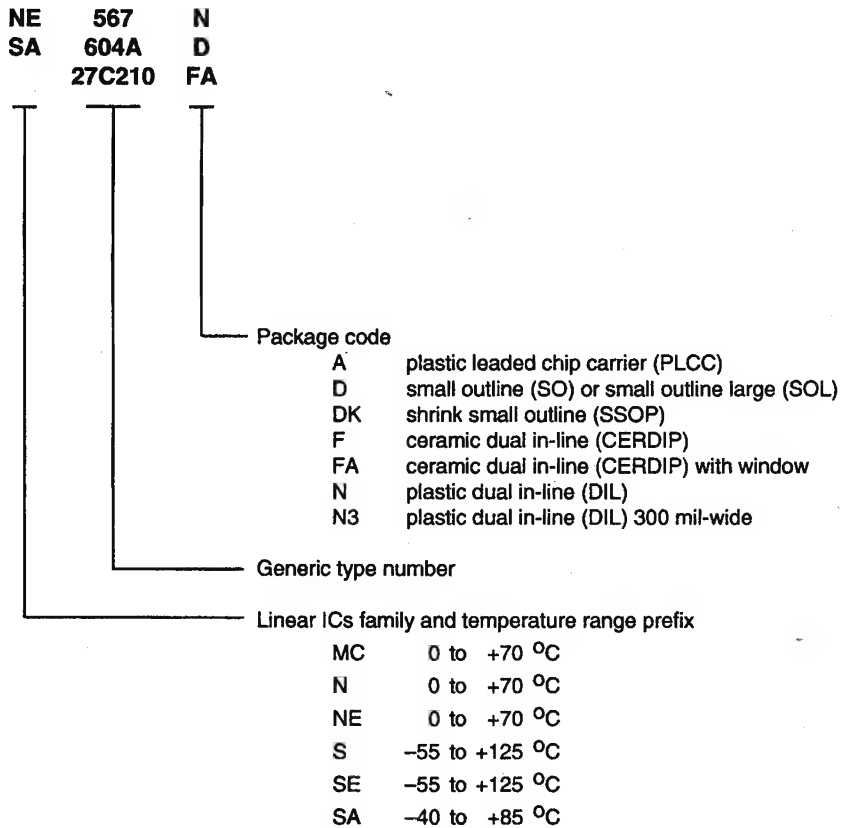
General

TYPE NUMBERING of HCMOS INTEGRATED CIRCUITS



General

TYPE NUMBERING of SIGNETICS LINEAR AND MEMORY DEVICES



General

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage

General

variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 k Ω per cm². The floor should also be covered with antistatic material. The following precautions should be observed:

- persons at a work bench should be earthed via a wrist strap and a resistor
- all mains-powered electrical equipment should be connected via an earth leakage switch
- equipment cases should be earthed
- relative humidity should be maintained between 50 and 65%
- an ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

Assembly

MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

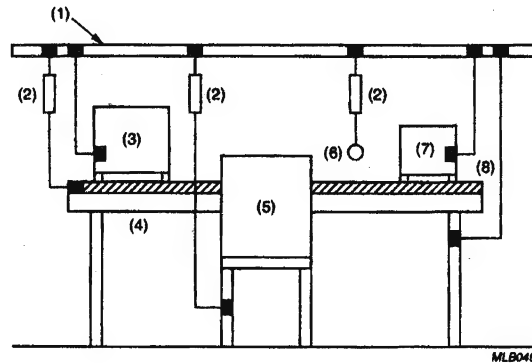
During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.

General



- (1) Earthing rail.
- (2) Resistor ($500\text{ k}\Omega \pm 10\%$, 0.5 W).
- (3) Ionizer.
- (4) Work bench.
- (5) Chair.
- (6) Wrist strap.
- (7) Electrical equipment.
- (8) Conductive surface/antistatic sheet.

Fig.1 Protected work station.

CHAPTER 3

INTRODUCTION TO PAGER SYSTEMS

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Introduction to pager systems

General pager information

Introduction

A pager is a widely known, fast growing way of receiving personal information, that is finding its way into many applications.

Pager systems are particularly interesting, because they are relatively cheap (low cost device, low power usage), they are small (as a system, easy to build-in), economic from a network point of view (small bandwidth, many users per channel, low cost of operation) and very user friendly (less intrusive than (cordless) telephones, fast installation, simple infra-structure).

Simple alert-only pagers may consist of only two integrated circuits while more sophisticated display pagers are not much bigger.

Because of these characteristics, the pager market is expanding rapidly. According to Mobile Radio Technology of February 1994:

- more than 50% of new pager customers are personal users,
- of total pager sales, 15% is by retail trade, to increase to 35% in the next two years,
- relatively high information rate; 26% of users receive 2 messages per day, 35% receive 3 - 5 messages and 17% receive more than 11 messages per day,
- Pager market will grow to US\$ 620.1 million by 1997.

Pager systems come in many varieties, mostly chosen for their simplicity and ease of operation; a few application examples may be mentioned:

- Personal communication (person to person); clip-on pager, in watches, as jewellery, in key-rings, in cordless (telepoint) and cellular phones.
- Personal information systems (system to person); in PC's, notebooks, palm-tops, personal organisers, smart-cards, information tags.
- Remote control applications (person to system); in gasoline pumps, remote metering, supermarket displays, cargo tags, cattle tracking, (second-)house control systems.

Pager networks are run by many different network operators, using a variety of protocols. Some protocols

have limited recognition outside their operational region, others have a higher penetration.

Philips is supporting the well known POCSAG protocol (Post Office Code Standardisation Advisory Group), also known as Radio Paging Code # 1 or RPC 1. This code is well established, being used on a worldwide scale with a high market share.

Successor systems are under discussion, either being designed or in operation in various parts of the world. These successor systems are designed using dedicated circuitry, or are based on system-elements from the current pager IC-line.

Remote metering

Remote utility-meter reading facility for water, gas, electricity etc. The system consists of an interrogation receiver/transmitter system, connected to the (private) utility meter. The system will respond to a passing interrogation vehicle with the current status and meter content. The system will also be capable of remote changing of tariffs. The advantages of POCSAG-based system for this remote measuring and control system are its low cost, the established receiver technology, the high number of addresses per channel, the possibility of having one (hardware) system with many, programmable, user addresses, suitable for on-line tariff switching. An other advantage is that no elaborate antennas are required.

Flight information pager

User to call (toll-free) telephone number to request flight date for any departure and destination city (in US). The best available flight, connections and fares are automatically identified by the system and the data is formatted for an alpha-numeric pager and distributed to the customer's paging service.

Five outbound and return flights and a matrix of fare options are then transmitted to the pager. The flight information may also be received on a PC, using an integrated pager receiver.

Introduction to pager systems

General pager information

Airport personal tracking and information system

An intelligent information system keeps the bearer informed on the latest information of his flight in and around the airport.

By means of an automatic interrogation system, the system also keeps track of the bearer's location; this enables the airport to selectively send (electronic-, public address-)information to the bearer only transmitting the information at the location of the bearer (position tracking). The system is to be the natural successor to the "boarding-pass" procedures.

Missing persons locator

A pager system is attached to a person to be secured. If this person is missing (sailors lost in a storm, skiers missing in the mountains etc), a special code (POCSAG?) is being send. The system will respond by activating a beacon(transmission) to home-in on.

Cattle "remote control" system

An automatic cattle herding system is based on radio-pagers for controlling the movements of grazing cattle. Specially trained cows will stop grazing and return to the feed trough on sound information from a neck-worn pager system. Training of the cattle is done over a one week period. The cattle can be addressed by dialling a group broadcast paging number by means of a standard (wireless) telephone.

Introduction to pager systems

Pager system aspects

1. System Overview

In general, a paging system consists of a base station and several paging receivers, which listen to the information transmitted by the base station. Although other ways of communication exist, only radio frequency (RF) transmission between base station and pager will be considered. The range covered by the transmitter may vary from a few 100 m for on-site applications to some 10 km in off-site paging systems. A cellular structure with more than one base station can be used to cover larger areas or even a whole country.

In order to issue a paging call to a subscriber, the required paging information has to be forwarded to the base station (BS). This can be done by telephone system or other network to which the BS is connected. In the base station the paging information is converted into the appropriate transmission code format, in this case the CCIR Radiopaging Code No.1 (POCSAG Code). The POCSAG Code format is presented in section 2. The RF carrier of the BS is modulated with the POCSAG coded information bits of each call.

Within this report, a frequency shift keying (FSK) modulation with a non- return-to-zero (NRZ) code and a frequency shift of ± 4.5 kHz is assumed. This type of modulation is normally associated with paging applications and the POCSAG Code. The bit rate of the information transfer can be either 512 or 1200 bit/s.

The RF section of the paging receiver processes the signals that come from the base station to convert them back to POCSAG Code format. This normally requires RF filtering, mixing, IF filtering, demodulation and output waveform generation. The output data stream, which is now in the transmission code format again, is passed to the decoder section of the paging receiver. The RF section may have a power down mode, which is controlled by the decoder.

The decoder section scans the incoming data stream. When a match is found between the receiver identification code (RIC) to the decoder and the address of a call transmitted by the base station, the decoder will signal "valid paging call received" to the man-machine interface (MMI). The information attached to a specific call is also passed to the MMI. Upon call reception, the

man-machine interface will generate some alert cadences and display the message information when instructed. The complexity of the MMI depends on the type of pager.

In alert-only (beep-only) pagers the MMI simply comprises an alerter and a few switches, the control logic will be a part of the decoder itself.

In display pagers the MMI is far more complex, the decoder becomes more or less a preprocessor to the man-machine interface. In this case the MMI is usually a display unit with its own microcontroller, which performs data processing on the call information passed by the decoder and display control functions.

2. Transmission Code Format

This section describes the CCIR Radiopaging Code No.1, which is also known as the POCSAG Code, see fig. 1-1.

- General transmission format, see fig.1-1a

A transmission according to the rules of the POCSAG Code consists of a preamble followed by batches of codewords, see fig. 1-1a. The transmission is stopped after the last batch, when there are no further calls to transmit.

The preamble is transmitted to allow the pagers to achieve bit synchronization and to prepare them to acquire word synchronization. The preamble is a pattern of bit reversals, 10101010..., repeated for at least 576 bits.

- Batch format, see fig.1-1b

Information is transmitted in the form of batches consisting of codewords of 32 bits length, which are transmitted MSB first. A batch comprises a synchronization codeword (SC) followed by 8 frames (FR0-FR7), each containing 2 codewords, see fig. 1-1b. Each pager is allocated to one of the 8 frames according to the 3 least significant bits of its receiver identification code (RIC). Only address codewords transmitted in the allocated frame are examined by the pager.

Introduction to pager systems

Pager system aspects

- Synchronization codeword, see fig.1-1c

The synchronization codeword has a fixed 32-bit pattern which is shown in fig. 1-1c. It consists of a pseudo-random sequence which has a very low correlation with the preamble. It is used to achieve batch synchronization.

Within a frame 3 different kinds of codewords may occur: address, message and idle codewords. A flag bit distinguishes address and idle codewords (MSB=0) from message codewords (MSB=1). Each codeword contains 20 bits of information. A further 10 CRC bits produced by a (31,21) BCH coding scheme and a parity bit are added to protect a call against transmission errors and to increase the call success rate by error correction.

- Address Codewords, see fig. 1-1d

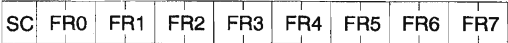
The address codeword is used to select a specific pager and to issue alert- only (beep-only) calls or message calls in conjunction with message codewords. Bit 1 (MSB) of an address codeword is always a "0". This distinguishes it from a message codeword. Bits 2-19 are the 18 most significant bits of the pager's identification code (RIC). The remaining 3 bits are coded in the number of the frame, in which the address codeword is transmitted. Two function bits (FC, bits 20-21) are used to classify calls as being either tone-only (beep-only), numeric or alphanumeric type.

- Message Codewords, see fig. 1-1e

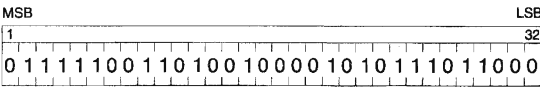
A message codeword always starts with a "1". The information to be transferred is put into the 20 message bits (bits 2-21) of subsequent message codewords. The whole message follows directly after the address codeword, effectively replacing the normal frame structure. Any address or idle codewords scheduled for transmission are postponed until the first appropriate frame after completion of the message. Longer messages may continue in subsequent batches, but the batch structure is maintained: a synchronization code-word precedes each group of 16 codewords.



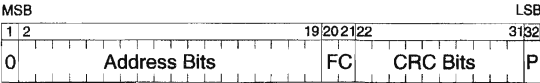
a) Transmission Format



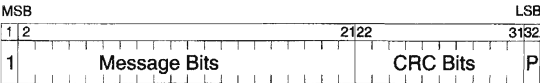
b) Batch Format



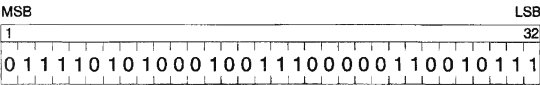
c) Synchronization Codeword (SC)



d) Address Codeword



e) Message Codeword



f) Idle Codeword

Fig. 1-1 POCsAG Coding Structure

- Idle Codewords, see fig. 1-1f

Idle codewords are used to fill unused codeword positions within a batch or to separate messages. The idle codeword is a valid address codeword outside the normal address range allowed for allocation to pagers. It has a fixed 32 bit pattern.

Introduction to pager systems

Pager system aspects

- The POCSAG character sets

Although in principle any message format may be used, two standard formats are used: a 4-bit numeric and a 7-bit alphanumeric format. The numeric format is based on BCD coding and is shown in fig. 1-2. The alphanumeric format consists of the standard 7-bits ASCII code (also known as CCITT Alphabet No 5) and is shown in fig. 1-3.

4-bit Combination	Displayed Character
Bit No: 4 3 2 1	
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	spare code
1 0 1 1	U(rgent)
1 1 0 0	Space (' ')
1 1 0 1	Hyphen ('-')
1 1 1 0]
1 1 1 1	[

Fig. 1-2 POCSAG Numeric Character Set

Messages are partitioned into contiguous blocks of 20 bits, retaining the character reading order. Bits of a character are transmitted LSB first and any unused part of the last codeword is filled with 'space' characters for numeric messages or non-printing characters (e.g. 'EM', 'EOT', 'NULL') for alphanumeric messages. Only the NULL character may be incomplete.

		0		0		0		0		1		1		1		1	
		0		0		1		1		0		0		1		1	
		0		1		0		1		0		1		0		1	
b ₇	b ₆	b ₅	b ₄	b ₃	b ₂	b ₁	b ₀	q	z	3	4	s	e	7			
0	0	0	0	0	1	2		NUL	DLE	SP	0	P			p		
0	0	0	0	1	1			SOH	DC1		1	A	Q	a	q		
0	0	1	0	0	2			STX	DC2	*	2	B	R	b	r		
0	0	1	1	1	3			ETX	DC3	#	3	C	S	c	s		
0	1	0	0	0	4			EOT	DC4	\$	4	D	T	t			
0	1	0	0	1	5			ENQ	NAK	%	5	E	U	u			
0	1	1	0	0	6			ACK	SYN	&	6	F	V	v			
0	1	1	1	1	7			BEL	ETB		7	G	W	w			
1	0	0	0	0	8			BS	CAN	(8	H	X	x			
1	0	0	0	1	9			HT	EM)	9	I	Y	y			
1	0	1	0	0	10			LF	SUB	*		J	Z	z			
1	0	1	0	1	11			VT	ESC			K	[k			
1	1	1	0	0	12			FF	FS		<	L	\	l			
1	1	1	0	1	13			CR	GS	-	=	M]	m			
1	1	1	1	0	14			SO	RS	>	>	N	^	n			
1	1	1	1	1	15			SI	US	/	?	O	_	o			DEL

Introduction to pager systems

Battery technology

Stored electricity

Man's quest for material well-being over the centuries has been tied largely to the harnessing of various forms of energy. And, from early days when man learned to use fire for heat and light, fuels have played a vital role in improving man's position.

Fuels are, in fact, all kinds of materials that are burned in order to release energy in the form of heat. The heat is generated by the reaction of the fuel with oxygen. Typical fuels are coal, firewood, oil and gas. Even the food we eat is a form of fuel.

However, burning fuel is not the only way to produce energy. The chemical reaction that occurs between different substances is another. Dramatic examples are those of fireworks and various forms of explosives.

Energy from batteries is yet another method. We all know batteries, we grew up with them. In torches and toys then later in portable radios and calculators, in photo flash units and movie cameras. After all, batteries have been around a long time - a clay battery utilizing copper and iron electrodes was used around 2000 years ago in the Bagdad area. In more modern times, the principle was rediscovered by Galvani in 1780.

Batteries for portable devices such as the electric torch have been known for many years. More recently, other types of batteries have become popular for use in electrical apparatus like pocket calculators and hearing aids. New types of industrial and household equipment are constantly being introduced and nowadays there is a great variety of different types of battery available.

Batteries provide us with portable, electrical energy. The battery industry has become much more sophisticated of late and the number of appliances originally designed for battery-powered use has steadily increased.

But it is not only toys, radios, clocks and the like that depend on batteries for power. A large number of other equipments and services depend on the electricity delivered from batteries. Electric vehicles, transmission relay stations and communication equipment to name just a few.

Technically speaking, a battery is combination of cells. Each cell is delivering its part to the total energy (voltage) of the battery. Commonly though, the words battery and cell are used interchangeably and we will use these words in the same way.

A battery converts chemical energy into electrical energy. It is theoretically possible to construct batteries from a virtually infinite variety of materials. However, in practice there are only a few 'fuels' and 'oxygen's that provide practical solutions bearing in mind efficiency and cost. In batteries 'fuels' and 'oxygen's are called 'electrodes'. The cell of each battery has one 'fuel' and one 'oxygen' electrode.

Just as the combination of a fuel with oxygen requires certain ambient conditions for a successful reaction, so does the battery. In this case, the electrodes need to be in a special salt solution called the electrolyte. To prevent direct contact between the two electrodes, and thus a short-circuit, an additional separator is usually placed between the electrodes. Although the separator isolates one electrode from another, it does not prevent reaction between the fuel and oxygen.

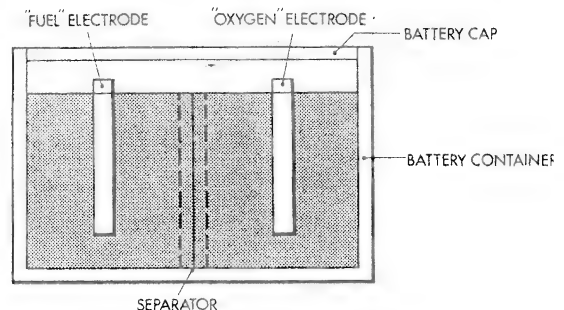


Fig 1 The principle of a battery

Some examples of different pairs of materials used for electrodes are:

- zinc and manganese dioxide
- zinc and mercury oxide
- lithium and manganese dioxide
- lead and lead peroxide
- cadmium and nickel oxide.

Introduction to pager systems

Battery technology

There are many types of battery produced these days. Table 1 gives a survey of those different battery systems that are of prime importance to our everyday life. They are arranged according to their volume.

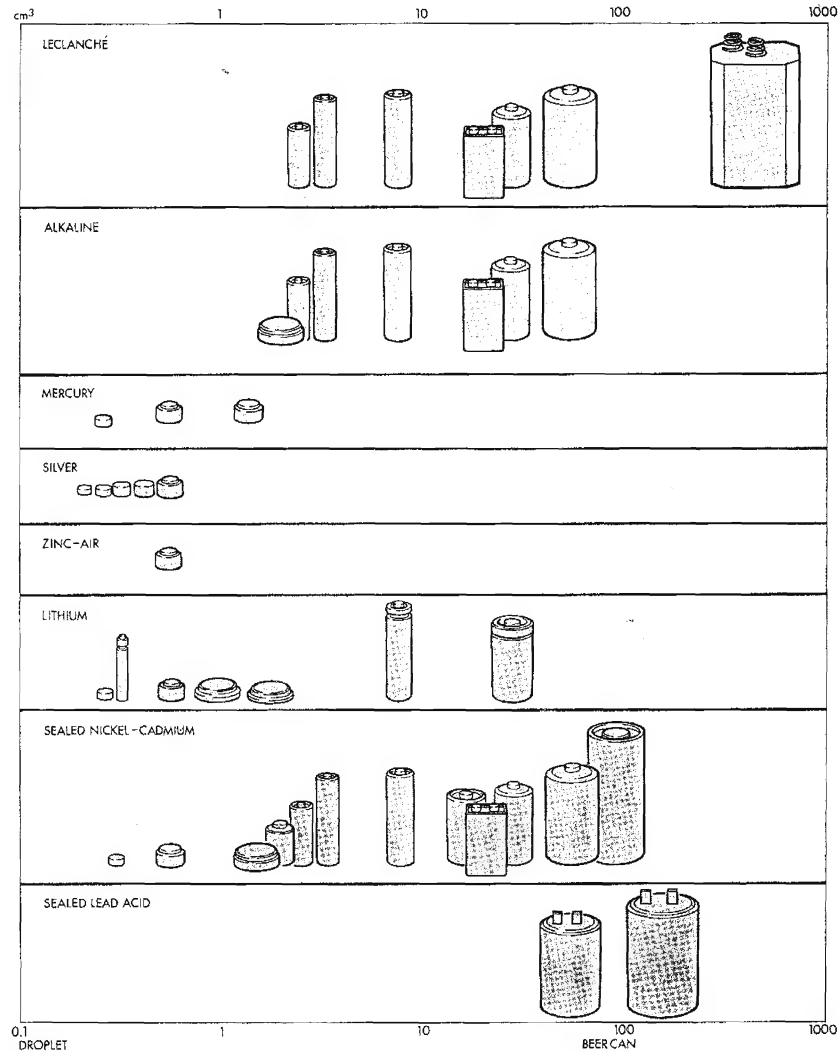


Table 1 Different battery systems arranged according to their volume.

Introduction to pager systems

Battery technology

Batteries come in a wide variety of sizes and shapes. The smaller ones, from droplet to beer can size, are mainly used in portable electronic and portable lighting applications. Without these small batteries our daily life would be very much different. There would be no electric torch, electronic watch, cordless shaver, pocket calculator, portable radio and so on.

Batteries can be divided into two main classes.

A Primary batteries

This type is disposed of after use as it cannot be reused.

Typical sorts of primary battery are:

- zinc manganese dioxide cells, e.g. Leclanché
- zinc-chloride and alkaline
- zinc-mercury oxide cell
- zinc-silver oxide cell
- zinc-air cell
- lithium batteries

B Secondary or rechargeable batteries

This type can be used over and over again because if electrical energy is supplied from an external source the chemical reaction of the battery is reversed and the battery is restored to its original charged condition.

Typical small rechargeable battery types are:

- sealed nickel-cadmium batteries
- sealed lead-acid batteries

Newcomers in the field of rechargeable batteries are the:

- nickel metal-hydride battery
- re-chargeable alkaline
- re-chargeable lithium cell

These types of batteries are still relatively expensive and exhibit no "established" construction yet.

Larger batteries are termed as those having a volume greater than that of a beer can. They are almost exclusively used in automotive or stationary applications that we all meet in our daily routine.

Typical examples are:

- the cranking of a car is done by a lead-acid battery about the size of a shoe box

- jet aircraft motors are started by nickel-cadmium batteries the size of a jerry can.
- telephone services are ensured against mains failure by the use of stand-by lead-acid batteries the size of barrels
- medium sized lead-acid and nickel-iron batteries are used in electric vehicles to provide pollution-free transport in towns and buildings.
- in the event of a mains failure, batteries provide us with emergency lighting to guide us safely through buildings and subways.

Virtually all of these larger batteries are rectangular in shape and rechargeable.

PORTABLE BATTERIES

There are many different types and sizes of portable batteries from which to choose for any application. The energy requirement and discharge schedule are the two fundamental criteria on which the correct choice is made.

Batteries for the larger portable apparatus are usually cylindrical, flat or rectangular in form. Furthermore, the battery systems employed are mainly the zinc-manganese and alkaline manganese types.

With the advent of micro-electronics, very small portable apparatus became possible with a consequent need for very small batteries. These batteries were developed in button, coin and pin forms. In connection with providing the highest possible energy content these types of battery generally use different systems to the larger types:

- zinc-mercury
- zinc-silver
- zinc-air
- lithium.

Rechargeable nickel-cadmium batteries are sometimes used in place of primary batteries in portable apparatus. They are available in cylindrical form for the more general application and in button form for use in such apparatus as hearing aids. Small lead acid rechargeable batteries have been mainly supplied in rectangular form up to now although batteries in cylindrical form are becoming more popular.

Introduction to pager systems

Battery technology

THE LECLANCHÉ BATTERY

This type of battery is the most widely known and billions of them are used every year throughout the world. Its proper name is a zinc-manganese dioxide battery and is used in appliances where ample space is available and where it has to operate from a number of hours up to about a year.

In addition to the names Leclanché battery and zinc-manganese dioxide battery it is also known as: zinc-carbon battery, dry cell and dry battery.

The name Leclanché comes from its inventor. George Lionel Leclanché (1838-1882) started manufacturing batteries around 1860 in Brussels. Although the principle has remained the same, the battery industry has introduced many changes during the last 120 years.

The modern Leclanché battery consists of a zinc container acting as the negative electrode and manganese dioxide as a positive electrode. The two electrodes are insulated from one another by a separating layer of electrolyte. Usually this electrolyte comprises of ammonium chloride but in the heavy duty types, zincchloride is used. The separating layer can be a gel in the so-called paste lined batteries, or paper as used in the so-called paper lined batteries. Because the paper lining occupies less space and improves the filling factor, the batteries utilizing this method usually have a higher capacity. There are other factors that influence capacity too: size, the 'purity' of the manganese dioxide and the type of electrolyte.

Particularly in conditions of higher discharge, the zincchloride types can withstand more continuous drain. However, ammoniumchloride types are superior at low discharge conditions (i.e. either lower currents or long rest periods). Furthermore, ammonium chloride batteries are cheaper.

A great deal of attention is given to the sealing and packaging of the cell. This is not only to ensure an attractive product but mainly to increase leak resistance under adverse environmental conditions and to maintain optimal performance after long-term storage.

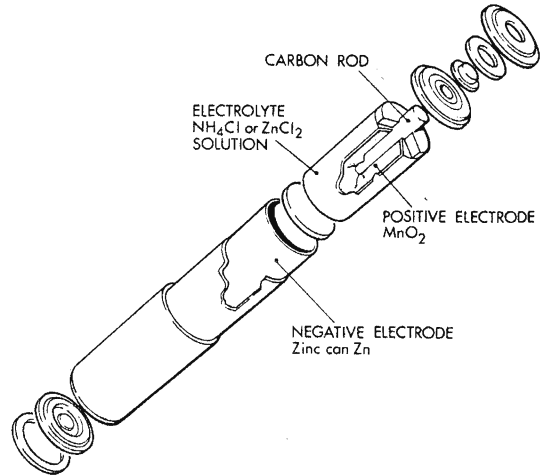


Fig. 2 Construction of a modern Leclanché battery.

Due to both chemical and physical reasons, water is less liable to be emitted from cells with zincchloride electrolyte. This fact combined with superior, more expensive sealing preventing loss of water, gives a longer shelf life and a better leak resistance than the ammonium chloride type.

Zinc-manganese batteries have a nominal voltage of 1.5 V. During discharge, the voltage gradually drops towards the endpoint voltage at which time the battery has to be replaced.

The batteries recuperate during rest periods, a fact that affects the total available capacity. With the zincchloride electrolyte type, however, the battery is able to deliver higher currents continuously with less need to recuperate; a considerable improvement on the more conventional Leclanché types. In fact, its characteristics approach those of the more expensive alkaline manganese types although not with relation to low temperature behaviour.

Introduction to pager systems

Battery technology

Summarizing, it can be said that for light loads and intermittent use, the lower cost ammonium chloride battery is well suited and that for heavier loads of a more continuous nature, the zincchloride battery is preferable.

The capacity is very much dependent on the current drain and the discharge schedule as shown in Fig. 3

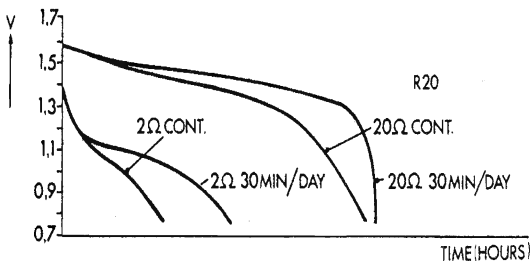


Fig. 3a Typical discharge curves for zinc-manganese dioxide/ammoniumchloride batteries.

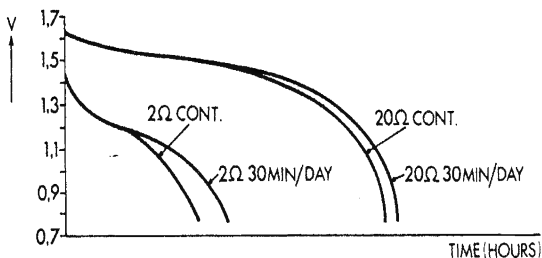


Fig 3b Typical discharge curves for zinc-manganese dioxide/zincchloride batteries.

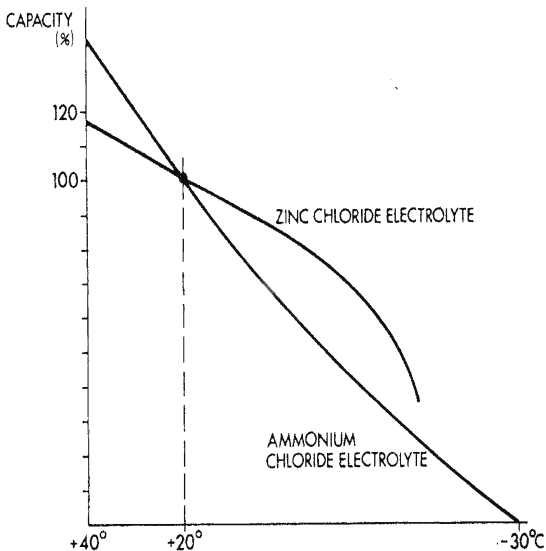


Fig. 3c Typical curves for temperature behaviour

THE ALKALINE BATTERY

The first information on the development of an alkaline manganese battery appeared in papers written in 1952. It was introduced on the market around 1959. Like the Leclanché batteries just described it too is a zinc-manganese dioxide battery. However, the electrolyte used is a caustic solution. Furthermore, the construction of the alkaline battery is totally different.

The negative zinc electrode is placed in the inside of the battery whilst the positive manganese dioxide electrode is placed around the zinc electrode. This means that the outer steel container acts only as a casing and takes no part in the chemical process of the battery. This fact together with the very effective sealing technique used leads to a very good leak resistance and a long shelf life.

Introduction to pager systems

Battery technology

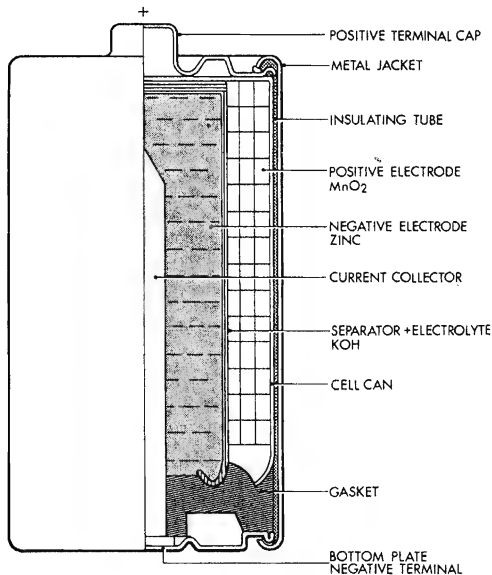


Fig. 4 Construction of an alkaline battery

As far as outside appearance and cell voltage are concerned, the alkaline battery is comparable to the Leclanché battery. However, its output performance at high loads is superior.

Alkaline batteries are suitable for heavy and continuous current drains; its higher capacity is less dependent on the load and discharge schedule. Energy densities are two to three times higher than comparable Nicads. This type of battery can also function at lower temperatures. Typical discharge curves at various temperatures are given in Fig. 5.

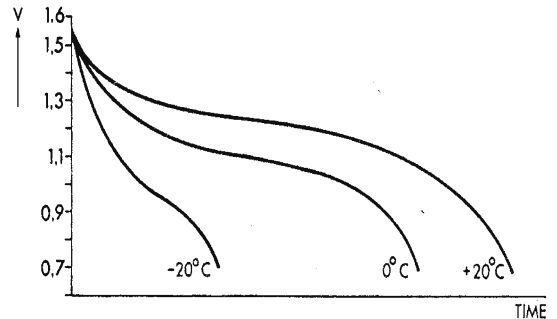


Fig. 5 Typical discharge curves for alkaline manganese batteries

Rechargeable alkaline manganese batteries

Whereas it is possible to construct an alkaline battery in a way that allows it to be recharged to a certain extent, those types normally on sale are not intended to be recharged. Attempts to recharge can be very dangerous as it can lead to cell leakage and even explosions.

The rechargeable alkaline batteries exhibit a slightly lower capacity than non-rechargeable types and a self-discharge that is usually around 0.01 percent per day. The number of charging cycles of this battery is still rather low at twenty to fifty times.

THE MERCURY BUTTON CELL

The zinc-mercuric oxide cell was first introduced around 1940 when it was used in large cells for military and other purposes. Since then the smaller, button type version has been developed. It is this type which is usually found in applications like hearing aids and photographic exposure meters.

Introduction to pager systems

Battery technology

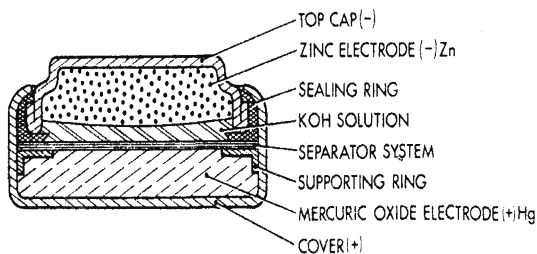


Fig. 6 Construction of a mercury button cell

The high energy density active material mercuric oxide is used for the positive electrode: powdered zinc being used for the negative electrode. To complete the chemical system there is a caustic electrolyte.

The nominal voltage of the cell is 1.35 V which is very stable during discharge. Further advantages of this type are its high capacity per unit volume and its hermetic sealing giving rise to a long shelf life during which the voltage characteristics are not affected. Furthermore, compared with the Leclanche battery, its capacity is less dependent on the discharge schedule.

The cell is not suitable for high currents nor low temperature operation. However, its high energy content, nearly flat discharge curve and durability make it very suitable for use in small appliances.

There is a second version of this type of cell, one having manganese dioxide together with mercuric oxide. This version has a nominal voltage of 1.4 V, accepts higher current drains and is somewhat less expensive.

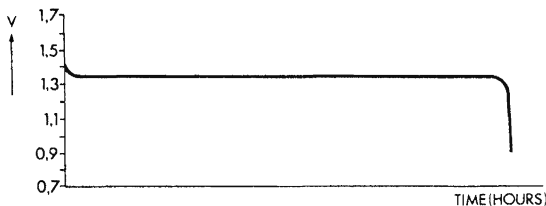


Fig. 7a Typical discharge curve for mercury oxide, low current drain type

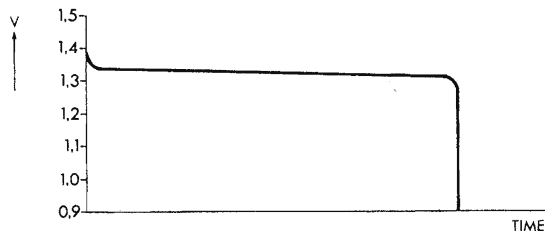


Fig. 7b Typical discharge curve for mercury oxide, high current drain type.

THE SILVER CELL

The zinc-silver oxide button cell has many similarities with the zinc mercuric oxide cell, not least of which is its construction and appearance. It was introduced around 1960 to satisfy the demand for a higher voltage than that obtained from mercury.

There are two types: monovalent and divalent silver oxide. Although the monovalent version is more widely used, the divalent version has a higher capacity but the same voltage characteristics.

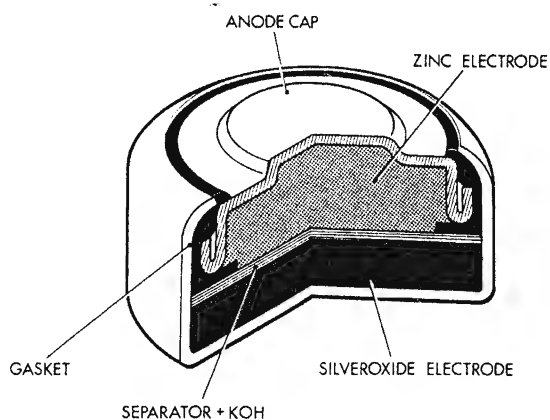


Fig. 8 Construction of a silver button cell

Introduction to pager systems

Battery technology

The discharge voltage is 1.5 V and very stable during discharge as shown on the curve of Fig. 7.

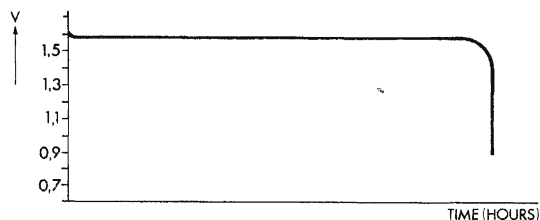


Fig. 9 Typical discharge curve for silver button cell.

The silver cell has been specifically designed for low rate continuous current drain applications. However, there are types available for higher current drains.

THE ZINC-AIR BUTTON CELL

This recent addition to the range of button cells is significantly different to all the other types. Whereas the others have both electrodes within the cell, the zinc-air type has only the zinc electrode; the oxygen of the outside atmosphere acts as the second electrode. Oxygen enters the cell via a specially constructed path through the cell cover. The most important advantage of this is that the zinc-air cell has sufficient interior space to accommodate approximately twice the amount of zinc as is possible with mercury or silver cells, giving rise to double the service lifetime.

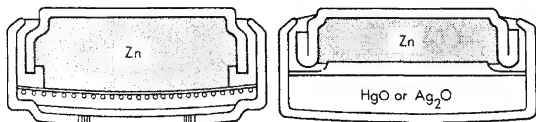


Fig. 10a Construction of the zinc-air cell compared to the conventional button cell

In practice, the cells are kept sealed from the atmosphere by attaching them to an air-tight self-adhesive tape. The cells are activated when the tape is removed. This tape removal is often found to be annoying for users, not accustomed to this type of battery cell.

There are a number of ways in which the zinc-air cell differs from other types of button cell:

- an air access path is provided to ensure that sufficient oxygen can enter the cell but which restricts the ingress of water and carbon dioxide to such an extent that leakage is prevented.
- a very thin membrane which acts as a catalyst to the oxygen electrode reaction.
- ample space to accommodate the zinc, and some room to store water that might penetrate the cell under extremely adverse environmental conditions.

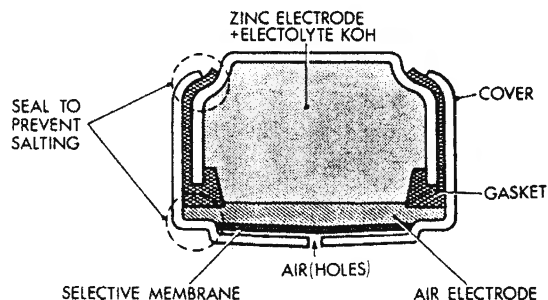


Fig 10b Construction of a zinc-air cell.

The cell discharge curve as shown on Fig. 11 is very flat compared with mercury and has a slightly lower voltage than silver button cells.

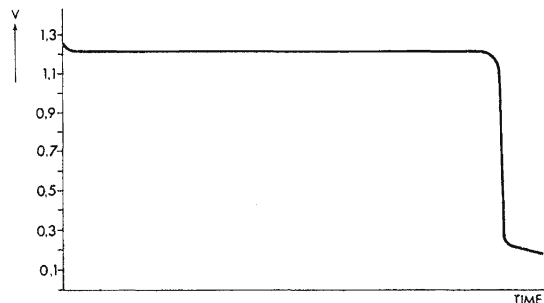


Fig. 11 Typical discharge curve of a zinc air button cell, AR44.

The large energy content of this type of cell makes it ideal for hearing aids, especially the high power types.

Introduction to pager systems

Battery technology

NICKEL-METAL HYDRIDE BATTERIES

Relatively new type of rechargeable batteries, with promising characteristics, often referred to as a strong battery competitor for the next century.

Reports of development of this battery date from early 1960, but it was not until the early 1980 that they became commercially available. The NiMH battery is still under development and many of its characteristics are not yet stabilized. This is also apparent when testing NiMH batteries from different manufacturers.

Although differences exist between various brand names, some characteristics of this type of batteries are of a more general nature and made the shining stars of current developments.

The advantages of this type of batteries are its relatively high capacity (tens of percents over regular Nicad) and lack of the "memory-effect". Also the environmental aspects make it interesting for the future as they contain no toxic metals.

Disadvantages of the currently available types are its lower number of charge/discharge cycles (less than half the Nicad types), its charging/discharging characteristics with a lower current and its higher self-discharge. Also the price for this new development is still relatively high.

Especially the disadvantages are currently under the attention of development laboratories and new solution may be found in the coming period. It is expected, that the NiMH type of battery will be especially suited for portable telecommunication applications. The NiMH battery has a cell voltage of around 1.25 V.

LITHIUM BATTERIES

Lithium batteries are a group that is totally different from all other types. The main reason is that they have a nominal voltage of 3 V compared to the 1.2 to 1.5 V range of other types. This is due to the use of the metal lithium instead of the zinc electrode as is the case with Leclanché, alkaline, mercury, silver and air cells. Because of this high voltage the lithium battery offers a very high energy content: when compared to Nicad batteries, the energy density is three to four times higher. The larger lithium batteries have the further advantage of being lighter in weight than their equivalents in other types and exhibit a very low self-discharge enabling a fully charged shelf-life for a number of years. On the negative side are its (very) low charging and discharging current. Also, the low number of charging cycles, down to one fifth compared to Nicads, and its high price, which is not likely to come down to its competitors makes the lithium cell penetrate niche markets only for years to come.

Although lithium is a very common element, its high reactivity makes it difficult to obtain in the metallic state. However, modern metallurgical techniques similar to those used for the melting of aluminium and titanium have recently overcome the difficulties. Only electrolytes that contain no water can be used, again due to the high reactivity of the lithium itself.

This also means that disposal at the end of its useful life is a matter of concern: corrosion may cause water to leak into the cell, eventually leading to a violent reaction.

There are a large number of materials that can be used for the second electrode: both organic and inorganic. Inorganic electrodes have the advantage of being slightly easier to manufacture. The most common material used as the second electrode is manganese dioxide, similar to that used in the Leclanche battery. For special purpose applications materials such as carbon fluoride, thionyl chloride and vanadium peroxide are used.

Introduction to pager systems

Battery technology

Lithium cells are available in various shapes and sizes, ranging from button cells up to the larger cylindrical forms. Examples of typical constructions are given in Fig. 12.

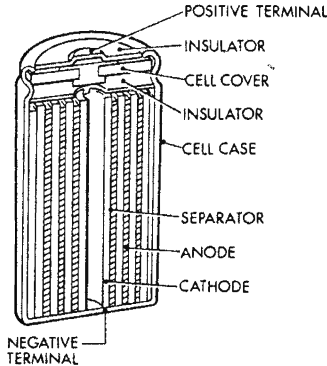


Fig. 12a Cylindrical-type lithium battery.

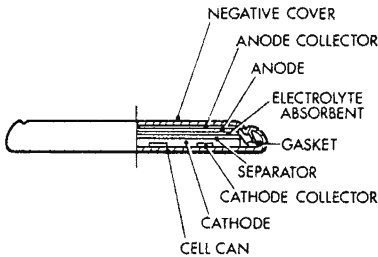


Fig. 12b Flat-type lithium battery.

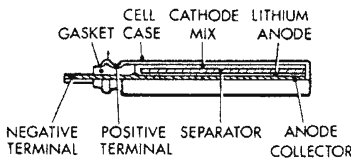


Fig. 12c Pin type lithium battery.

The different voltage produced by lithium batteries prevents them from being used as direct replacements for conventional primary types.

Hermetic sealing of the cell is of the utmost importance due to the possible ingress of water and its violent

reaction with lithium. Perfect sealing together with a very low self discharge give these types of battery a very long shelf life which can be five to ten years long.

The absence of water from the cell makes use at very low temperatures possible. Some lithium cells are designed to operate even at -40°C . However, due to the relatively low conductivity of the various electrolytes, the internal resistance of the cell is high and it cannot supply large currents for longer periods.

Lithium cells are used for applications where low current drains are required over a very long period. Typical application are pacemakers and long-life watches. They are even used to supply the power to operate a light emitting diode on top of a fishing float.

Typical discharge curves and storage characteristics are given in Fig. 13.

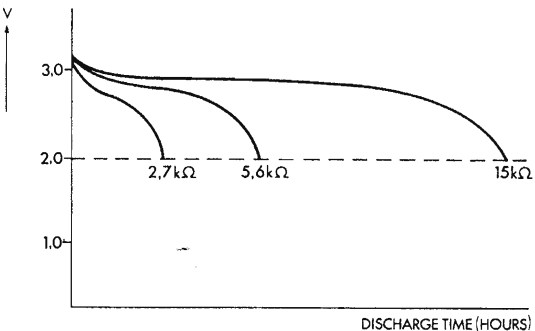


Fig. 13a Typical discharge curves of a small Li-MnO₂ cell

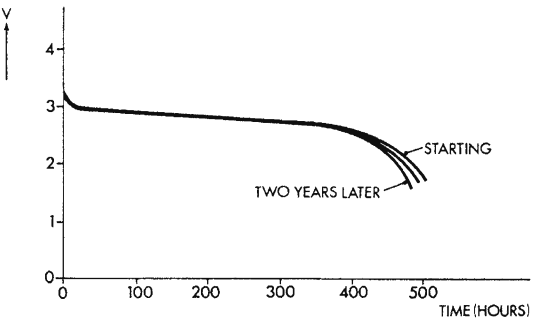


Fig. 13b Storage characteristics of a Li-MnO₂ cell

Introduction to pager systems

Battery technology

Rechargeable lithium batteries

These type of batteries are becoming available for special cases where the high energy -to-weight ratio is of extreme importance. This newcomer is still expensive and hardly out of the experimental phase. Operating voltages are in the 3-4 volt range and the life expectancy is over five-hundred charge cycles. Self discharge is somewhat higher than alkaline types, but still very much lower than Nicads. The output current has gone up dramatically compared to the older non-rechargeable lithium type.

A problem remains the very precise charging regime; some specifications are mentioning charging at 4.2 volt \pm 50 mV. under current limiting conditions.

SEALED NICKEL-CADMIUM BATTERIES

The nickel-cadmium battery was developed around the turn of the last century with much pioneer work being carried out in Sweden. Its introduction coincided with that of the nickel iron battery used as a power source in electric vehicles. These days the sealed cylindrical type of Nicad battery (as it is commonly known) is available in a variety of sizes ranging from button size to one approximately the size of a beer can.

The advent of sealed nickel cadmium batteries has made it feasible to use rechargeable batteries in portable devices that have a high current drain or are used very often. A typical application is an electric shaver.

Also the high number of discharge cycles (up to 1000 plus) and the excellent load performance, even at the low temperatures have made this battery penetrate many portable applications. Further favourable qualities are the simple storage and transportation provisions; most air freight companies have no problem transporting them.

In the cylindrical types the electrodes are based on a very thin porous, sintered nickel matrix. These electrodes are wound with an interleaving separator to fill the outer container. In this way, a large electrode surface is gained giving high capacity values. The sealed versions of the battery are maintenance free and can operate in any position.

The system is very robust in that it can withstand over-charging and deep discharge. Prolonged periods of storage in a discharged condition should be avoided. Under these circumstances, thin needles of crystalline metal may form, that puncture the separator between the positive and negative plate. This will cause high self-discharge and usually mean the end of its useful life.

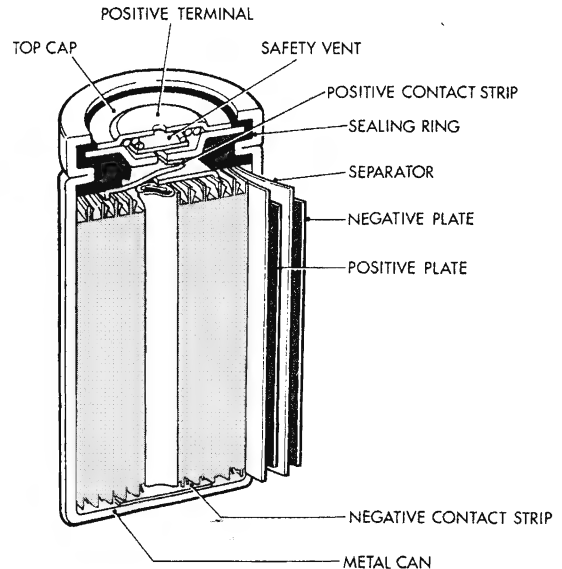


Fig 14 Construction of a typical sealed nickel cadmium battery

If the battery is consistently used in a shallow discharge pattern or in a trickle charge condition it may exhibit the so called memory effect whereby the capacity of the battery is seemingly lower than its nominal capacity. The effect can be remedied by subjecting the battery to full discharge followed by recharging; this is usually also the regime under which this type of batteries performs best. The memory effect was found in the earlier days of production but is virtually not found in our present days any more.

When fast-charging the Nicad battery, "reflex loading" or "reverse load charging" improves capacity and adds to

Introduction to pager systems

Battery technology

the life expectancy. This charging scheme exposes the battery to short periods of discharging during the recharging period; this promotes internal gas-recombination, thus boosting the efficiency of the charging operation. Reflex loading may also add ten to twenty percent to the useful life of the battery.

Typical discharge curves, the effect of overcharging and the influence of temperature are given in Fig. 15.

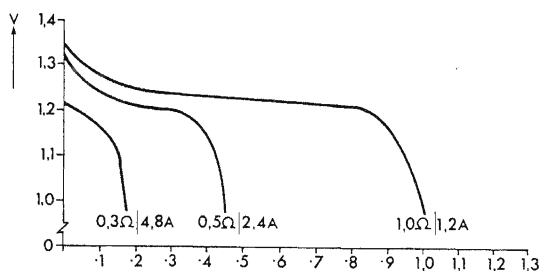


Fig. 15a Typical discharge curves

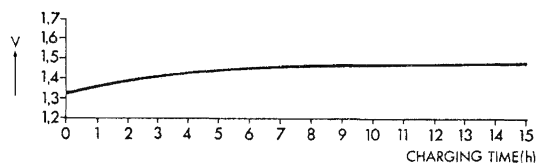


Fig. 15b Voltage during charging with constant current

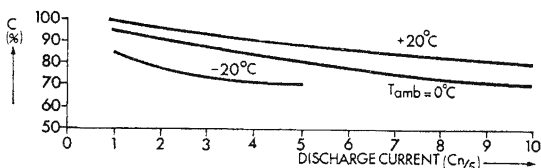


Fig. 15c Influence of temperature and current-drain on capacity

Although the nominal voltage of a Nicad battery is 1.25 V compared to the 1.5 V of a Leclanché cell, it can be directly interchanged due to its flat discharge curve compared to the sloping curve of the Leclanché cell.

The versatility of the Nicad battery is greatly enhanced by its very long typical life time (5 to 7 years) and its extended cycle life (up to 1000 cycles). Special types are suitable for trickle charging and are excellent sources for emergency power applications.

SEALED LEAD ACID BATTERIES

Since about 1975 the battery industry has been producing sealed lead acid batteries for use in applications where an operating time of several to many hours is needed on one charge. They are employed in applications where intensive use makes dry batteries expensive and inconvenient.

For (trans-)portable applications we find them in camcorders, laptop computers and medical equipment. The sealed lead acid battery has no memory effect, may be trickle charged for long periods of time, and is relatively cheap. The comparably low penetration in smaller portable systems is mainly due to its relatively low energy density, its low-current charging requirements and low charge/discharging cycle life and its reduced power at low temperatures. Also, because of its composition, it is regarded as potentially threatening to the environment.

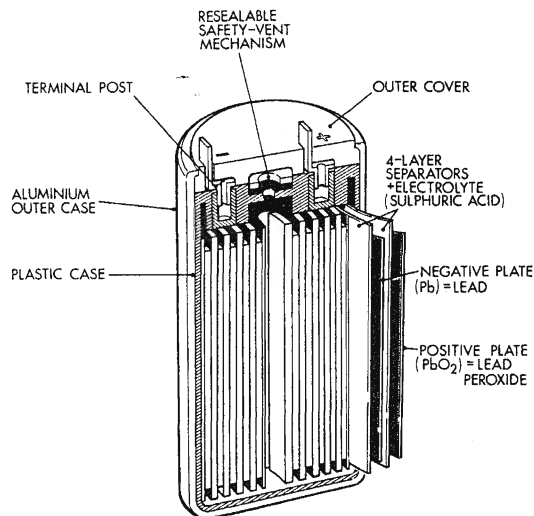


Fig. 16 Construction of a sealed lead acid battery

Introduction to pager systems

Battery technology

The construction of the battery is more or less comparable to the Nicad battery. Its sealed construction makes it maintenance free. However, the battery is sensitive to storage in a deeply discharged condition. On the other hand, self-discharge is less than that of the nickel-cadmium cell. A shelf life of over 2 years is possible for a fully charged lead acid battery.

The nominal and operating voltage is 2 V compared to 1.2 V for Nicad and 1.0 to 1.5 V for dry batteries.

Also, as battery technology is constantly progressing, the information on a particular type may not be accurate any more. Especially for the newer battery types, better designs may move a particular battery into applications that were out of reach before.

The following tables should therefore be regarded for general comparison reasons only; it is recommended to get the latest information directly from the battery manufacturer.

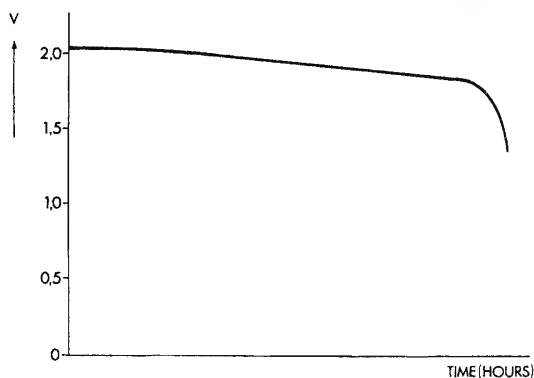


Fig 17 Typical discharge curve of a sealed lead acid battery

OVERVIEW ON BATTERY TYPES

A battery is selected according to the specific requirements of the application. For applications that should be left unattended for a long period of time, the initial price of the battery may be of less importance than the cost of regular maintenance. For other applications, the very constant cell voltage over life may be a favourable quality when savings on stabilizing circuitry can make the final device smaller or cheaper. A third application may require occasional deep discharges on high current, calling for different selection criteria again.

Introduction to pager systems

Battery technology

Non rechargeable batt. types	energy density Wh/kg	cell voltage *	charge/ disch. current	self-discharge	purch. cost	environment load	remarks
Standard "Dry" cell	80	1.5	-/mod	v. low	v.low	mod	1
Alkaline	120	1.4	-/high	v.low	low	mod	2
Mercury butt.	100	1.3	-/low	v.low	high	high	3
Zinc/silver bt	120	1.5	-/low	v.low	high	mod	4
Zinc/air cell	120	1.2	-/low	low	high	mod	4
Lithium	150	3.0	-/low	v.low	high	depends	5

Table 2 Comparison of non-rechargeable batteries

* Cell voltage is averaged over life

remarks:

1 - readily available

2 - cost effective performer

3 - not for new applications; environmental hazard

4 - very constant voltage over life

5 - for low current over long periods

Rechargeable battery types	energy density Wh/kg	cell voltage *	charge/ disch. current	self-discharge	purch. cost	environment load	char/ disch. cycles
Re-ch Alkal.	100	1.3	low/mod	v. low	low	mod	low
NiMH	70	1.2	mod/high	high	high	mod	mod
Re-ch Lithium	120	2.8	low/mod	v.low	high	low	high
Nicad	60	1.2	high/high	mod	mod	high	high
Sld. Lead acid	30	2.0	mod/high	mod	low	high	mod

Table 3 Comparison of rechargeable batteries

* Cell voltage is averaged over life

Introduction to pager systems

Supply concepts

GENERAL

Pager systems are attractive because of their small size, their user-friendly way of operation and their long operational life on batteries compared to other (wireless) ways of communication.

As this long battery life is related to the power consumption of the pager circuit, most pager ICs are developed with battery economics in mind.

As a rule of thumb, circuits that operate on a higher frequency will consume more power than low(er) frequency circuits. This is one of the reasons why pager IC manufacturers are separating the supply to (especially pager-) receiver ICs: by carefully optimizing between active- and stand-by-periods, high- and low-current consumption parts and taking establishment timings into account, extra power savings may be possible.

Although power and power saving are important issues at the design of integrated circuits, also the minimum operational voltage may be important. This minimum voltage will be a factor when the type of battery for the pager design is being considered (EMK vs power drain) and/or more than one battery element should be used.

As it turns out, power consumption and battery life although being related, are two separate issues that have to be calculated independently in every circuit under consideration.

In the following paper, various supply schemes will be visited, using realistic assumptions for the circuit parameters.

SUPPLY CONFIGURATIONS

In this paper we distinguish four different supply schemes. These four supply schemes are given as examples for comparison reasons only.

For all these four situations we assume that:

- pager receiver is UAA2080, pager decoder is PCF5001
- battery voltage is constant over life-time
- bias currents are independent of supply voltage

- voltages and currents:

battery voltage	$U_{bat} = 1.5 \text{ V}$
battery capacity	$C_{bat} = 1000 \text{ mAh}$
frond-end current	$I_{fro} = 2 \text{ mA}$ via pin 28, 24/25, 12/13 (H-version)
decoder + dig. circuits	$I_{dig} = 60 \mu\text{A} + 140 \mu\text{A}$ ($= 200 \mu\text{A}$)
receiver duty-cycle	$d = 8\%$
DC/DC converter eff.	$\eta = 70\%$
U_{out} DC/DC converter	$U_{out} = 2.2 \text{ V}$

Supply schemes:

- I : - Two 1.5 V cells;
- 3 V supply for receiver plus decoder plus other dig. circuits
- II : - One 1.5 V cell and DC/DC converter;
- 2.2 V supply for receiver plus decoder plus other dig. circuits
- III : - Two 1.5 V cells;
- 1.5 V for receiver front-end
- 3.0 V for receiver back-end plus decoder plus other dig. circuits
- IV : One 1.5 V cell and DC/DC converter;
- 1.5 V for receiver front-end
- 2.2 V for receiver back-end plus decoder plus other dig. circuits

SUPPLY SCHEME 1

Two 1.5 V cells; 3 V supply for receiver, decoder and other circuits, see figure 1.

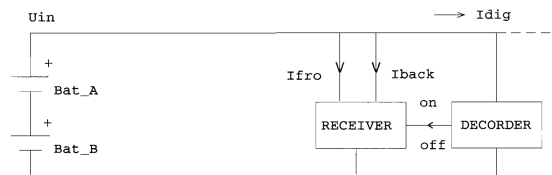


Fig. 1 Supply scheme with 3 V for receiver and decoder

Introduction to pager systems

Supply concepts

Power dissipation.

The power dissipated by the receiver (front-end and back-end) plus the power dissipated by the digital circuits equals the power delivered by the two batteries.

The average power consumption of the receiver equals:

$$P_{rec} = d * 2 * U_{bat} * (I_{fro} + I_{back}) = 0.6 \text{ mW}$$

The digital part consumes:

$$P_{dig} = 2 * U_{bat} * I_{dig} = 0.6 \text{ mW}$$

The total power dissipation then becomes $P_{rec} + P_{dig} = 1.20 \text{ mW}$.

The power delivered by Bat_A (equal to Bat_B):

$$P_{Bat_A} = U_{bat} * I_{bat} = 0.6 \text{ mW}$$

Battery life-time.

The total current through both batteries equals the constant current through the digital circuit plus on/off switched current of the receiver. Note that the average current of the receiver approx. equals the current of the digital part!

$$\begin{aligned} I_{Bat_A} &= I_{Bat_B} = I_{dig} + d * (I_{fro} + I_{back}) = \\ &= 0.2 + 0.08 * (2.0 + 0.5) = 0.4 \text{ mA} \end{aligned}$$

From this we calculate the battery life-time:

$$Bat_It = C_{bat} / I_{bat} = 1000 \text{ mAh} / 0.4 \text{ mA} = 2500 \text{ h}$$

Conclusion 1:

In a two cell concept with 2 cell supply for the receiver front-end the power consumption of the receiver and digital parts are approx. the same. The two batteries deliver both half the power; both batteries have the same life-time.

SUPPLY SCHEME II

One 1.5 V cell plus a DC/DC converter. One supply for receiver, decoder and other circuits, see figure 2.

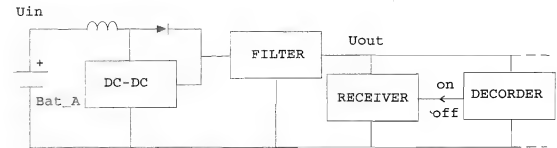


Fig. 2 Supply scheme with 1.5 V battery

Power dissipation

The power dissipated by the receiver (front-end and back-end) plus the power dissipated by the digital circuits depends on the output voltage U_{out} of the DC/DC converter. Note that the lower U_{out} , the lower the power dissipation of the receiver and digital circuits will be. A good choice for $U_{out} = 2.2 \text{ V}$.

The average power consumption of the receiver equals:

$$P_{rec} = d * U_{bat} * (I_{fro} + I_{back}) = 0.44 \text{ mW}$$

The digital part consumes:

$$P_{dig} = U_{out} * I_{dig} = 0.44 \text{ mW}$$

The power delivered by Bat_A equals the power delivered to the converter:

$$\begin{aligned} P_{Bat_A} &= P_{conv_in} = (P_{rec} + P_{dig}) / \eta = 0.88 / 0.7 = \\ &= 1.26 \text{ mW} \end{aligned}$$

Conclusion 2:

By using a high efficiency (>70%) DC/DC converter with low output voltage (<2.2 V) the total power consumption is approximately the same as for a two 1.5 V cells, as in power supply scheme I.

Introduction to pager systems

Supply concepts

Battery life-time

The total current through the battery can be calculated from the power delivered by this battery.

$$IBat_A = PBat_A/UBat = 1.26/1.5 = 0.85 \text{ mA}$$

From this we calculate the battery life-time:

$$Bat_It = Cbat/IBat = 1000 \text{ mAh}/0.85 \text{ mA} = 1176 \text{ h}$$

Conclusion 3:

By using a high efficiency (>70%) DC/DC converter with low output voltage (<2.2 V) the battery life-time is approximately half the life-time of the two batteries as in supply scheme I.

SUPPLY SCHEME III

Two 1.5 V cells; 1.5 V for receiver front-end, 3 V for receiver back-end plus decoder plus other circuits, see figure 3.

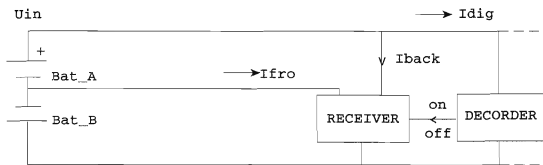


Fig. 3 Supply scheme using "split-battery"

Power dissipation

The total power dissipation is the sum of the power dissipated by the receiver front-end and back-end plus the power dissipated by the digital circuits.

$$P_{tot} = d \cdot U_{bat} \cdot I_{fro} + d \cdot 2 \cdot U_{bat} \cdot I_{back} + 2 \cdot U_{bat} \cdot I_{dig} \\ = 0.24 + 0.12 + 0.6 = 0.96 \text{ mW}$$

This power is partly delivered by Bat_A and partly by BAT_B:

$$PBat_A = U_{bat} \cdot IBat_A = 1.5 \cdot (0.08 \cdot 0.5 + 0.2) \\ = 0.36 \text{ mW}$$

$$PBat_B = U_{bat} \cdot IBat_B = 1.5 \cdot (0.08 \cdot 2.0 + 0.08 \cdot 0.5 + 0.2) \\ = 0.6 \text{ mW}$$

Conclusion 4:

By feeding the receiver front-end with 1.5 V instead of 3 V the total power consumption reduces approx. 20%. The power consumption of the digital part becomes more dominant. Moreover the current through battery B is almost twice the current through battery A.

Battery life-time

The total current through both batteries determine the battery life-time.

$$IBat_A = I_{dig} + d \cdot (I_{back}) = 0.2 + 0.08 \cdot (0.5) = 0.24 \text{ mA}$$

$$IBat_B = I_{dig} + d \cdot (I_{fro} + I_{back}) = 0.2 + 0.08 \cdot (2.0 + 0.5) \\ = 0.4 \text{ mA}$$

From this we calculate the battery life-time:

$$Bat_A_It = Cbat/IBat_A = 1000 \text{ mAh}/0.24 \text{ mA} = 4166 \text{ h}$$

$$Bat_B_It = Cbat/IBat_B = 1000 \text{ mAh}/0.4 \text{ mA} = 2500 \text{ h}$$

Conclusion 5:

In a two cell supply concept with 1.5 V for the receiver front-end the power consumption of the pager is significantly smaller than with 3 V at the front-end. However, the battery life-time of the most heavily loaded battery is equal to the life-time in a conventional 2-cell concept as in supply scheme I. A 1-Volt front-end saves power, but does not increase battery life-time: when one battery is empty, two will be replaced!

Introduction to pager systems

Supply concepts

SUPPLY SCHEME IV

One 1.5 V cell plus DC/DC converter. 1.5 V for receiver front-end, 2 - 3 V for receiver back-end plus decoder plus other circuits, see figure 4.

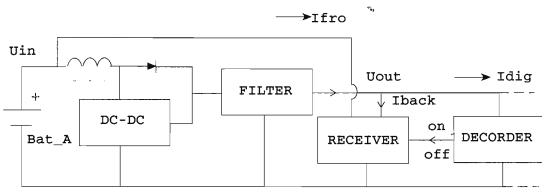


Fig. 4 Supply scheme using optimized powering

Power dissipation

The power dissipation of the receiver equals the power dissipated by the receiver front-end and back-end plus the power dissipated by the digital circuits. Losses of the DC/DC converter give some additional power consumption.

$$P_{fro} = d \cdot U_{bat} \cdot I_{fro} = 0.24 \text{ mW}$$

$$P_{out_dc/dc} = d \cdot U_{out} \cdot I_{back} + U_{out} \cdot I_{dig} \\ = 0.528 \text{ mW}$$

The total power delivered by Bat_A equals:

$$P_{Bat_A} = P_{fro} + (P_{out_dc/dc})/n = 0.24 + 0.528/0.70 \\ = 0.99 \text{ mW}$$

Conclusion 6:

The power to be delivered by Bat_A is almost equal to the power to be delivered by Bat_A plus Bat_B in a 2-cell, 1.5 V frond-end concept as in supply scheme III.

Battery life-time

The total current through the batteries determines the battery life-time.

$$I_{Bat_A} = P_{Bat_A} / U_{Bat_A} = 0.99 / 1.5 = 0.66 \text{ mA}$$

From this we calculate the battery life-time:

$$Bat_A_It = C_{bat} / I_{Bat_A} = 1000 \text{ mAh} / 0.66 \text{ mA} \\ = 1515 \text{ h}$$

Conclusion 7:

In a 1-cell supply concept with 1.5 V for the receiver front-end the power consumption of the pager is almost the same as for a 2-cell supply concept with 1.5 V front-end as in supply scheme III. The battery life-time of this 1-cell concept (1515 h) is, in this example, 17% more than halve the life time of a 2-cell concept with 1.5 V front-end (2500 h) as in supply scheme III.

SUMMARY OF RESULTS

supply scheme	Number of cells	Power dissipation receiver + dig.	Effective battery life-time
I	2	1.2 mW	2500 h
II	1+DC/DC	1.26 mW	1176 h
III	2	0.96 mW	2500 h
IV	1+DC/DC	0.99 mW	1515 h

Conclusion 8:

Using a 1 V frond-end in a 2-cell supply (scheme III) saves power but battery life-time remains the same as for a 2-cell supply with 2 V frond-end (scheme I). Using a 1 V frond-end in a 1-cell supply scheme with a high efficiency (>70%), low voltage (<2.2 V) DC/DC converter saves power and increases battery life-time (scheme IV).

CHAPTER 4

PAGER RECEIVERS

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Pager receivers

Antenna aspects

1. FUNDAMENTAL CHARACTERISTICS

1.1 Input Impedance and Far-field Patterns

The loop is one of the primary antenna structures; its use as a receiving antenna dates back to the early experiments of Hertz on the propagation of electromagnetic waves. Today loop antennas have important applications as receiving antennas because of their 360° radiation pattern, inherent frequency selectivity and sensitivity for magnetic fields only (less interference).

Thin wires or similar conductors are bent into the shape of a closed curve which may have any regular configuration. Single loop antennas as well as multi-turn structures including a number of overlaying turns are used. Loops can be divided into two general classes:

- those in which both the total conductor length and the maximum linear dimension of a turn are very small compared with the wavelength
- those in which both the conductor length and the loop dimensions begin to be comparable with the wavelength.

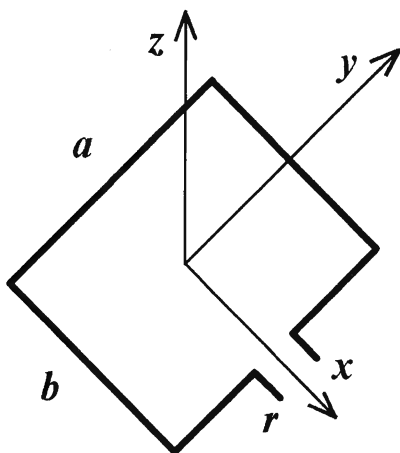


Fig. 1-1 Square loop antenna; $a = b = 50$ mm, wire radius $r = 0.5$ mm.

In the first class, the total length of the conductor in the loop must not exceed 0.1λ . Beyond this length, the current is not the same either in amplitude or phase in every part of the loop. This change in current distribution gives rise to entirely different properties as compared with a small loop.

The basic characteristics of loop antennas are fully described by the input impedance and the radiation pattern. In order to give an impression of the wide variety for the input impedance and the change in radiation patterns for small antennas compared with those up to a perimeter length, λ , some numerical calculations with NEC have been done.

The Numerical Electromagnetic Code, usually abbreviated to NEC, is a very widely used computer modelling technique. It uses an Electric Field Integral Equation (EFIE) to model wires and wire-like objects and a Magnetic Field Integral Equation (MFIE) for surfaces.

The input impedance of the square loop shown in Fig. 1-1 is plotted in Fig. 1-2 as a function of frequency and perimeter length l . As can be seen from the figure a first resonance occurs at $l/\lambda \approx 0.5$ (anti resonant point). The second resonance phenomenon at $l/\lambda \approx 1.09$ (resonant point) appears slightly outside the frequency range shown here. For perimeter lengths below $l/\lambda = 0.14$ the input resistance is extremely low ($R_r \leq 0.5 \Omega$) and the input reactance shows a linear frequency behaviour. The input resistance becomes nearly constant ($R_r \approx 100 \Omega$) at frequencies between the first and the second resonance. It obtains a relative maximum near the point of anti resonance and a relative minimum near the point of resonance. For a one-wavelength perimeter the input reactance is relatively small.

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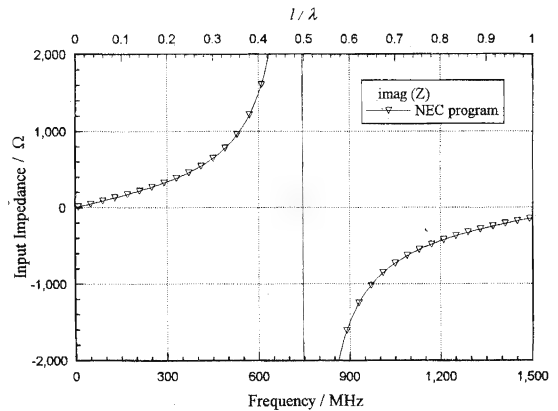
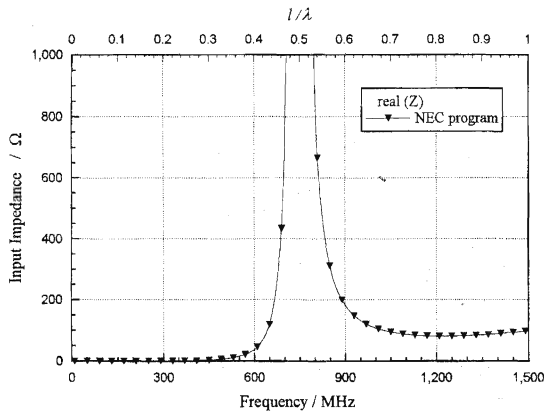


Fig. 1-2 Input impedance of a square loop antenna (dimensions from Fig. 1-1) as a function of frequency and loop perimeter l . Left: Input resistance. Right: Input reactance.

The radiation patterns of electrically small loop antennas are insensitive to the loop shape and depend only on the loop area. The behaviour of a loop antenna as given in Fig. 1-1 is very similar to that of a magnetic dipole directed normal to the plane of the loop, as shown in Fig. 1-3. As with magnetic dipoles the radiation pattern shows its maximum in the plane of the loop and is zero along its axis. These facts follow directly from the current amplitude and phase being constant over the loop, which in turn is due to the loop being electrically small.

Only in case of electrically large loops with a perimeter comparable to $\lambda/2$ or λ , the radiation patterns become sensitive to the shape of the loop and the location of the feeding point.

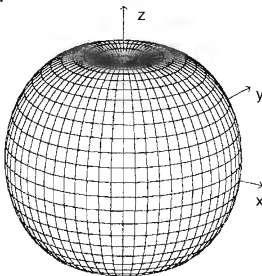


Fig. 1-3 Typical radiation pattern of an electrically small loop antenna, scaled in dB.

1.2 Operating Environment

In section 1.1 an introduction on the basic characteristics of loop antennas have been given. Those characteristics have been fully described by the input impedance and the radiation patterns as a function of frequency. The operating environment for the calculations was assumed to be free space. In pager applications the loop antenna is often mounted on a printed circuit board which itself is surrounded by a dielectric housing. In addition, most of the time the pager is used in close proximity to the human body. Therefore changes in the loop characteristics due to this kind of operating environment can be divided into two classes:

- I. Effects on the input impedance and radiation pattern due to nearby metal parts which change the electromagnetic field surrounding the loop and gives additional loss effects.
- II. Effects caused by the presence of the human body.

Both are disturbing the mode of operation of the loop antenna as a receiving system but can also be used to improve the overall performance of the pager system. In order to use the effects this way they shall be emphasised and discussed in the following paragraphs.

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As has been described above, loop antennas are often mounted on printed circuit boards. In a modelling process, the board can be seen as a metallized plane. The arrangement under numerical investigation is shown schematically in Fig. 1-4.

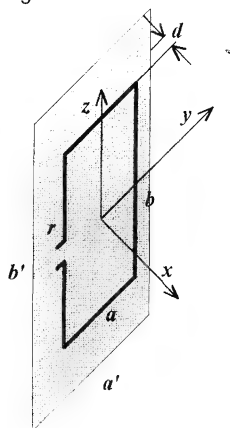


Fig. 1-4 Square loop antenna parallel to an ideal conducting plate at spacing d ;
 $a = b = 50$ mm, $a' = b' = 100$ mm, wire radius $r = 0.5$ mm.

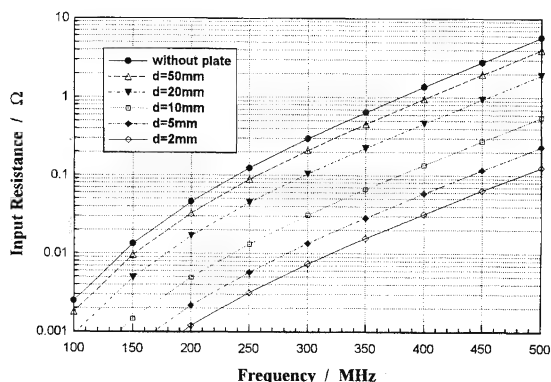


Fig. 1-5 Input resistance of a square loop antenna parallel to an ideal conducting plate (dimensions from Fig. 1-4) as a function of frequency and spacing d .

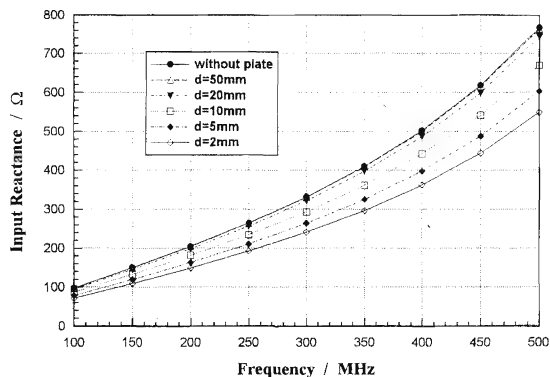


Fig. 1-6 Input reactance of a square loop antenna parallel to an ideal conducting plate (dimensions from Fig. 1-4) as a function of frequency and spacing d .

The curves in Fig. 1-5 and Fig. 1-6 give an impression of the changes in the input impedance of a loop antenna due to the presence of a conducting plate (with ideal metallization). As can be seen from the plots the resistive part of the input impedance decreases strongly for small values of the distance d .

In the calculation the real part of the impedance is only determined by the radiation resistance. The reduction of the radiation resistance can be considered as a reduction of the effective antenna area by the conducting plate. Loss effects such as non-ideal metallization of the wire or the plate have not been taken into account.

The presence of the ground plane beneath the loop also causes a decrease in the reactive part of the input impedance. Reactance changes of about 25% may be observed at a frequency of 500 MHz.

For the inductance the ground plane effect can be explained by applying the method of current images. Assuming the ground plane being extended to infinity, it causes the same effect as a second loop at two "ground-plane spacings" below the actual loop. The image is the reflection of the loop antenna with current flowing in the opposite direction. The opposing current introduces a negative mutual inductance which creates a reduction in the net inductance of the original loop and its image.

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Beside the changes in loop characteristics due to the printed circuit board and the housing of the pager, influences due to the proximity of the human body are also important. Measurements from literature show that the human body has a near-constant conductance over the frequency range up to 500 MHz.

Experiments on the body effect are mostly done using a very simple "body" model, the salt pillar. It consists of a plastic tube of 300 mm diameter, 1.7 m high, filled with salt water. From an electrical point of view the body model is a dielectric resonator of cylindrical shape homogeneously filled with a lossy dielectric.

Fig. 1-7 compares the input impedance of a loop antenna in free space with one mounted on a salt pillar. The proximity of the human body causes a frequency dependent increase in the resistive part. As could be expected only changes in the real part of the input impedance were found. The imaginary part is mainly caused by the loop inductance and the magnetic field components are not influenced by a nearby dielectric. From the measurements it is impossible to split up the resistance into a part from the radiation and a part representing the dielectric losses inside the salt pillar.

Radiation patterns of loop antennas attached to the "body" model and some results on pager receiver sensitivity while mounted on the salt pillar will be described at the end of chapter 3.1. However it should be mentioned that it is difficult to summarise the effect of the human body on the radiation pattern. Depending on the frequency of operation the body acts as a director or a reflector. In addition the body can polarize the signal from the ground station in a way that a best possible choice for the orientation of the loop antenna with respect to the body becomes possible.

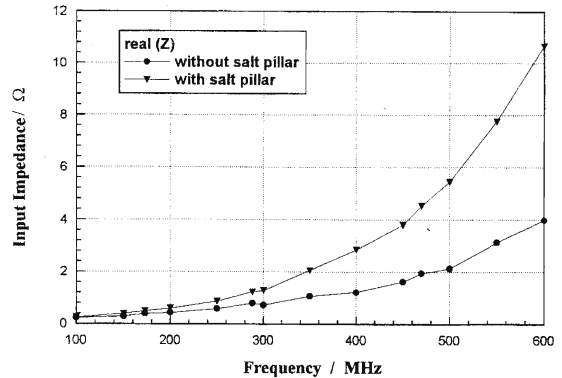


Fig. 1-7 Input resistance of a square loop antenna in free space in comparison with a loop of the same size mounted vertically on a salt pillar; rectangular shaped (25 x 50 mm) single turn loop, wire radius $r = 0.5$ mm (Fig. 1-4), spacing to the salt pillar $d = 2$ mm, loop plane perpendicular to the pillar.

2. APPROXIMATING DESCRIPTION

2.1 Input Impedance

The input impedance is a very important parameter for the design of the antenna. Although available numerical techniques can be used to calculate the input impedance Z_{ant} of a loop antenna, during optimisation approximating formulas are needed to determine the input impedance. The equivalent circuit for the input impedance of a loop antenna is shown in Fig. 2-1.

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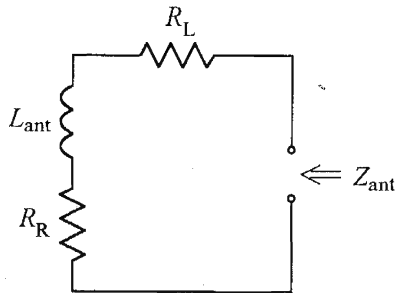


Fig. 2-1 Equivalent circuit for the input impedance of a loop antenna.

2.1.1 Loops with Circular Cross Section Wire

The formulas used to calculate all antenna parameters have been implemented in the PALOMA software package. The antenna model comprises outer parameters corresponding to a lossless wire (radiation resistance R_R and antenna inductance L_{ant}) and inner parameters representing losses caused by skin and proximity effects (described by R_L and an additional inductance).

The equations and formulas are based on the physical understanding of all electromagnetic effects related to rectangular loops formed by wires with a circular cross section. The algorithm handles single as well as multiturn loop antennas and supports both corner and centre excitation. All mutual coupling effects between adjacent turns and wire radius effects are included. As mentioned above the main part is based on a physical interpretation of all those effects. Only a few parameters were obtained by curve fitting from results of numerical simulations (using the NEC program).

For the special case of small rectangular loops with an effective wire length $l = 2(a+b)n^2 < 0.1\lambda$, neglecting the influence of the skin effect on the antenna inductance and the effect of centre excitation, the approximating formulas used in PALOMA reduce to:

$$R_R = \frac{31200\Omega(abn)^2}{\left[\lambda^2 \cos\left(2\pi \frac{n(a+b)}{\lambda}\right)\right]^2} \quad \text{Eq. 2-1}$$

and

$$L_{ant} = \frac{\mu_0 n}{\pi} \left(1 + 0.1 \left(\frac{b}{a}\right)^{-0.25}\right)^{-\left(1 + \frac{8r}{a}\right)^2} \frac{\left(a \operatorname{arccosh}\left(\frac{b}{2r}\right) + b \operatorname{arccosh}\left(\frac{a}{2r}\right)\right)}{\cos\left(2\pi \frac{n(a+b)}{\lambda}\right)} \quad \text{Eq. 2-2}$$

where R_R is the radiation resistance, L_{ant} the antenna inductance, a and b are the side lengths (with $b \geq a$), n is the number of loop turns made from a wire with radius r , and λ is the wavelength.

2.1.2 Strip Antennas

The approximating formulas defined by Eqs. 2.1 and 2.2 are related to wires of circular cross section with radius r . As far as the impedance characteristics and radiation patterns are concerned, a thin strip is equivalent to a cylindrical wire with an equivalent radius r_{eq} . The equivalent radius of many simply shaped cross sections can be found by the method of conformal mapping. The mapping for a wire with rectangular cross section is displayed graphically in Fig. 2-2.

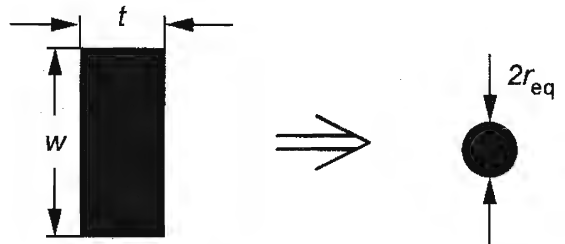


Fig. 2-2 Mapping of a rectangular onto a circular cross section of equivalent radius r_{eq} . Note: drawing not to scale.

The equivalent radius r_{eq} can be calculated as follows.

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$$r_{eq} = \frac{w}{4} \left\{ 1 + \frac{t}{\pi w} \left[1 + \ln \left(\frac{4\pi w}{t} \right) \right] \right\} \quad \text{Eq. 2-3}$$

2.1.3 SLMW Antennas

In order to minimize the antenna losses a sophisticated concept of a special antenna will be discussed in Section 4.4.1. This antenna type shall be referred to as Single Loop Multi Wire (abbreviated SLMW) throughout this document.

As shown in Fig 4.22 the rectangular strip of a single turn loop may be replaced by a number of parallel cylindrical wires. In that case it is possible to interpret the parallel wires as a solid metal strip. This is demonstrated in Fig. 2-3. Now Eq.2.3 again can be used to calculate the equivalent radius r_{eq} .

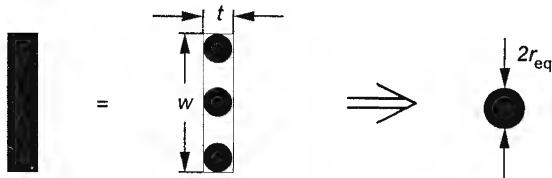


Fig. 2-3 Mapping of a SLMW structure onto a cylindrical section of equivalent radius r_{eq} . Note: drawing not to scale.

2.1.4 Single Turn Loops

Input impedances of perfectly conducting single loop antennas are shown in Fig. 2-4 as a function of frequency. For this analysis all antennas have the same loop area $a \times b = 2500 \text{ mm}^2$.

Starting with a square shape of dimensions $a = b = 50 \text{ mm}$, the ratio of b/a has been varied from a factor 1 to 5. The resonance frequency decreases from $f_{res} = 750 \text{ MHz}$ for a perimeter length $l = 200 \text{ mm}$ to a value of $f_{res} = 560 \text{ MHz}$ for $l = 268 \text{ mm}$. Note that the presence of a conducting plane or PCB (printed circuit board) causes f_{res} to decrease even more.

Depending on the excitation source location different impedances can be obtained.

Corner excited loops show slightly higher values for the external inductance, which may become important during the design of the antenna matching network. As can be expected from the loop geometries, results for corner excitation and for centre excitation at the shorter side become very similar with increasing values of b/a .

Because of skin effect losses in the wire due to non-ideal metallization the efficiency of loop antennas is generally small. Therefore improvement of the radiation resistance R_r may result in better efficiency. This leads to a requirement for loop areas which are as large as possible. For a constant loop area variation of the ratio $b/a > 1$ directly leads to a larger perimeter, which in turn gives higher values for the resistance R_r . Depending on the wire radius an optimal choice for the rectangular shape becomes possible.

2.1.5 Multi-Turn Loops

For the multi-turn structures shown in Fig. 2-5 the axial distance d between successive turns is varied in three steps: $d = 10, 5$ and 2 mm . The first resonance changes to lower values for decreasing distances d . This effect can be explained by the increasing electromagnetic coupling between the turns which gives rise to a capacitive effect. This capacitance may be assumed to be parallel to Z_{ant} in Fig. 2-1.

In order to give a very simple model for multi-turn loops the mutual coupling effects have been incorporated in the inductive part of the formulas implemented in PALOMA. As can be seen from the following figures there is good agreement between results from the approximation formulas and the numerical simulations using the NEC program, up to the first resonance.

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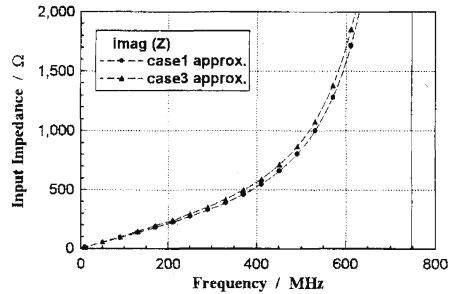
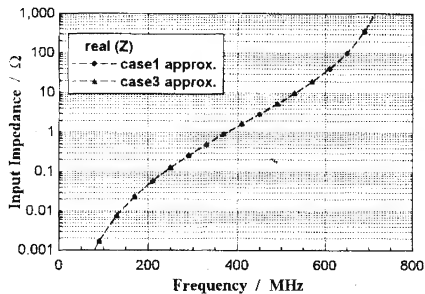
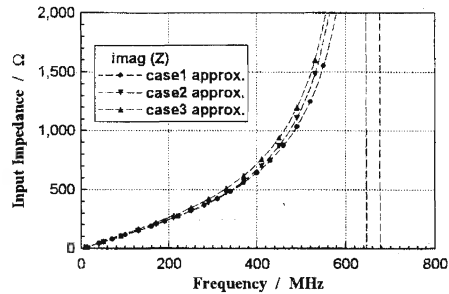
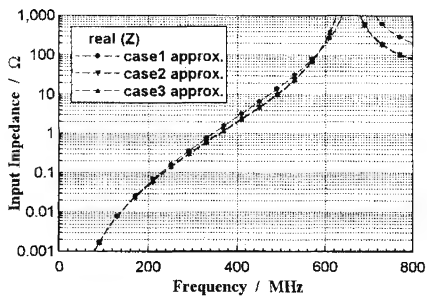
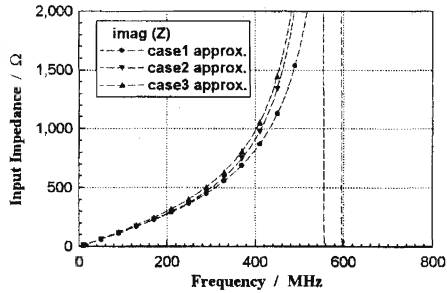
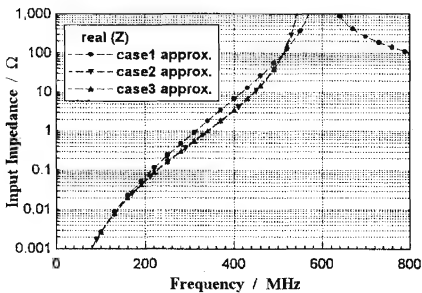
a) $b/a = 1$, $a = b = 50$ mmb) $b/a = 3$, $a = 28.9$ mm, $b = 86.6$ mmc) $b/a = 5$, $a = 22.4$ mm, $b = 111.8$ mm

Fig. 2-4 Calculated input impedance of a rectangular shaped single turn loop antenna as a function of frequency; wire radius $r = 0.5$ mm. Left: input resistance. Right: input reactance.

Case 1: centre excitation at the longer side.
Case 2: centre excitation at the shorter side.
Case 3: corner excitation.

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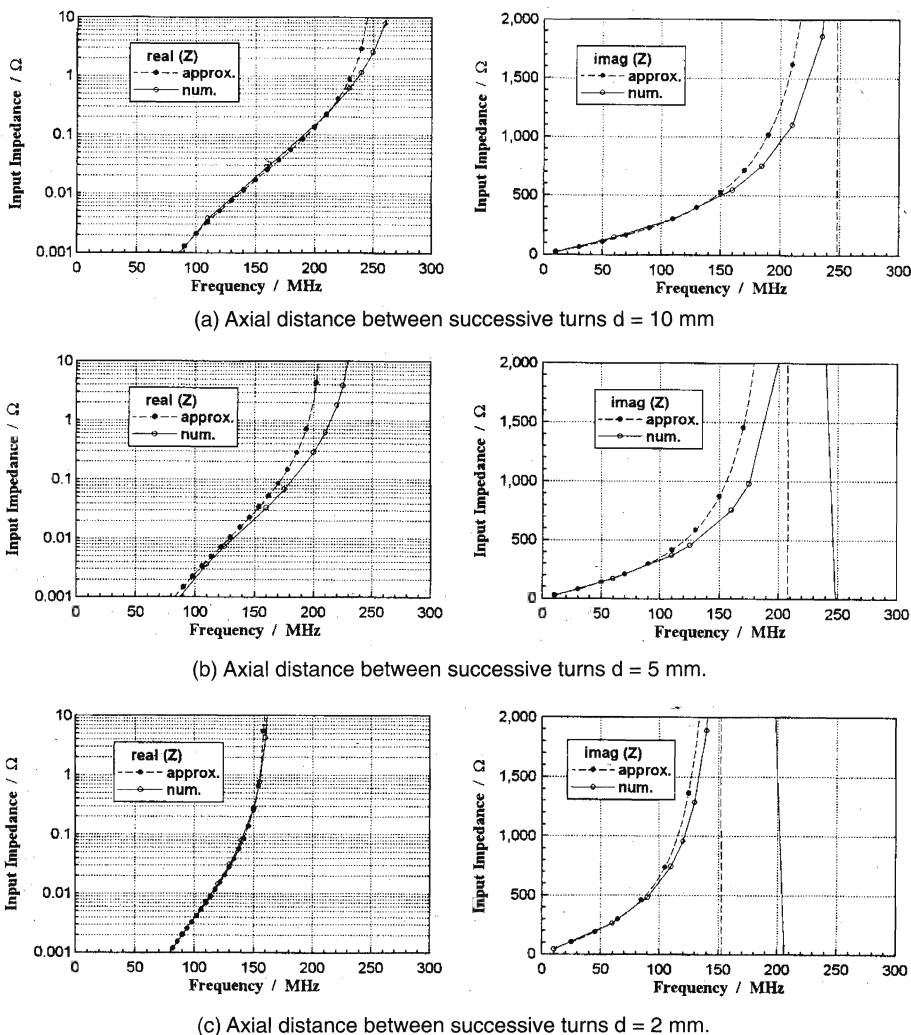


Fig. 2-5 Calculated input impedance of a 4-turn rectangular shaped loop antenna as a function of frequency;
 $b/a = 5$, $a = 10$ mm, $b = 50$ mm, wire radius $r = 0.5$ mm.
 Varied: axial distance between successive turns:
 $d = 10$ mm, 5 mm and 2 mm.

Left : Input resistance.
 Right : Input reactance.
 Num. : Numerical simulation results using the NEC program.
 Approx.: Results using the approximating formulas.

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2.2 Wire Losses due to Skin Effect

Skin effect may cause a large change in the resistance R_L of the conductor, since it effectively reduces the cross section area of the current path. If the frequency increases to infinity, so does the resistance. At any given frequency, a cylindrical conductor may be regarded as a tube whose outer diameter is that of the wire and whose thickness is directly related to the effective penetration depth of the current into the conductor.

2.2.1 Loop Wire with Circular Cross Section

For a cylindrical conductor with specific conductivity σ , after introducing the skin depth δ , the ratio x and the resistance R_{DC} :

$$\delta = \frac{1}{\sqrt{\pi f \mu \kappa}}, \quad x = \frac{r}{2\delta} \quad R_{DC, cyl} = \frac{2n(a+b)}{\kappa \pi r^2} \quad \text{Eq. 2-4}$$

R_L can be given approximately by the following simple expressions

$$\frac{R_{L, cyl}}{R_{DC, cyl}} = \begin{cases} 1 + \frac{1}{3}x^4 & \text{for } x < 1 \\ x + \frac{1}{4} + \frac{3}{64}x^{-1} & \text{for } x > 1 \end{cases} \quad \text{Eq. 2-5}$$

Furthermore, in PALOMA a small additional inductance L_L due to the skin effect is taken into account. The dependence of these two variables (R_L and L_L) on x from Eq. 2.4 is shown in Fig. 2-6 in terms of impedance ratios.

2.2.2 Loop Wire with Rectangular Cross Section

For wires with a rectangular cross section a very simple expression for the internal impedance can be obtained. Based on the geometrical definitions in Fig. 2-2 and assuming $w > t$ without losing generality, the internal resistance is defined for skin depths d while keeping $\delta \ll t$ by.

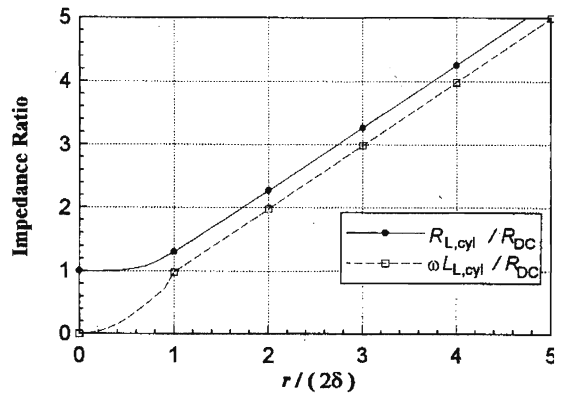


Fig. 2-6 Internal impedance per unit length of a cylindrical wire as a function of $x = r / (2\delta)$ with wire radius r and skin depth δ .

$$R_{DC, rec} = \frac{2n(a+b)}{\kappa wt} \quad \text{Eq. 2-6}$$

with .

$$\frac{R_{L, rec}}{R_{DC, rec}} = K_{skin} \frac{wt}{2\sqrt{2}wt} \sqrt{\omega \mu \kappa} \quad \text{Eq. 2-7}$$

The correction factor K_{skin} is illustrated in Fig. 2-7.

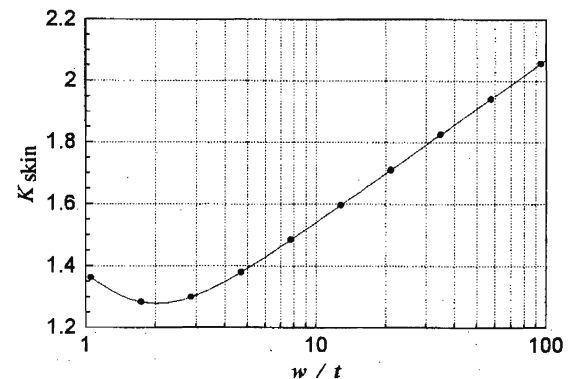


Fig. 2-7 The parameter K_{skin} as a function of the dimensions of the cross section.

2.2.3 Proximity Effect In Multi-Loop Antennas

For multi-loop or SLMW antennas, the current distribution in each loop is affected by the magnetic flux produced by the adjacent loops, as well as by the magnetic flux produced by itself. This effect causes the loss resistance of such structures to be higher than the value calculated with the above equations. This loss increase is expressed by the proximity factor F_p , which is also included in PALOMA.

3. EXPERIMENTAL ANALYSIS

3.1 Impedance of Loop Antennas

3.1.1 Measurement Technique

The impedance measurement of antennas is straightforward using a network analyser with calibration technique. Measuring the real part of the impedance of pager loop antennas is a much more difficult problem. Since theoretical study shows that loop antennas for pager applications have a high quality factor Q , the results of the impedance measurements are very sensitive to losses caused by the measurement set-up and the antenna connections. Best results were achieved using an image plane and measuring only one half of a loop (see Fig. 3-1). The antenna can be fed directly by means of a coaxial cable. The impedance of a full loop antenna is given as twice the measured impedance for the half loop.

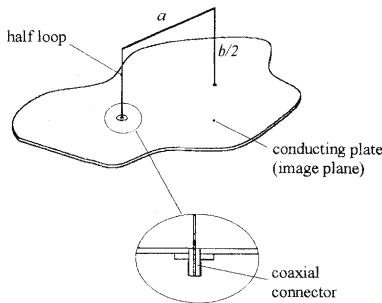


Fig. 3-1 Image plane technique used to measure the input impedance of loop antennas.

3.1.2 Fundamental Impedance Characteristics

Fig. 3-2 and Fig. 3-3 show the measured real and imaginary parts of the input impedance of a rectangular loop antenna and the quality factor Q , defined by.

$$Q = \frac{|\text{Im}(Z)|}{|\text{Re}(Z)|} \tag{Eq. 3-1}$$

The loop inductance found shows good agreement with the theory. The agreement is much less for the real part of the impedance. Since pager loop antennas have a very high Q , this difference can be explained by external losses in the measurement set-up. Examples are losses in the image plane, losses at the soldering connections to the antenna or secondary radiation at the connector.

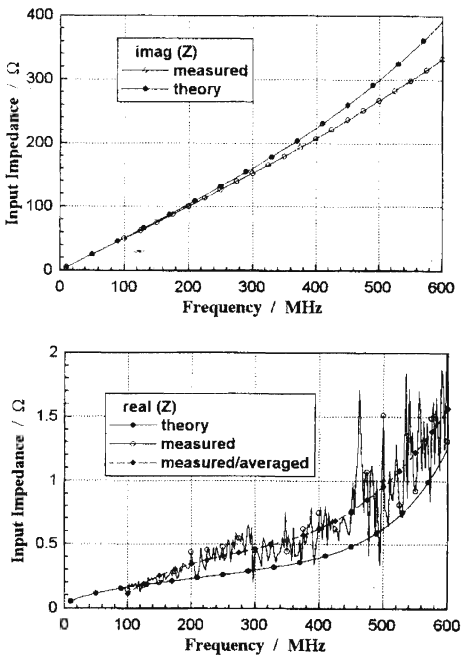


Fig. 3-2 Theoretical and measured input impedance of a rectangular loop antenna (60 x 10 mm loop, wire $r = 0.5$ mm). Left: imaginary part, right: real part.

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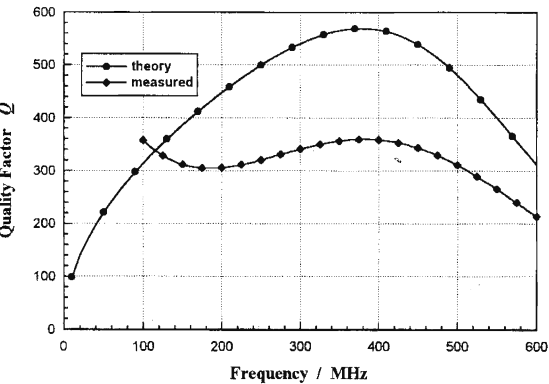


Fig. 3-3 Theoretical and measured quality factor Q of a rectangular loop antenna (60 x 10 mm loop, wire radius r = 0.5 mm).

3.1.3 Different Loop Materials

The loop material is an important cost factor for pagers. As expected different loop materials result in a change of the real part of the input impedance. Fig. 3-4 shows that this change depends not only on the material but also on the diameter of the wire. The different impedances are given in Table 3-1 for some typical pager frequencies.

No great influence can be observed on the imaginary part of the input impedance. However, a larger wire radius gives a smaller inductance in accordance with Eq.2.2. The use of materials like Fe or Ni which show additional magnetic losses is not advised.

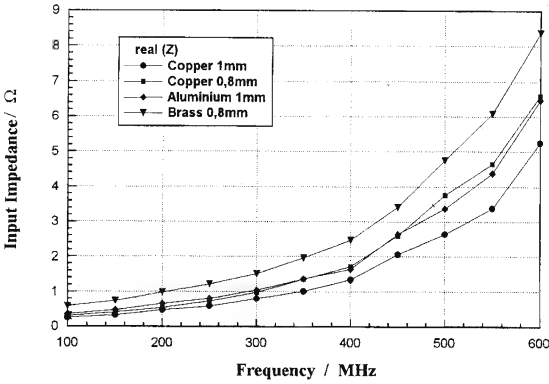


Fig. 3-4 Measured real part of the input impedance of a rectangular loop antenna with different loop materials (50 x 25 mm loop, wire radius r = 0.5 mm)

TABLE 3-1 Input Impedance for Different Loops

Material	f=173MHz		f=288MHz		f=470MHz	
	R_{in}/Ω	$\omega L_{in}/\Omega$	R_{in}/Ω	$\omega L_{in}/\Omega$	R_{in}/Ω	$\omega L_{in}/\Omega$
Copper 1mm	0.376	117	0.791	204	2.508	377
Copper 0.8mm	0.462	128	0.838	223	3.336	416
Silver 1mm	0.465	116	1.192	196	2.078	345
Aluminium 1mm	0.520	119	0.963	207	3.118	384
Brass 0.8mm	0.829	129	1.447	224	4.274	416

Rectangular loop (50 x 25 mm, wire radius 0.5 mm)

3.1.4 Loop Antennas Over Board

The normal application for loop antennas is the use over or near a PCB (printed circuit board). The theoretical analysis in Section 1.2 has shown, that an important change of the loop impedance can be expected when the loop is mounted parallel to a board. For smaller distances between the antenna and a conducting layer the loop inductance becomes smaller and the losses (R_L) higher.

For higher frequencies the change of the radiation resistance R_R dominates the opposite change in losses. This results in a minimum of the real part of the impedance for 5 mm board distance and a frequency of 470 MHz, as shown in Fig. 3-5.

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The conducting board from Fig. 3-5 consisted of a fully metallized PCB board with the conducting side facing the loop antenna. For the frequencies used this is equivalent to an all-metal plate.

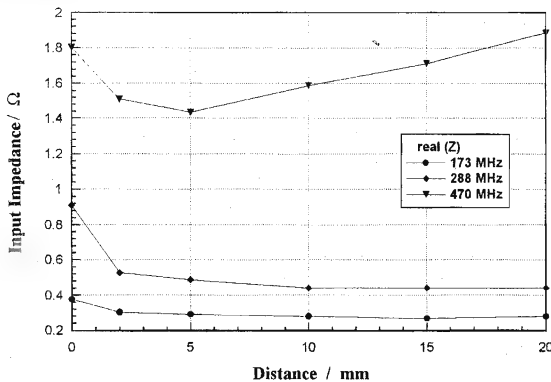


Fig. 3-5 Measured real part of the input impedance of a rectangular loop antenna over a conducting board, for typical pager frequencies (50 x 25 mm loop, wire radius $r = 0.5$ mm).

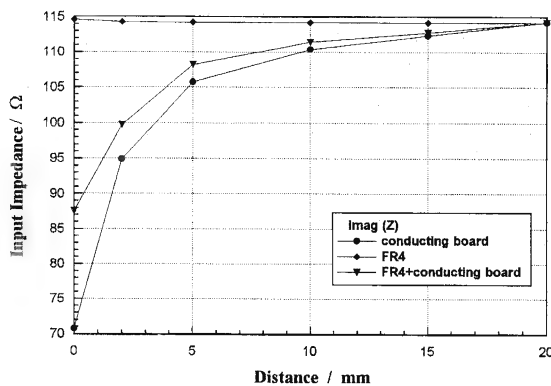


Fig. 3-6 Measured imaginary part of the input impedance of a rectangular loop antenna over a PCB board for different board materials (50 x 25 mm loop, wire radius $r = 0.5$ mm, $f = 173$ MHz).

From the point of view of the pager design it is very important to know the influence of the board material on the losses of the loop antenna. Fig. 3-6 shows the change of the loop impedance for different board materials. Here FR4+conducting board (FR4 is the standard substrate for PCBs) means PCB board, metallized on one side, the conducting side facing away from the loop. The increase of the loop losses is caused by the presence of a conducting board close to the antenna and is not due to dielectric losses in the PCB. A comparison of different board metallizations shows only a small effect on the antenna losses.

3.1.5 Loop Antenna on a Salt Pillar

The most realistic case of impedance characterisation of a pager loop antenna is the measurement on a salt pillar. This shows the influence of a simulated human body on the impedance of loop antennas. The salt pillar used for these measurements was based on German PTT regulations for pager tests. The salt pillar has a height of 1.7 m and a diameter of 0.3 m. It is a dielectric cylinder containing a salt water solution with a concentration of 1.49 g NaCl per litre.

Problems arise when trying to use the image plane technique for impedance measurements near the salt pillar. The image plane can only be realized on one side of the antenna because it is necessary to bring the antenna as close as possible to the salt pillar. This is why the results cannot be compared to the measurements using a full image plane but only show the relative change due to the salt pillar.

The impedance characteristics given in Fig. 3-7 and Fig. 3-8 show a comparison between a 50 x 25 mm loop antenna on the pillar with and without salt water inside. Since water can be regarded as a lossy dielectric, the influence of the body can only be seen in the real part of the input impedance. The characteristics show two to three times higher losses of the loop at UHF frequencies due to the presence of the salt pillar.

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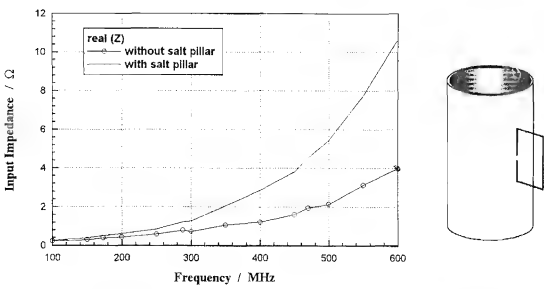


Fig. 3-7 Measured real part of the input impedance of rectangular loop antenna (50 x 25 mm loop, wire radius $r = 0.5$ mm) vertically mounted on a salt pillar, with the antenna plane perpendicular to the salt pillar surface.

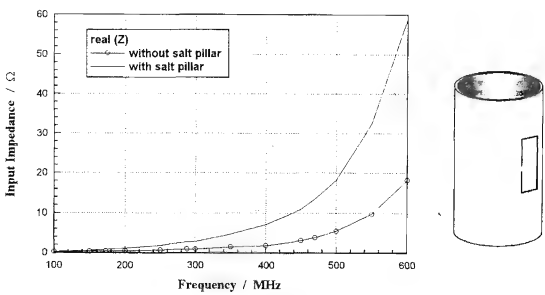


Fig. 3-8 Measured real part of the input impedance of rectangular loop antenna (50 x 25 mm loop, wire radius $r = 0.5$ mm) mounted flat on a salt pillar, with the antenna plane parallel to the salt pillar surface.

The characteristic of Fig. 3-7 was measured with the loop mounted in a vertical position, while for Fig. 3-8 the loop was mounted in a flat position. A comparison of the measured impedances in Table 3-2 shows, that the losses due to the salt pillar are somewhat higher for the flat position.

$f=8173$ MHz				$f=288$ MHz		$f=470$ MHz	
Position		R_{mea}/Ω	vL_{mea}/Ω	R_{mea}/Ω	vL_{mea}/Ω	R_{mea}/Ω	vL_{mea}/Ω
vertical	without salt pillar	0.3932	116.60	0.7954	201.35	1.9657	366.49
	with salt pillar	0.5026	116.32	1.2330	201.43	4.5437	368.27
flat	without salt pillar	0.4048	119.44	0.8970	206.99	3.8417	381.93
	with salt pillar	0.8228	119.75	2.6548	208.35	13.6077	387.53

TABLE 3-2 Input Impedance on a Salt Pillar

Rectangular loop (50 x 25 mm, wire radius $r = 0,5$ mm)

3.2 Sensitivity Measurement

The sensitivity measurements were carried out with Philips UAA2080T pager receiver demonstration boards at the frequencies 172.941 MHz, 288.234 MHz and 469.950 MHz.

After removing the 50 Ω -connector and the matching network an extra PCB was used to realise the loop antenna and the antenna matching network. Small wires were soldered to contact the additional PCB to the pager demonstration board.

A BER (Bit Error Rate) measurement system from Philips was used to measure the bit error rate for a defined field strength. The sensitivity of the pager board was defined as the measured field strength for a 3% bit error rate. For all measurements the digital filter on the BER-board was used. This digital filter corresponds with the one built into the Philips pager decoders and improves the sensitivity.

Two forms of measurements were used to characterize the sensitivity of different antenna structures and matching networks:

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1. The free space sensitivity measurement was carried out in a strip-line cell (so-called "TEM cell"). The dimensions of the homogenous field were 20 cm x 20 cm x 20 cm. To obtain optimum coupling with the magnetic field inside the cell the loop was aligned as shown in Fig. 3-9.
2. At the salt pillar the sensitivity was measured in an outdoor range because of the large dimension of the salt pillar. A stepper positioner was used to turn the salt pillar to the 8 positions necessary for the standard sensitivity tests of pagers.

The field inside the strip-line cell and in the outdoor range was calibrated relative to the input power using a calibrated H-field sensor and a spectrum analyser. Results of sensitivity measurements in the TEM cell are given in Section 4.4.1 and Section 4.5.

The following pages show the sensitivity of the pager board on a salt pillar for different antenna positions and measurement angles to the salt pillar. Fig. 3-10 shows for $f = 173$ MHz typical far-field sensitivity characteristics of a loop antenna in horizontal and flat position relative to the pillar. To obtain an easy graphical representation the sensitivity has been plotted as negative values: a large

circle now corresponds to a high sensitivity. The sensitivity in dB $\mu\text{V}/\text{m}$ can be read from the graph by disregarding the sign of the plotted values. A significant rise and change in shape of the sensitivity characteristic can be observed for a vertical orientation of the loop. This vertical orientation seems to be the optimum orientation of the loop relative to the salt pillar for achieving the highest pager sensitivity.

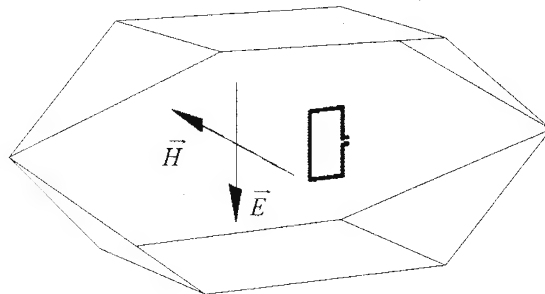
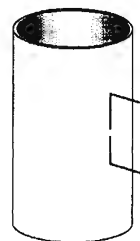
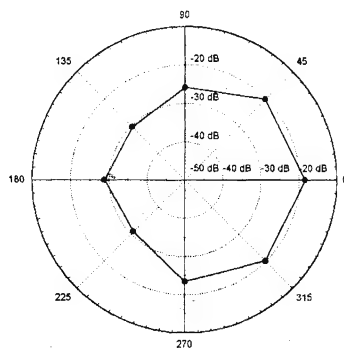


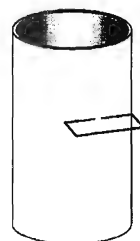
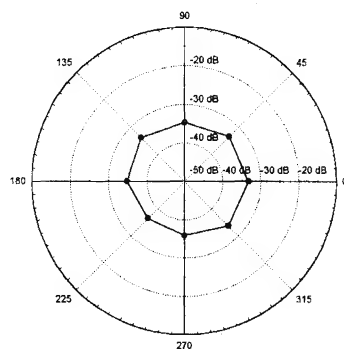
Fig. 3-9 Antenna position relative to the field polarisation in the TEM cell.

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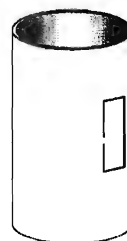
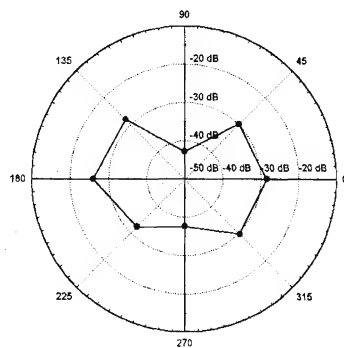
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vertical mounting



horizontal mounting



flat mounting

Fig. 3-10 Sensitivity characteristic of a rectangular loop antenna for different positions on a salt pillar. To find the sensitivity in dB $\mu\text{V/m}$ disregard the negative sign (50 x 25 mm loop, wire radius $r = 0.5$ mm, $f = 172.941$ MHz).

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4. SYSTEM ASPECTS

4.1 Antenna Noise Figure and LNA Noise Properties

The network topology of a low-noise receiver system with a loop antenna and a noise matching network (NMN) is shown in Fig. 4-1. The equivalent circuit for a loop antenna consists of a generator with an internal resistance R_R describing the power dissipation due to radiation, an inductance L_{ant} and a resistance R_L describing the losses (AL: antenna losses) in the antenna which are mainly caused by the skin effect. The LNA is the balanced RF amplifier of the UAA2080 pager receiver.

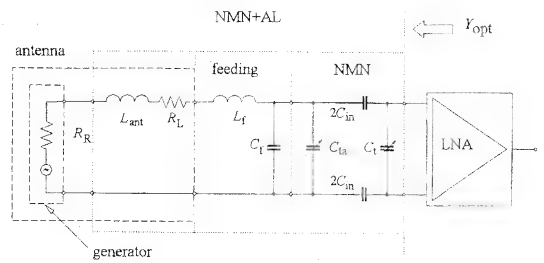


Fig. 4-1 The network topology

Some examples of the dependency of these elements on the loop area are shown in Fig. 4-2 to Fig. 4-10. The inductance L_{ant} as well as the resistance R_R increase with the loop area. High values for R_R improve the antenna efficiency and also the antenna noise figure F_{ant}

$$F_{ant} = 1 + \frac{R_L \cdot T}{R_R \cdot 290 K} \quad , \quad \text{Eq. 4-1}$$

where T is the ambient temperature. The advantage of high R_R values is combined with the disadvantage of large L_{ant} which might require very small and impractical values for capacitors C_{in} or C_{la} . For noise or gain matching the admittance Y of the NMN+AL must be equal to Y_{opt} seen by the LNA. Fig. 4-11 shows the dependence of the optimum admittance on the resistance R_e (R_e is determining the overall current of the LNA). The corresponding normalised noise resistance R_n and minimum noise figure F_{min} of the LNA is given in Fig. 4-12. In case of $R_e = 330 \Omega$ it is:

f / MHz	Real(Y_{opt_Fmin})	Real(Y_{opt_Gmax})	Imag(Y_{opt_Fmin})	Imag(Y_{opt_Gmax})
173	0.556 mS	0.169 mS	-0.413 mS	-0.684 mS
288	0.587 mS	0.216 mS	-0.687 mS	-1.139 mS
470	0.665 mS	0.340 mS	-1.121 mS	-1.859 mS

Tab. 4.1 Optimum LNA Matching Admittance (Noise and Power)

The subscript "opt_Fmin" refers to the minimal noise figure and "opt_Gmax" stands for maximum gain of the LNA.

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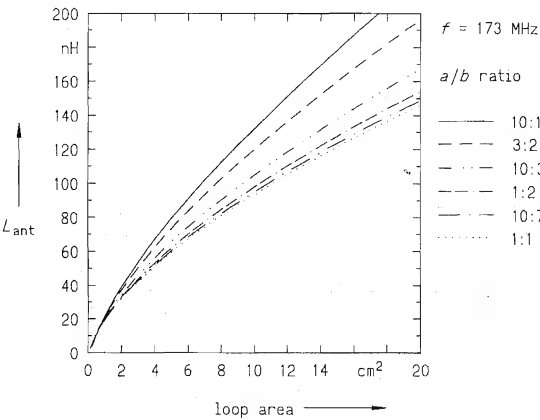


Fig. 4-2 Inductance of a single loop at $f = 173\text{ MHz}$.

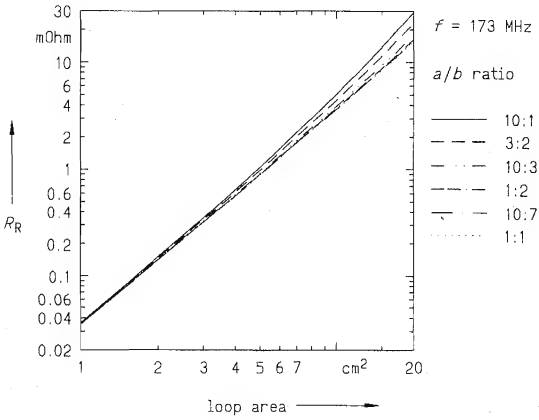


Fig. 4-3 Radiation resistance of a single loop at $f = 173\text{ MHz}$.

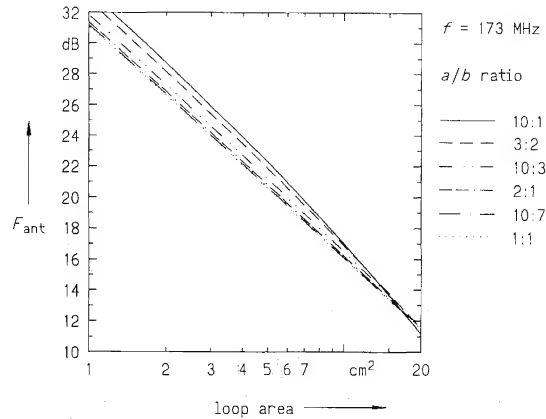


Fig. 4-4 Antenna noise figure of a single loop at $f = 173\text{ MHz}$.

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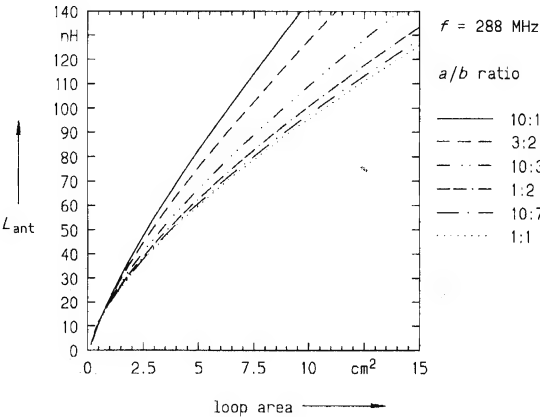


Fig. 4-5 Inductance of a single loop at $f = 288$ MHz.

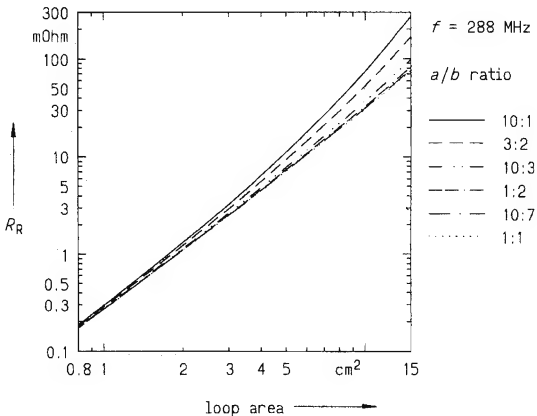


Fig. 4-6 Radiation resistance of a single loop at $f = 288$ MHz.

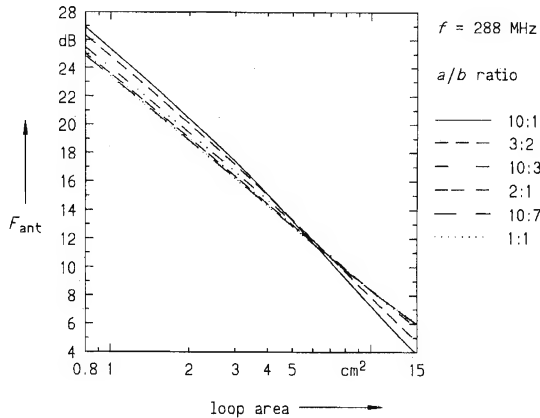


Fig. 4-7 Antenna noise figure of a single loop at $f = 288$ MHz.

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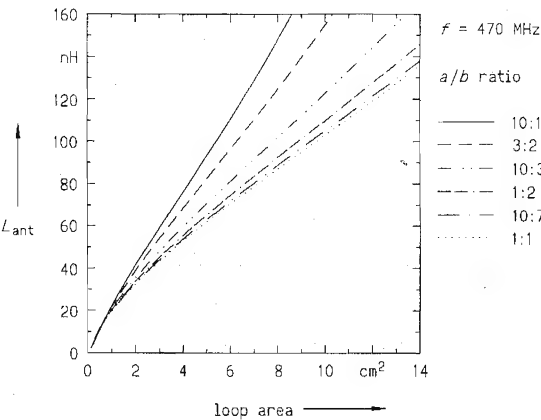


Fig. 4-8 Inductance of a single loop at $f = 470$ MHz.

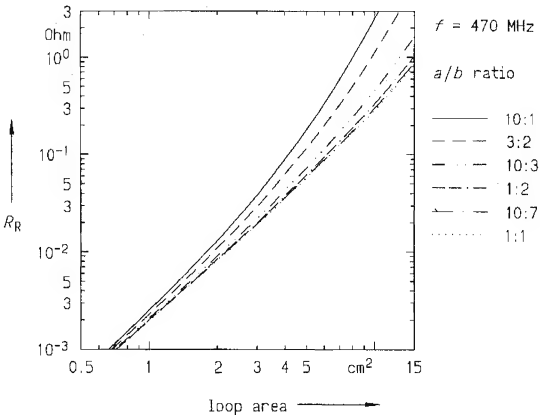


Fig. 4-9 Radiation resistance for a single loop at $f = 470$ MHz.

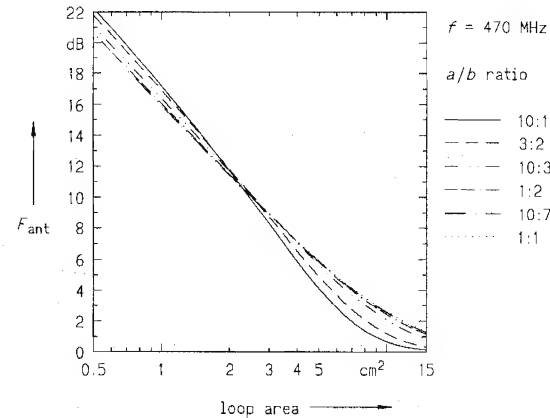


Fig. 4-10 Antenna noise figure of a single loop at $f = 470$ MHz.

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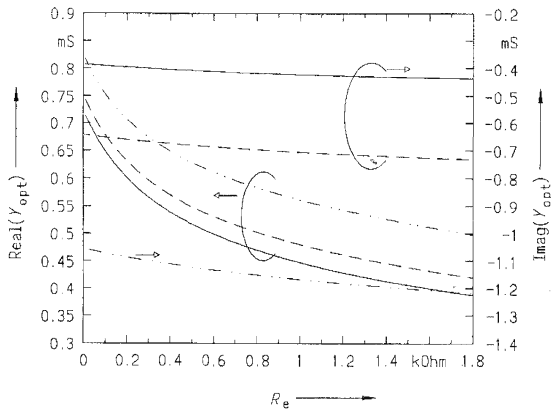


Fig. 4-11 The optimum NMN output admittance seen by the LNA to achieve the minimum noise figure F_{\min} . Solid line: $f = 470$ MHz, dashed line: $f = 288$ MHz and dot-dashed line: $f = 173$ MHz.

4.2 Pager Sensitivity

The signal-to-noise ratio at the input of the demodulator is responsible for the bit error rate of the digital output. For a bit error rate of 3% a S/N ratio of at least 1 dB at the input of the demodulator is required. In fact we have

$$\frac{S}{N} = \frac{S_{\text{in}}}{N_{\text{in}}} F_{\text{system_TA}}, \quad \text{Eq. 4-2}$$

describing the pager from the antenna to the demodulator input, with S_{in} representing the input signal power. The input noise power N_{in} at the antenna with the bandwidth Δf and the antenna radiation resistance R_{p} is

$$N_{\text{in}} = k \cdot T_{\text{A}} \cdot R_{\text{p}} \cdot \Delta f. \quad \text{Eq. 4-3}$$

This noise power as well as the noise factor $F_{\text{system_TA}}$ are dependent on the antenna noise temperature T_{A} . This is due to the fact, that the noise figure is defined for a generator temperature of 290 K, whereas the antenna acts as a generator with a strongly frequency dependent temperature.

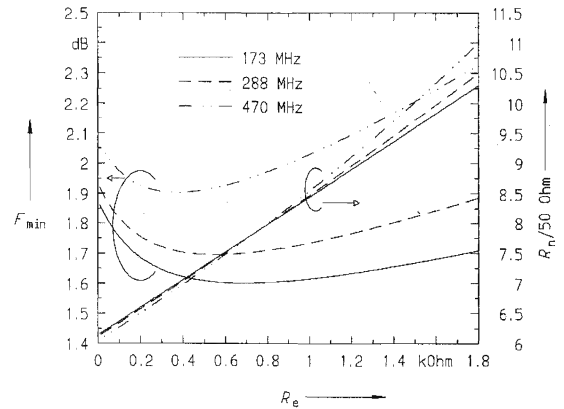


Fig. 4-12 The LNA minimum noise figure F_{\min} and the noise resistance R_{n} .

T_{A} is influenced by the environmental properties of the outer space. In Fig. 4-13 its variation and frequency dependency are shown. The minimum value may be obtained for an elevation angle of 90° during the night, whereas the other line (labelled 'max') indicates the more realistic situation in a pager, when the antenna is able to "see" the horizon. Furthermore the warm earth and the sun create additional noise. The antenna noise temperature varies approximately as:

$$T_{\text{A}} = 1.32 \left(\frac{1 \text{ GHz}}{f} \right)^{2.5} \quad \text{Eq. 4-4}$$

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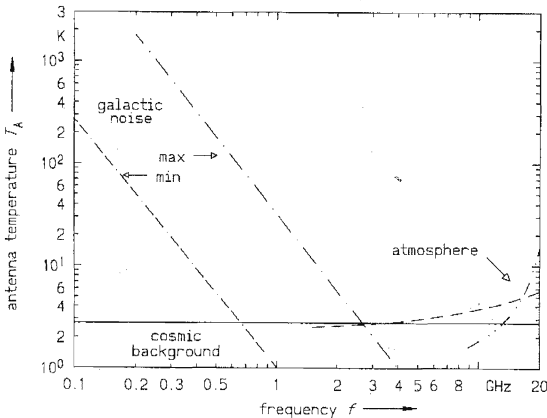


Fig. 4-13 The antenna noise temperature versus frequency due to environment.

The system noise factor F_{system} depends on the losses in the noise matching network NMN+AL, the LNA and the post-LNA network. In our consideration the NMN+AL network includes the antenna losses which are mainly caused by the skin effect. Since the source (the antenna) is not at the temperature of 290 K, we have to transform the noise figure using.

$$F_{\text{system_TA}} = 1 + (F_{\text{system}} - 1) \frac{290K}{T_A}. \quad \text{Eq. 4-5}$$

In order to discuss the influence of the different parts of the overall system, we have to look at the following relation.

$$F_{\text{system}} = F_{\text{NMN+AL}} + \frac{F_{\text{LNA}} - 1}{G_{\text{NMN+AL}}} + \frac{F_{\text{post_LNA}} - 1}{G_{\text{LNA}} \cdot G_{\text{NMN+AL}}}. \quad \text{Eq. 4-6}$$

By using these equations, it is possible to determine the minimum signal power S which is necessary to realize a signal to noise ratio S/N equal to 1 dB at the end of the receiver (call success rate = 80%). The next figures show S_{in} and the sensitivity E_{sens} of the pager versus the losses in the NMN+AL network. This calculation is useful, because the properties of the first stage of the

system are important with respect to the system noise figure. The relation between the effective electric field strength E_{sens} at a lossless antenna and the power S_{in} is

$$E_{\text{sens}} = \sqrt{\frac{Z_0 \cdot S_{\text{in}} \cdot C_{\text{corr}}}{\frac{1.5}{4\pi} \lambda^2}} \quad \text{with} \quad C_{\text{corr}} = \frac{R_R}{R_{\text{small}}}. \quad \text{Eq. 4-7}$$

In this formula R_R is the radiation resistance resulting from Eq. 2-1, while R_{small} is the radiation resistance for very small antennas, calculated as follows:

$$R_{\text{small}} = \begin{cases} 1.8850 \cdot 10^{-3} \left(\frac{sn}{\text{cm}^2} \right)^2 \Omega \\ 0.2657 \cdot 10^{-3} \left(\frac{sn}{\text{cm}^2} \right)^2 \Omega \\ 0.0346 \cdot 10^{-3} \left(\frac{sn}{\text{cm}^2} \right)^2 \Omega \end{cases} \quad \text{Eq. 4-8}$$

with $s=a \cdot b$ representing the loop area in cm^2 and n the number of turns (for multi-loops).

The relation between E_{sens} and S_{in} becomes geometrically independent for very small antennas, i.e. $R_R = R_{\text{small}}$. Very small antennas have an effective wire length $l = 2 \cdot (a+b) \cdot n^2 \leq 0.05 \lambda$. In that case it is possible to give a relation between the pager sensitivity E_{sens} and the losses and noise figure of the noise matching network NMN+AL including the losses in the antenna, as shown in Fig. 4-1.

For these calculations it was assumed that the output impedance of the NMN network is the optimum choice with respect to the maximum gain of the LNA with $F_{\text{NMN+AL}} = 1/G_{\text{NMN+AL}}$, which is valid only for matched networks. In general, the noise figure and the gain of the LNA depend on the noise matching network.

In Fig. 4.14 to 4.19 some calculations have been performed for a minimum S/N -ratio of 1 dB as a function of antenna temperature and frequency. For the calculations see Section 4.2.1.

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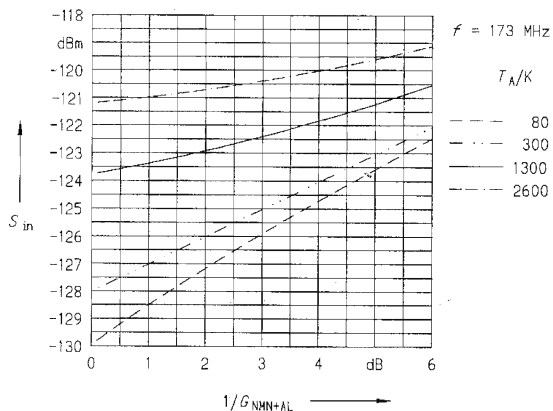


Fig. 4-14 The minimum input signal power in order to realise $S/N \geq 1$ dB for different antenna temperatures at $f = 173$ MHz.

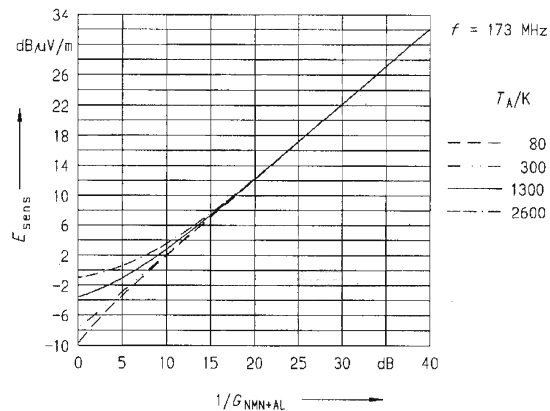


Fig. 4-15 The minimum electric field at the antenna in order to realise $S/N \geq 1$ dB for different antenna temperatures at $f = 173$ MHz.

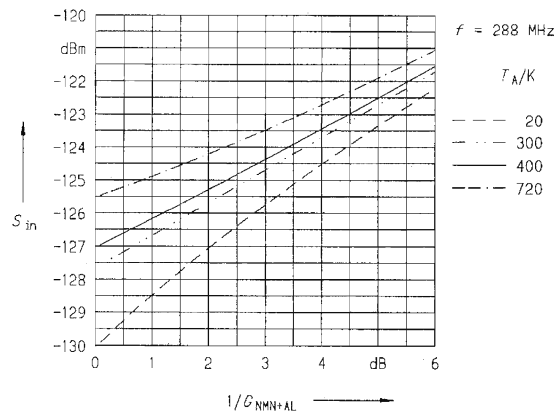


Fig. 4-16 The minimum input signal power in order to realise $S/N \geq 1$ dB for different antenna temperatures at $f = 288$ MHz.

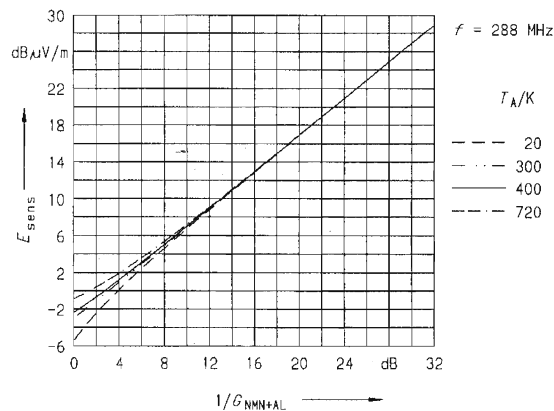


Fig. 4-17 The minimum electric field at the antenna in order to realise $S/N \geq 1$ dB for different antenna temperatures at $f = 288$ MHz.

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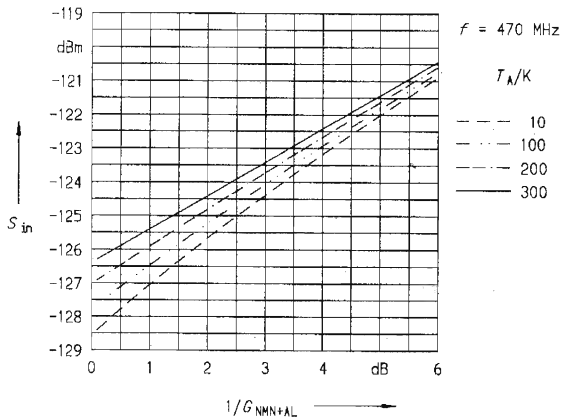


Fig. 4-18 The minimum input signal power in order to realise $S/N \geq 1$ dB for different antenna temperatures at $f = 470$ MHz.

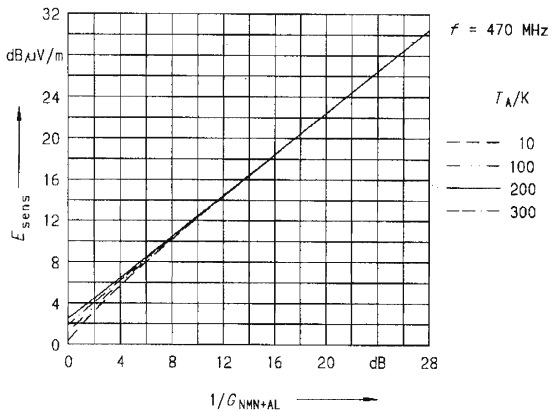


Fig. 4-19 The minimum electric field at the antenna in order to realise $S/N \geq 1$ dB for different antenna temperatures at $f = 470$ MHz.

4.2.1 Pager Sensitivity Calculation Procedure

In general, determining the pager sensitivity using Eq. 4-6 requires the knowledge of losses in the antenna, in the NMN, matching conditions between antenna and NMN as well as between LNA and NMN. In order to avoid large

effort in calculation the following approximation may be used:

1. Calculate the losses of the NMN+AL network and set $F_{\min} = 1 / G_{\text{NMN+AL}}$. In case of $C_{\text{is}}=0$ the following approximation holds (where T is the ambient temperature and R_{cn} the loss resistance of the non-tuneable capacitors in the NMN, see Fig. 4-20).

$$1/G_{\text{NMN+AL}} = F_{\text{NMN+AL}} = 1 + \frac{(R_L + 2R_{\text{cn}}) \cdot T}{R_R \cdot 290 \text{ K}} \quad \text{Eq. 4-9}$$

2. Extract from Fig. 4-15, Fig. 4-17 and Fig. 4-19 the pager sensitivity E_{sens} for small loops.
3. Calculate the correction factor from Eq. 4-7, using R_R from Eq. 2-1 and R_{small} from Eq. 4-8.
4. Add this correction (in dB) to the E_{sens} value obtained in step 2.

4.3 Input Noise Matching Network

The noise figure of the NMN+AL network depends on losses in the antenna. R_L describes those losses which are mainly due to the skin effect. Further losses exist due to the finite quality of the elements in the input matching network. They are modelled by resistance R_{cn} for non-tuneable capacitors and by R_{ct} for tuneable capacitors (see Fig. 4-20). It was found, that for most SMD capacitors the losses are well-described by a series resistor which is capacitance independent.

It is useful to analyze a noise matching network like the one given in Fig. 4-20. It shows a capacitive transformation of the low radiation resistance R_R to the high input resistance of the LNA. In general an inductive transformation would give higher losses because of the lower quality factors of inductors in comparison with capacitors.

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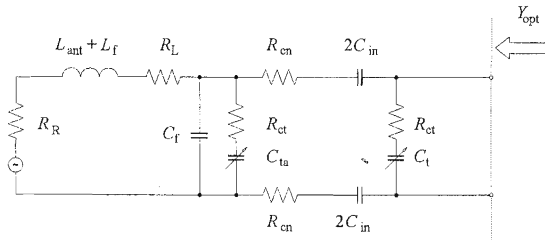


Fig. 4-20 The input noise matching network topology

Noise or gain matching means, that the output admittance Y of the NMN+AL is equal to Y_{opt} (for noise respectively gain) seen by the LNA. With the knowledge of the real part and the imaginary part of Y_{opt} , the antenna data, C_{ta} and the quality factors of the capacitances, it becomes possible to calculate the capacitances C_f and C_{in} forming the NMN. The network does not contain any parasitic board capacitance, so the calculated C_f must be reduced by ≈ 1.5 pF. The presence of an antenna feed (see Ch. 4.3.2) can have a great influence on the matching network optimum values of C_{in} and C_f and must also be taken into account.

4.3.1 Calculation of NMN Elements

In order to calculate the capacitances of the NMN network it is necessary to analyse the topology given in Fig. 4-20. In case of $C_{ta} = 0$, $R_{ct} = 0$ and no antenna feed the following relations with $R_x = R_R + R_L + 2R_{cn}$ can be used to determine C_{in} and C_f ,

$$\left[\operatorname{Re}(Y_{opt_Gmax}) (R_x + \omega^2 L_{ant}^2) \right] \cdot C_{in}^2 - 2 \operatorname{Re}(Y_{opt_Gmax}) \cdot C_{in} + \frac{\operatorname{Re}(Y_{opt_Gmax})}{\omega} = 0, \quad \text{Eq. 4-10}$$

$$C_f = \frac{\operatorname{Im}(Y_{opt_Gmax})}{\omega} - \frac{C_{in} [1 - (\omega^2 C_{in} L_{ant})]}{(\omega C_{in} R_x)^2 + [1 - (\omega^2 C_{in} L_{ant})]^2}. \quad \text{Eq. 4-11}$$

4.3.2 Calculation of Feed Elements

As illustrated in Fig. 4-21 it can sometimes be necessary or useful to have an antenna feed which consists of a two parallel lines with the length l_f and the distance d_f . Especially the capacitance created by such a feed must be taken into account. Using the transmission line formula for round parallel wires in air

$$Z_L = \frac{377 \Omega}{\pi} \ln \left(\frac{d_f}{2r} + \sqrt{\left(\frac{d_f}{2r} \right)^2 - 1} \right), \quad \text{Eq. 4-12}$$

the feeding capacitance C_f and inductance L_f are obtained by

$$C_f = \frac{l_f}{Z_L c_{light}} \quad \text{and} \quad L_f = \frac{l_f Z_L}{c_{light}}. \quad \text{Eq. 4-13}$$

If the feed elements are realised as PCB tracks or using a conductor with a different cross-section from the antenna, C_f and L_f must be corrected accordingly.

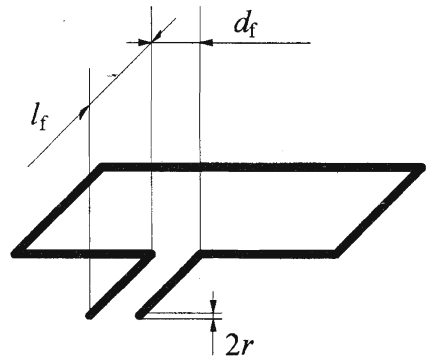


Fig. 4-21 Antenna feed geometry.

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4.4 Antenna Design

4.4.1 Reducing Antenna Losses

Considering the quality of the capacitors used in the NMN network, it is only useful to focus effort on improving antennas when the antenna losses are dominant. When C_{ia} in Fig. 4-20 is zero it makes no sense to reduce the antenna losses R_L when low quality capacitors with $R_{ct} \gg R_L$ are used at the same time (see Eq.4-9).

Furthermore, it is sometimes possible to improve the antenna performance by using surfaces coated with materials of high conductivity. On well-conducting material such as copper coating prevents surface corrosion and contamination.

A comparison of the SLMW antenna with its single-wire counterpart has been made in Table 4-2. It shows a lower loss in terms of a reduced R_L , a lower antenna noise figure and an improved sensitivity by 6 dB for the SLMW

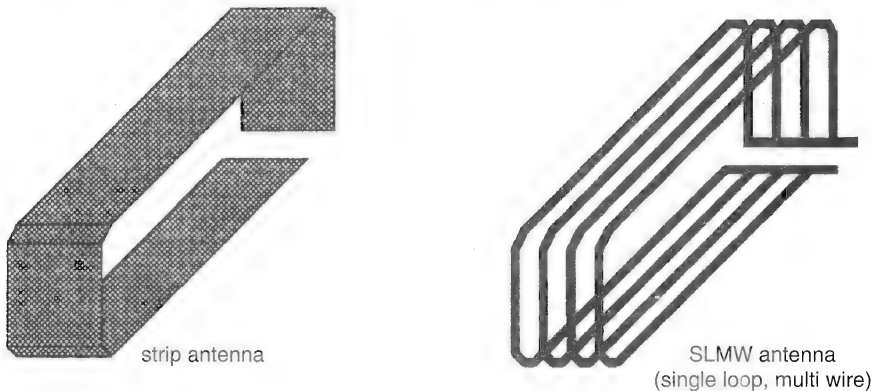


Fig. 4-22 Antennas with reduced skin effect losses

Reducing antenna losses requires a larger surface of the wire metallization in order to lower the skin effect losses. In Fig. 4-22 two possible solutions are shown: a strip antenna and a single loop multi wire (SLMW) antenna. The inductance and radiation resistance of the strip antenna as well as the SLMW-antenna may be calculated using an equivalent wire diameter given by Eq. 2-3. For calculation of the losses refer to Eqs. 2-5 and 2-9.

In general, skin effect losses can be minimized by observing the following guidelines:

- use antennas with smooth surfaces, particularly on the inner side of the loop
- avoid cracks at corners by using a sufficiently large bending radius
- avoid sharp edges in strip material by rounding or sanding

structure, as expected due to the factor 4 in the number of wires. The relatively large deviation between theoretical and measured sensitivity may be caused by the contact resistance (neglected in the theory). This only becomes important when R_L is in the range of some $10^{-3} \Omega$.

In general the SLMW antenna is the best solution for a pager antenna when the most important task is to minimize antenna size. For best sensitivity it makes more sense to choose a larger antenna area and capacitors of high quality.

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Antenna aspects

loop geometry loop type excitation "wire" geometry	feeding geometry	NMN theory	NMN real
L_{ant}	L_f	$2 C_{\text{in}}$	$2 C_{\text{in}}$
R_R		C_t	C_t
R_L	C_f	C_{ta}	C_{ta}
F_{ant}		$1 / G_{\text{NMN+AL}}$	
C_{corr}		E_{sens}	E_{sens}
Receiver frequency $f = 470 \text{ MHz}$			
4 x 0.8 cm SLMW corner excitation 4 parallel wires, radius = 0.5 mm distance = 1.5 mm	8 x 3mm		
35.19 nH 54.62 mΩ 0.051 Ω 2.91 dB 1.51 dB	5.65 nH 0.13 pF	2.20 pF 2.31 pF 1.80 pF 8.9 dB 12.0 dBμV/m	2.20 pF 1.7-3 pF 1.80 pF 17.8 dBμV/m
4 x 0.8 cm single loop corner excitation	5 x 3 mm		
57.66 nH 25.81 mΩ 0.169 Ω 8.91 dB 1.26 dB	3.53 nH 0.08 pF	5.11 pF 3.90 pF 0.00 pF 16.8 dB 20.2 dBμV/m	5.11 pF 2.5-6 pF 0.00 pF 23.7 dBμV/m

Tab. 4.2 Performance of SLMW vs. single wire loop at 470 MHz.

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4.4.2 Hints For Selecting the Right Antenna

With the approximation given in Section 2.1 it is possible to find the best antenna for any given limits with respect to budget and size. The main task is to find a compromise between the antenna area and size limit due to the pager package. As described in the previous chapter, an optimal position of the antenna with respect to the human body exists. Much the same holds for preferred positions with respect to the board in order to avoid coupling effects between antenna and pager electronics.

Fig. 4-23 shows the best position of an antenna near a human body: The loop antenna plane should be perpendicular to the body surface and perpendicular to the earth surface. The best position with respect to the pager electronics depends on the layout. In general, the antenna should be as far away as possible from inductors, oscillators and metal objects such as batteries.

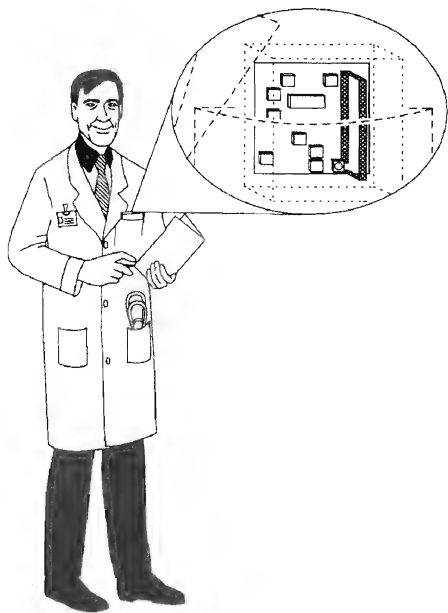


Fig. 4-23 The optimum position of a pager near a human body.

To find the best possible pager sensitivity the following procedure is recommended:

1. Choose an antenna geometry for a single loop antenna which can have the optimum position as shown in Fig. 4-23 and fulfils the pager size requirements.
2. Calculate antenna data and design the appropriate matching network.
3. If it possible to use a $C_{ia} > 1$ pF, do so! If necessary reduce the antenna area somewhat to reduce the antenna inductance. Perhaps use a large feeding in order to realise a non zero C_{ia} without extra capacitor. Furthermore, look into the use of a multi-loop structure (budget ?) to improve the antenna noise figure.
4. In case of a single loop antenna and $C_{ia} > 1$ pF consider an additional improvement by using a SLMW structure (budget ?) or a strip antenna with or without surface coating. In case of a strip antenna avoid additional skin effect losses due to surface roughness, sharp edges and corner cracks, otherwise its advantages will be lost.
5. At high frequencies, where the maximum antenna inductance is restricted (because the resonance C becomes impractically small), C_{ia} must be zero. In that case it makes more sense to select high quality capacitors $2C_{in}$.

The following notions (listed in order of importance) will help to get the best sensitivity:

1. large area, perhaps multi-loop
2. if $C_{ia} > 0$:
 - 2.1. SLMW structure
 - 2.2. strip antenna
 - 2.3. high quality capacitors $2C_{in}$
 - 2.4. coating
3. if $C_{ia} = 0$:
 - 3.1. high quality capacitors $2C_{in}$
 - 3.2. SLMW structure or strip antenna
 - 3.3. (coating)

Pager receivers

Antenna aspects

4.4.3 Advantages and Disadvantages of Multi-loops

The advantage of multi-loops is the large effective loop area $n \cdot a \cdot b$. As can be seen in Table 4-5 a single loop gives a similar pager sensitivity to a dual loop with loops half the size.

Beside the higher cost of producing multi-loops with identical wire distance (with influence on L_{ant}) it will be difficult to construct a multi-wire multi-loop or a strip multiloop in order to lower the antenna losses. Especially at high frequencies a high antenna inductance becomes the limiting factor because a high L_{ant} requires impractically low capacitances in the NMN.

Ultimately, the use of a multi-loop seems to be determined more by the available manufacturing capabilities than by the benefit of a low antenna noise figure.

4.4.4 Antenna Surface Treatment

The metallic surface of a loop antenna must be smooth without grooves and may not have sharp corners or edges. The surface should consist of a conductive material with a thickness of >3 times the skin depth δ (see Eq. 2-4). Of course, solid silver or copper wire can also be used.

The use of tin-plating or nickel and/or iron alloys without a good conductive surface layer will result in a considerable increase of the antenna losses.

To prevent corrosion an organic protective coating (e.g. lacquer) is recommended for cosmetic reasons.

Application of a coating will be determined largely by the permissible manufacturing costs.

4.5 Antenna Examples: Prototypes

Many different loop antennas have been built and tested with the UAA2080T pager receiver. Only a few examples are given on the next pages. All antenna parameters were determined using the PALOMA software.

The antenna dimensions (in particular of the multi-loops) do not permit the use of the simplified equations given in this document. The antennas consist of a copper wire with circular cross section with a diameter of $d = 1$ mm and the feed point was located in the middle of the longer side, if not otherwise specified. In all experiments the most frequently used antenna was the large 5×2.5 cm loop. For smaller antennas the agreement between experiment and theory should be equal or even better.

For all calculations of the NMN $R_{cn} = 0.4 \Omega$ and $R_{ct} = 0.4 \Omega$ have been assumed. Sometimes two slightly different capacitors were used to realise $2C_{in}$. For example, in Table 4-3 $2C_{in}^a = 2.7$ pF and $2C_{in}^b = 3.3$ pF gives $2C_{in} = 2.97$ pF.

The sensitivity results E_{sense} are given for a S_{in}/N_{in} ratio of 1 dB at the demodulator input. of the UAA2080. This corresponds with a Bit Error Rate of 3% in the receiver output data.

Pager receivers

Antenna aspects

loop geometry loop type number of loops with wire distance	feeding geometry	NMN theory	NMN real
L_{ant} R_R R_L F_{ant} C_{corr}	L_f C_f	$2 C_{in}$ C_t C_{la} $1 / G_{NMN+AL}$ E_{sens}	$2 C_{in}$ C_t C_{la} E_{sens}
2.1 x 0.75 cm 5 loops, distance = 1.1 mm corner excitation	3 x 3 mm		
569.74 nH 5.40 mΩ 0.397 Ω 18.86 dB 4.01 dB	2.12 nH 0.05 pF	3.30 pF 8.74 pF 0.00 pF 24.5 dB 20.0 dBμV/m	3.30 pF 3-10 pF 0.00 pF 22.7 dBμV/m
6 x 1.5 cm single loop	5 x 3 mm		
101.04 nH 3.19 mΩ 0.161 Ω 17.25 dB 0.57 dB	3.53 nH 0.08 pF	8.20 pF 3.74 pF 5.60 pF 21.6 dB 13.8 dBμV/m	8.20 pF 2.5-6 pF 2.5-6 pF 14.8 dBμV/m
5 x 2.5 cm single loop		5 x3 mm	
113.59 nH 5.93 mΩ 0.161 Ω 14.62 dB 0.40 dB	3.53 nH 0.08 pF	2.97 pF 2.88 pF 6.00 pF 20.5 dB 11.9 dBμV/m	2.97 pF 2.5-6 pF 2.5-6 pF 12.1 dBμV/m

Tab.4.3 Data of antenna prototypes at $f = 173$ MHz.

Pager receivers

Antenna aspects

loop geometry loop type number of loops with wire distance	feeding geometry	NMN theory	NMN real
L_{ant} R_{R} R_{L} F_{ant} C_{corr}	L_{f} C_{f}	$2 C_{\text{in}}$ C_{t} C_{ta} $1 / G_{\text{NMN+AL}}$ E_{sens}	$2 C_{\text{in}}$ C_{t} C_{ta} E_{sens}
2.1 x 0.75 cm 3 loops, distance = 2.5 mm corner excitation	5 x 3 mm		
177.48 nH 11.19 mΩ 0.255 Ω 13.90 dB 2.76 dB	3.53 nH 0.08 pF	4.26 pF 4.43 pF 0.00 pF 20.6 dB 20.1 dBμV/m	4.26 pF 3-10 pF 0.00 pF 23.8 dBμV/m
6 x 1 cm single loop	5 x 3 mm		
84.90 nH 13.87 mΩ 0.193 Ω 11.88 dB 1.61 dB	3.53 nH 0.08 pF	4.26 pF 3.90 pF 1.80 pF 16.1 dB 13.9 dBμV/m	4.26 pF 2.5-6 pF 1.80 pF 17.4 dBμV/m
5 x 2.5 cm single loop	5 x 3 mm		
117.60 nH 53.89 mΩ 0.207 Ω 6.97 dB 1.13 dB	3.53 nH 0.08 pF	2.97 pF 0.45 pF 1.50 pF 11.0 dB 10.8 dBμV/m	2.97 pF 2.5-6 pF 1.50 pF 14.1 dBμV/m

Tab.4.4 Data of antenna prototypes at $f = 288$ MHz.

Pager receivers

Antenna aspects

loop geometry loop type number of loops with wire distance	feeding geometry	NMN theory	NMN real
L_{ant} R_R R_L F_{ant} C_{corr}	L_f C_f	$2 C_{in}$ C_t C_{ta} $1 / G_{NMN+AL}$ E_{sens}	$2 C_{in}$ C_t C_{ta} E_{sens}
2.1 x 0.75 cm 2 loops, distance = 1.8 mm corner excitation	5 x 3 mm		
115.56 nH 42.17 mΩ 0.232 Ω 8.25 dB 3.53 dB	3.53 nH 0.08 pF	2.20 pF 2.37 pF 0.00 pF 14.6 dB 21.1 dBμV/m	2.20 pF 1.7-3 pF 0.00 pF 22.3 dBμV/m
4 x 0.8 cm single loop corner excitation	5 x 3 mm		
57.66 nH 25.81 mΩ 0.169 Ω 8.91 dB 1.26 dB	3.53 nH 0.08 pF	5.11 pF 3.90 pF 0.00 pF 16.8 dB 20.2 dBμV/m	5.11 pF 2.5-6 pF 0.00 pF 23.7 dBμV/m
5 x 2.5 cm single loop	7 x 3 mm		
132.16 nH 603.84 mΩ 0.264 Ω 1.62 dB 3.12 dB	4.94 nH 0.11 pF	1.80 pF 1.62 pF 0.00 pF 4.5 dB 10.1 dBμV/m	1.80 pF 1.4-2.1 pF 0.00 pF 12.9 dBμV/m

Tab. 4.5 Data of antenna prototypes at $f = 470$ MHz.

Pager receivers

Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

1. GENERAL

The pager receiver circuits UAA2033T and UAA2050T have been around for some time now, finding their way into a host of pager applications. Especially the first circuit was welcomed to the market as an interesting new development, as was demonstrated by the adjudication of the Queens Award for Technology in the United Kingdom in 1989.

Since then, new developments have expanded on this first design, making the direct conversion technology even more suited for the specialized Pager markets, where power economy, high sensitivity and high degree of integration are key factors.

The UAA2033T is no longer a serious candidate for new developments any more, and also the UAA2050T, although still a powerful solution to many applications, should no longer be used for new designs.

In the following paper, the UAA2033T and UAA2050T will be discussed mainly for reference reasons, as many designs with these circuits are still around.

For present developments, the UAA2080T, zero IF, zero offset receiver circuit is offering improved specification and improved packaging allowing for smaller and more advanced designs. For application information on this versatile circuit, please see next paper.

Pager receivers

Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

2. PREFACE

This report was written to give a support to the application of the pager receiver circuits UAA2050T and UAA2033T. After describing the principle of operation and the block schemes of both circuits and their main differences three essential types of application modifications have to be dealt with.

- Change of radio frequency influencing the FRONT-END application
- Change of parameters influencing the BACKEND application
- Controlling

Information about test results and PCB layout hints follows. The Appendices summarize all detailed information which can be expressed as formulae. PCB layouts of the test circuits, pinning and application diagrams finish this report.

3. FEATURES AND QUICK REFERENCE DATA

- Wide operating frequency range, VHF to UHF
- Low noise pre-amplifier ensuring high RF sensitivity (UAA2050T)
- Low current consumption
- Fully compatible with all FSK modulated systems (POCSAG, GOLAY, etc.)
- Low battery voltage detector
- Power down mode, selectable via enable input
- Automatic frequency control (AFC) on chip
- Wide operating supply voltage
- High integration level, few external components
- SO 28 package

Quick Reference Data

Receiver type		UAA 2050T	UAA 2033T	
Frequency range	f	27 – 500	27 – 175	MHz
Noise figure pre-amplifier f = 470 MHz	NF	4	—	dB
Sensitivity at 50Ω (BER = 10 ⁻²) f = 470 MHz	V _{SEN}	0.18 -122	—	μV dBm
	V _{SEN}	0.14 -124	0.20 -121	μV dBm
Current consumption	I _{TOT}	3.0	2.6	mA
Supply voltage range	V _S	1.9 – 3.5	2.0 – 3.5	V
Detection voltage	V _{IND}	1.07 / 2.0	2.135	V
Temperature range	T _{amb}	-10 – +70		°C

4. INTRODUCTION

The UAA2050T and the UAA2033T are integrated receiver circuits primarily intended for use in UHF/VHF paging systems employing direct FM Non-Return-to-Zero (NRZ) Frequency Shift Keying (FSK) modulation.

Used in conjunction with the PCA5000T, PCA5000AT or PCF5001T POCSAG decoders they offer an extremely advanced radio paging concept.

Both ICs are based on the offset receiver architecture and offer highest integration level up to now.

Compared to superhet receivers a dramatically reduced amount of components is achieved which gives a significant breakdown in manufacturing costs with excellent performance.

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Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

In general, RF-circuits cannot be inserted and switched on. To achieve an optimized performance, a few but essential rules have to be followed. Special care has been taken for describing the front-end application which has a significant contribution to the overall performance. Further chapters cover the application of backend and control circuitry.

Typical examples are given to enable a proper selection of external components for other system requirements.

Measurement results are included to enable a performance comparison with the individual application.

The report closes with hints for PCB layout which has also to be taken into account, especially for the UHF range.

5. PRINCIPLES OF OPERATION

Both receiver circuits are working with the "offset receiver" principle, refer to figure 5-1.

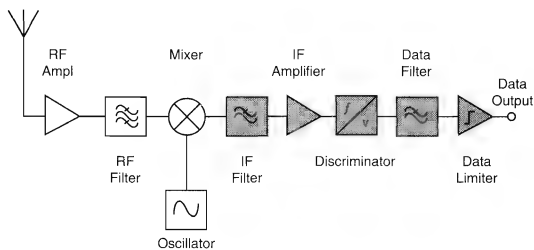


Figure 5-1 Offset receiver principle

As shown in figure 5-2, the basis of the "offset receiver" principle is correct choice of the amount by which the oscillator frequency is offset ("receiver frequency offset f_{OFFS} ") from the carrier frequency of the wanted signal. If the frequency offset is chosen to be half of the transmitter frequency deviation (Δf_{TX}) caused by FSK modulation of the RF-carrier (f_{TX}), the FM spectrum of the wanted signal within the IF-band will have a centre frequency of Δf_{TX} and a shift of Δf_{IF} due to FSK modulation.

$$\Delta f_{\text{IF}} = \frac{\Delta f_{\text{TX}}}{2}$$

Consequently, image rejection is unnecessary because the "image frequency band" is part of the "wanted frequency band" at IF level.

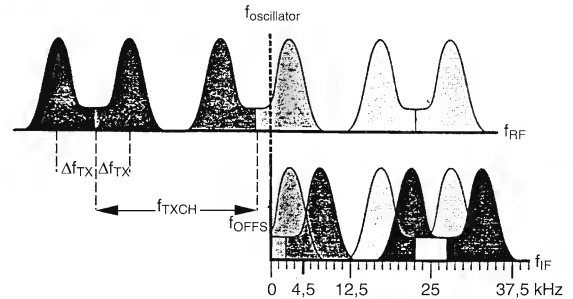


Figure 5-2 Example spectrum Offset receiver

The wanted channel (centre) and unwanted channels to either side and IF spectrum corresponding to the RF spectrum are convoluted around the 225 kHz offset oscillator frequency (channel separation $f_{\text{TXCH}} = 25$ kHz and frequency deviation $\Delta f_{\text{TX}} = 4.5$ kHz assumed).

6. DESCRIPTION OF THE BLOCK SCHEMES

This description is related to the block diagram figure 6-1, which shows the block schemes of both circuits and their main differences. The RF signal from the aerial passes a matching circuit for impedance transformation reasons. In the UAA2050T three additional blocks are now following compared to the UAA2033T:

- Low noise amplifier,
- External RF filter circuit and
- Internal matching circuit.

The RF signal is then mixed down to IF level in a double balanced mixer. This mixer is driven by a local oscillator formed of an XTAL oscillator and a frequency multiplier. The mixer stage is followed by an IF filter block formed of internal amplifiers and external frequency determining components. The filtered IF is amplified in a limiter and then fed through an AFC and Data discriminator. In the

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discriminator the "zero phase" and the phase shifted IF are processed and the resulting signal is squared in a data limiter after having been filtered in the data filter. The ICs incorporate an AFC circuit by means of which the oscillator frequency can be tuned to compensate for all frequency changes, caused e.g. by voltage or temperature drift, XTAL aging or transmitter frequency offset, and to lock the oscillator after switching the receiver on.

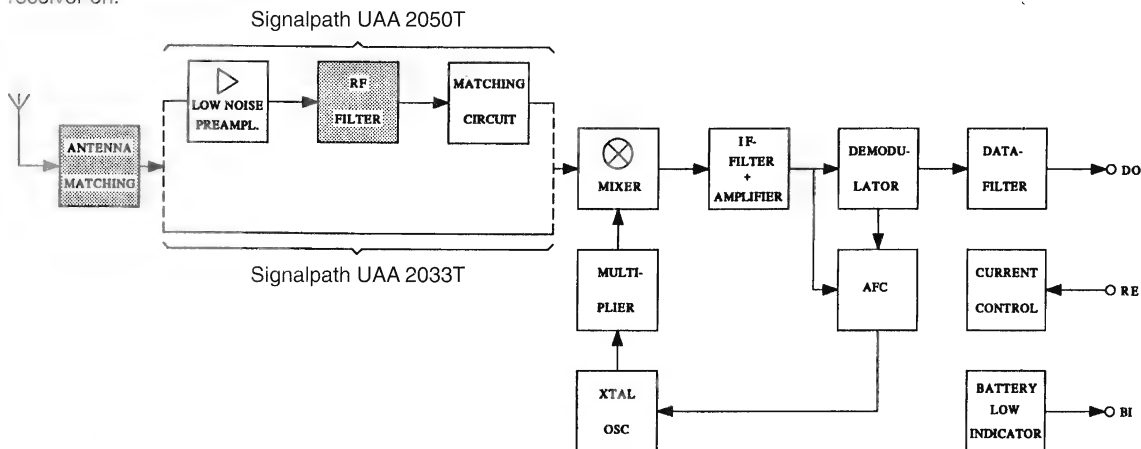


Figure 6-1 Block schemes of the UAA2050T and the UAA2033T

The ICs have also a built in battery low indicator and a current control circuit.

The spectral power of the transmitter carrier frequency f_{tx} does not really contribute to the total power spectrum caused by the NRZ type of the FSK modulation. Due to the fact that the multiplier-frequency has an "offset" of half the transmitter frequency deviation the mixer output signal (IF signal) consists mainly of two different frequencies either one or the other being present at the time. This pair of tones is centred on a frequency equivalent to the deviation frequency which is therefore called the "discriminator operating frequency" f_{dis} (see figure 5-2). The values of these two frequencies only are influenced by frequency offset and deviation and not by the signal bit rate of the transmitted data and of course not by the RF signal frequency.

So we can say that there are three essential types of application modifications that have to be dealt with.

- Change of radio frequency influencing the FRONT-END application
- Change of parameters influencing the BACKEND application
- CONTROLLING

7. OPERATION AND APPLICATION

7.1 Frontend

By changing the radio frequency within the range the UAA2050T and the UAA2033T are specified for questions arise concerning the appropriate design of the RF input stage, the voltage controlled XTAL oscillator and the frequency multiplier circuit.

As the ICs were specified for a wide frequency range (see Features and Quick reference data) we find the nominal application being designed for the upper band limit due to the intention that the circuit should be used as a UHF or VHF paging receiver.

As is well known the sensitivity of a receiver will be mainly determined by the noise figure (NF) of the RF input stage and is in general frequency dependent except from other parameters so that the choice of the generator

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impedance will somehow influence the NF. Another parameter to be taken into account for the design of an aerial is the input impedances of the ICs.

As a part of the frontend of the receiver the local oscillator circuitry has to be adapted to the various RF-frequencies. In these ICs the local oscillator circuitry is formed by a combination of an XTAL oscillator and a frequency multiplier circuit. This arrangement is necessary due to the high oscillator frequency which can mostly not be generated by a simple XTAL- oscillator in one step but has to be generated in a frequency multiplier circuit which will be synchronized by the 3rd or 5th harmonics of the XTAL oscillator. For lower frequencies, of course, it is possible to use the multiplier like an amplifier.

As shown in figure 6-1 the most important difference between both ICs is the low noise amplifier of the UAA 2050T. Therefore two chapters are following for the RF input stages of the UAA2050T and the UAA2033T.

7.1.1 RF input stage

Corresponding to figure 6-1 the RF Input stage of the UAA2050T consists of a matching circuit, a low noise amp (LNA), a RF- filter, a second matching circuit and a mixer. The RF Input stage (see figure 7.1.1-1) is optimized for UHF application with following assumptions:

- LNA current $I = 400 \mu\text{A}$
- Mixer current $I = 400 \mu\text{A}$
- Source Impedance $R = 500 \Omega$
- Loaded Q $Q = 50$

Under these conditions the RF sensitivity V_{SEN} and the voltage of the third order intermodulation product V_{IP3} were optimized by varying the area of the transistors and the matching circuit.

To optimize the RF input stage for different RF frequencies following parameters could be changed by application:

- Source impedance by changing the input matching circuit
- Q of the RF filter.

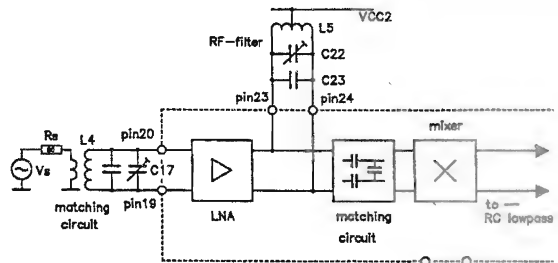


Figure 7.1.1-1 RF input stage of the UAA2050T

7.1.1.1 Low noise amplifier UAA2050T

With respect to the optimization of the receiver application for different frequencies calculations for the low noise amplifier (LNA, see figure 7.1.1-2) have been carried out.

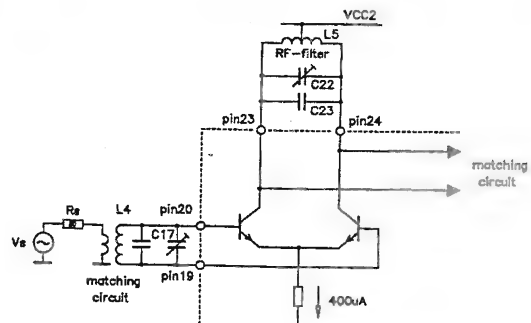


Figure 7.1.1-2 Principle circuit of the LNA of the UAA2050T

To get high sensitivity the generator impedance has to be optimized, i.e. the noise figure (NF) has to be minimized. To minimize the NF it is absolutely necessary to drive the LNA symmetrically.

Figure 7.1.1-3 shows the dependence of the Single Side Band (SSB) noise figure (NF) on the applied source impedance for various frequencies as a function of source impedance R_{GOPT} of the LNA for the UAA2050T.

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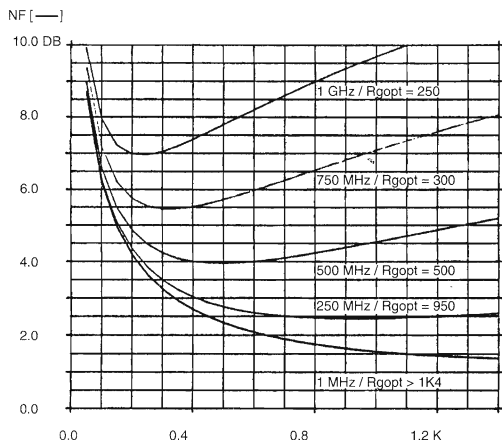


Figure 7.1.1-3 Simulated SSB noise figure for UAA2050T LNA

These curves were computed under the assumption that the imaginary part of the input impedance was compensated for by an LC-circuit in parallel of the LNA input. The inductance of this LC-circuit is formed by an appropriate transformer coil. While in this test application the transformer is needed to generate reproducible source impedances in a practical paging receiver this input circuitry is of course formed by the aerial. The LNA input impedance and capacitance (parallel) for the UAA2050T is shown in figure 7.1.1-4.

To minimize the NF of the whole receiver you have to take care, that the power gain of the first stage is high enough. Therefore the LNA is optimized under the condition that the minimum gain from LNA input to mixer input is 6 dB.

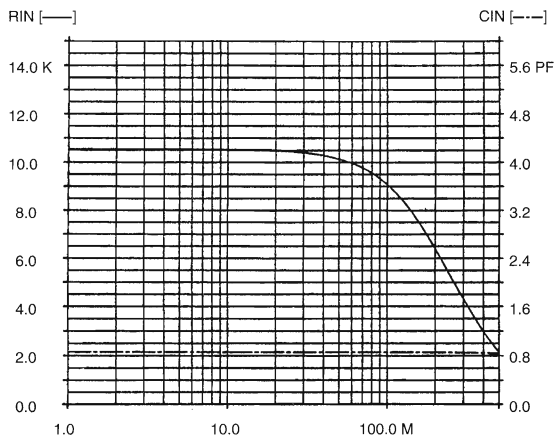


Figure 7.1.1-4 LNA Input impedance and capacitance (parallel) UAA2050T

7.1.1.2 Mixer stage UAA2050T

The principle circuit diagram is shown in figure 7.1.1-5

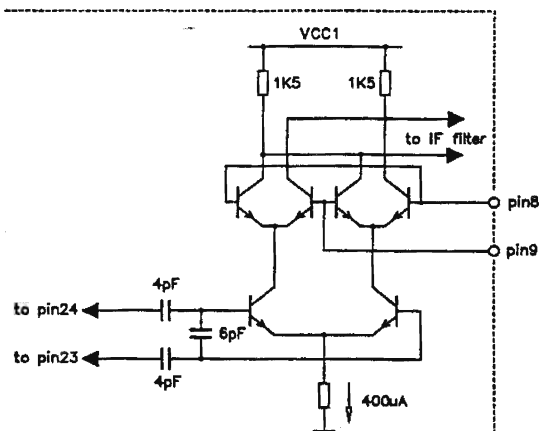


Figure 7.1.1-5 Mixer and matching circuit principle (UAA2050T)

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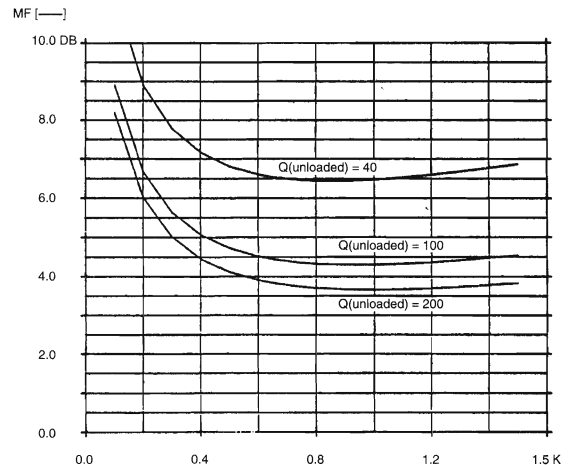
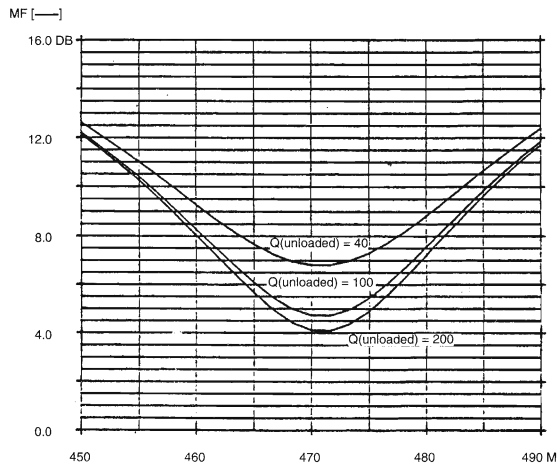


Figure 7.1.1-6 Simulated SSB noise figure for UAA2050T LNA and mixer

7.1.1.3 RF input and mixer stage UAA2033T

The RF input stage of the UAA2033T is the lower layer of the mixer. The principle circuit of the mixer is shown in the figure 7.1.1-7 below.

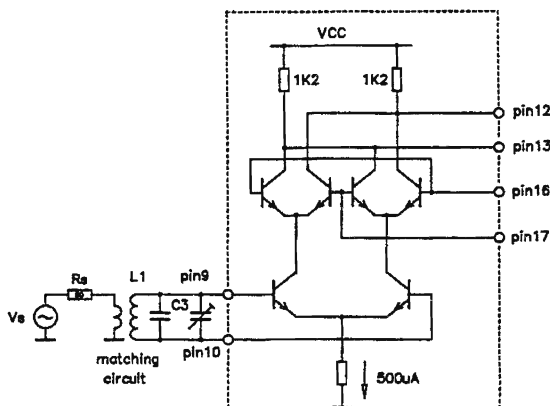


Figure 7.1.1-7 Principle mixer circuit of the UAA2033T

To get high sensitivity the generator impedance has to be optimized, i.e. the noise figure has to be minimized. To minimize the NF it is absolutely necessary to drive the LNA symmetrically. Figure 7.1.1-8 shows the dependence of the NF on the applied source impedance for various frequencies. These curves were computed under the assumption that the imaginary part of the input impedance was compensated for by an LC-circuit in parallel of the mixer input. The inductance of this LC-circuit is formed by an appropriate transformer coil. While in this test application the transformer is needed to generate reproducible source impedances in a practical paging receiver this input circuitry is of course formed by the aerial.

The noise figure curves in figure 7.1.1-8 give an idea about the magnitude of influence of the source impedance on the noise figure. First we can see that there is a 3 dB decrease of noise figure in the frequency range of 174 MHz to 30 MHz if the source impedance is still on its optimum value. On the other hand a slight mismatching of source impedance with respect to its optimum does not have a dramatic effect. This may help while designing a suitable aerial. A decrease of noise figure should be found in an increase of sensitivity as well. The two RF-frequencies 174 MHz and 30 MHz

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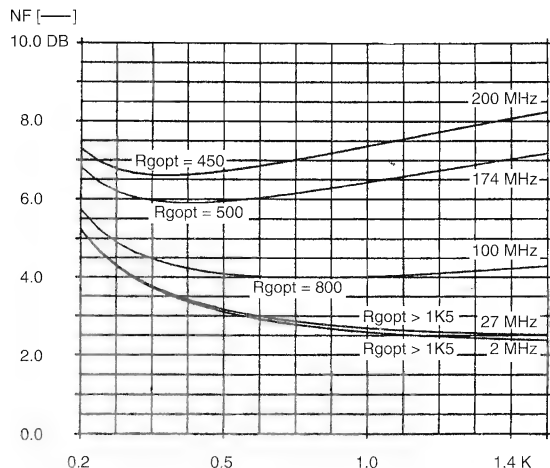


Figure 7.1.1-8 Simulated SSB noise figure for UAA2033T mixer

have been under investigation in our lab and it was found that there is an increase in sensitivity of about 2-3 dB if performing 30 MHz reception, under the precondition that the external components were adapted in a appropriate way.

Another parameter to be taken into account for the design of an aerial is the input impedance of the IC: calculations have been carried out and the results are shown in figure 7.1.1-9. These curves show the real and the imaginary port of the input impedance of the input stage.

7.1.2 Antenna

In general one should notice that much experience and several attempts might be necessary to optimize the antenna and its matching to the receiver. A detailed procedure can not be given.

7.1.2.1 Antenna type

Since there are various antenna principles known it is very difficult to recommend one special type, which fits best to our receivers. Basically the antenna has to be of the symmetrical type, to avoid any unbalanced to

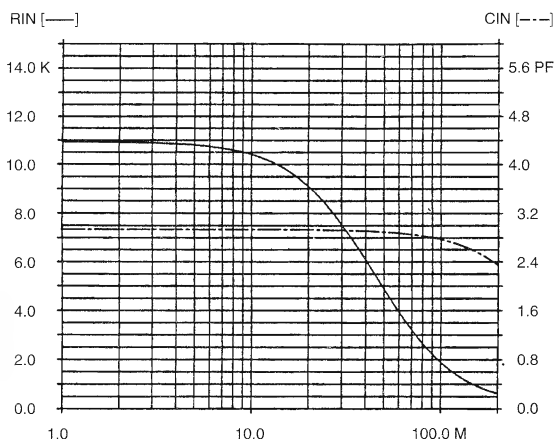


Figure 7.1.1-9 Mixer input resistance and capacitance (parallel) UAA2033T

balanced transformation network and its associated losses. A symmetrical driving of the receiver RF input is necessary, due to the internal receiver design. else a dramatic loss in sensitivity occurs. From the wide range of basic antenna configurations we suggested the folded dipole or loop antenna to be a good choice. Taking into account that the antenna length for a folded dipole is very short (limited by the pager size usually) in comparison to the input signal wave length it always offers an inductive reactive component. like a loop antenna. Compensation and transformation of the antenna impedance can be achieved by a capacitance network. This is of fortune, because of easy application in comparison to a inductive transformation network.

Although several efforts have been made to develop equations and approximations, which describe antenna characteristics, one must notice that these formulae is valid within a free field only. Considering a pager application and its minimum space requirement these formulae get more or less worse, because of the unknown dielectric surrounded from the antenna. To obtain the antenna characteristics from a measurement (antenna impedance at the receive frequency) is the fastest way to precede. However, it is recommended to consider the geometric design rules for the mentioned

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antennas and not to declare a piece of wire connected between two pins and routed somehow to be the antenna. To improve the antenna surface could be considered (e.g. gilding) to improve the antenna performance.

7.1.2.2 Antenna matching

The matching circuit is necessary to compensate any reactant component of the antenna impedance and to transform the antenna impedance, to obtain the best sensitivity. The receiver sensitivity is a function of the source impedance at the RF input. The goal is to optimize the signal to noise ratio at the IF filter output, to obtain a bit error rate which is as low as possible. The best sensitivity can be achieved, if the matching is within the range noise matching to power matching. The noise figure and input impedance presented above, are used to select an appropriate matching circuit for the antenna. Because of the LNA provided for the UAA2050T and its power gain, an antenna impedance matching between noise and power matching should be selected. The noise figure presented for the UAA2050T LNA circuitry shows the source impedance (x-axis) for which the noise figure (y-axis) is a minimum, for several input frequencies as parameter. The UAA2033T doesn't provide a LNA and therefore a matching closer to the power matching has been found to result in the best sensitivity. The mixer input impedance presented for the UAA2033T in the figure above, shows the source impedance necessary for power matching.

The antenna matching circuitries presented below are effective for antenna impedances providing a real part greater or approximate equal to the selected receiver matching impedance, which normally happens, because of the short antenna geometry.

In general a antenna matching circuit may look like the one shown in figure 7.1.2-1 .

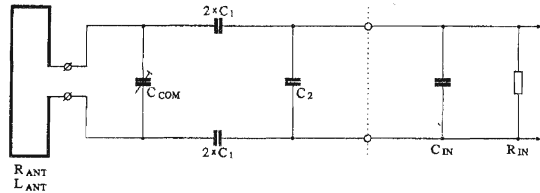


Figure 7.1.2-1 Antenna matching principle (impedance matching ratio IMR > 1)

The antenna impedance is transformed by the operation of a tapped resonant circuit, which is build of the antenna having an inductive reactive component and additional capacitances. To compensate the reactive antenna component the matching circuit has to be in resonance. Obtaining a high quality factor will improve the receiver sensitivity. The total matching circuit capacitance C_{TOT} , which is comprised of C_{COM} , C_1 , C_2 and C_{IN} (parasitic capacitance aren't taken into account), can be estimated according to

$$C_{TOT} = \frac{1}{L_{ANT} * (2 * \pi * f_{RX})^2} \quad A.1-1A$$

The impedance transformation for the matching circuit correspond to the square of the ratio C_1 to C_2 in the case of resonance and if R_{GOPT} as more than ten times the impedance of C_2 . C_2 is estimated according to

$$C_2 = (C_{TOT} - C_{COM}) * \frac{\sqrt{R_{ANT}}}{\sqrt{R_{GOPT}}} - C_{IN} \quad A.1-1B$$

C_{COM} is a capacitor added for tuning of the matching circuit to meet the resonant case. It should be selected to be as low as possible to fulfil the following condition, else the estimations aren't exact and an impedance calculation for the matching circuit will be necessary.

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$$C_2 > \frac{10}{2 * \pi * f_{RX} * R_{IN}} \quad A.1-1C$$

Further, C_1 is estimated according to the following equation. Please notice that because of symmetry reasons two capacitances have been provided, each twice the value of the calculated capacitance, see figure 7.1.2-1.

$$C1 = \frac{(C_2 + C_{IN})}{\frac{\sqrt{R_{ANT}}}{\sqrt{R_{GOPT}}} - 1} \quad A.1-1D$$

In the formulae above, R_{IN} and C_{IN} are obtained from the receiver input impedance figure and R_{GOPT} from the noise figure. R_{ANT} is the real part from the antenna impedance and L_{ANT} its inductance.

If the impedance matching ratio IMR gets close to one, C_1 becomes very high valued.

$$IMR = \frac{\sqrt{R_{ANT}}}{\sqrt{R_{GOPT}}} \quad A.1-1E$$

The impedance transformation may now be omitted, because of an impedance transformation ratio close to 1. The matching circuit may now look like the one shown in figure 7.1.2-2.

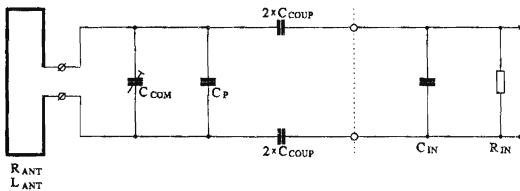


Figure 7.1.2-2 Antenna matching principle (impedance matching ratio $IMR \approx 1$)

This matching circuitry is built up symmetrical also, like the one in figure 7.1.2-1, for appropriate driving of the receiver input. Two coupling capacitors (C_{COUP}) have been added to improve the common mode rejection of the receiver input for low frequency irradiation into the

antenna (50 Hz, microcontroller and POCSAG decoder clock frequency, etc.). The matching circuit has to be in resonance to compensate any reactive antenna component and to improve the sensitivity by means of the quality factor. The total matching circuit capacitance may be estimated according to the equation given above (A.1-1). C_{COM} is known to be the tuning capacitance to meet the resonant case. An additional capacitance (C_P) in parallel might be necessary if C_{COM} doesn't provide sufficient capacitance or to spread Us tuning range. C_P may be estimated according to

$$C_P = C_{TOT} - C_{COM} - C_{IN} \quad A.1-1F$$

The influence of the coupling capacitors (C_{COUP}) needn't to be considered, because of their high value in contrast to the receiver input capacitance (C_{IN}). The coupling capacitors (C_{COUP}) should provide a sufficient low impedance at the receive frequency to avoid a loss in sensitivity. Please notice that two coupling capacitances have been provided for symmetry reasons, each twice the value of the calculated capacitance, see figure 7.1.2-2. Allowing a loss of less than 0,2 dB the coupling capacitance may be estimated according to

$$C_{COUP} = \frac{5}{2 * \pi * f_{RX} * R_{IN}} \quad A.1-1G$$

Finally, a more complex solution for antenna matching shall only be mentioned. Its basic idea is to provide the impedance transformation by tapping of the antenna itself. Interconnection to the rf inputs may be formed of a balanced line, which may also be used to serve as a transformation network.

7.1.3 Voltage controlled crystal oscillator

A voltage controlled crystal oscillator is used as a reference, to determine the receive frequency (f_{RX}) by means of a multiplier circuitry. The multiplier circuitry is locked to the 3rd or 5th harmonic of the crystal oscillator frequency (f_{XOSC}), in order to achieved the high mixer injection signal frequency, necessary for UHF resp. VHF applications. For lower frequencies, the multiplier circuitry may be operated as an amplifier. For proper offset receiver operation it is essential necessary to provide a frequency offset between the mixer injection signal and the desired receive frequency, according to the transmitter frequency deviation used.

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$$f_{\text{OFFS}} = \frac{1}{2} * |\Delta f_{\text{TX}}| \quad \text{A.2-1A}$$

The crystal oscillator frequency (f_{xosc}) has to be selected according to the following equation.

$$f_{\text{xosc}} = \frac{f_{\text{RF}} + f_{\text{OFFS}}}{A} \quad \text{A.2-1B}$$

A may be 1, 3 or 5, depending of the receiver device and multiplier application used. The standard application select A = 3 for VHF and A = 5 for UHF. Note that A = 5 is possible for the UAA2050T only. A = 1 is used, when the receive frequency is very low. The multiplier then operates as an amplifier, consequently, the crystal oscillator operates at the receive frequency. In the other cases, the crystal oscillator frequencies range around 50 MHz for VHF and around 90 MHz for UHF normally. Obviously, the crystal used will be of the overtone type. A 3rd overtone crystal is used for VHF applications, a 5th overtone crystal is used for UHF applications normally. Of course the UAA2050T and UAA2033T crystal oscillator circuits can also run crystals in a different overtone or even in fundamental mode. Please do not mix the overtone mode of the crystal with the multiplier characteristics (A, 1, 3 or 5).

As shown in figures 7.1.3-1 and 7.1.3-2 the oscillator has been internally designed as a Colpitts oscillator with an crystal as a frequency determining feedback circuit. By means of an internal AFC circuit the capacitor in series to the crystal changes from $C = \infty$ to $C = C_{\text{AFC}}$, providing frequency pulling of the oscillator. Additionally there is an extra damping resistor R_{DAMP} or R_{10} , applicable to increase the lock-in-range and to avoid spurious oscillation at unwanted frequencies. The additional inductance L1 (UAA2050T) parallel to the crystal compensates the package capacitance C_{oxL} of the crystal to avoid spurious oscillation. For the UAA2033T oscillator no inductance for compensation is necessary.

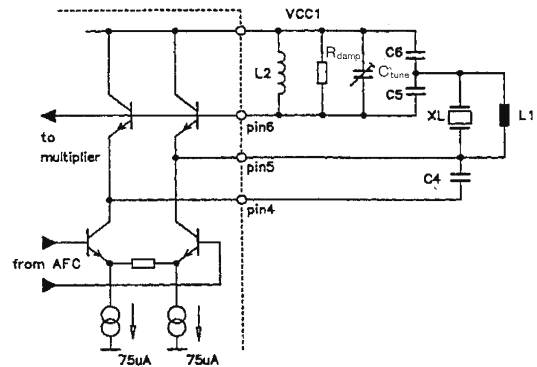


Figure 7.1.3-1 Principle oscillator circuit of the UAA2050T

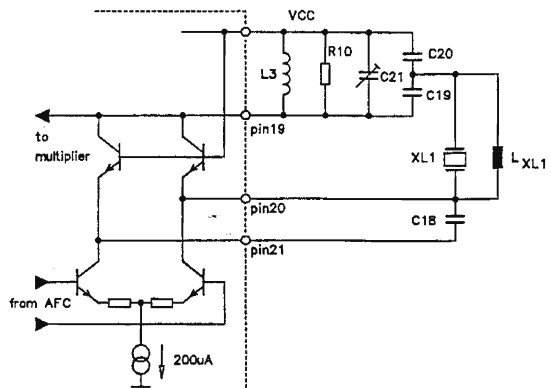


Figure 7.1.3-2 Principle oscillator circuit of the UAA2033T

The capacitance ratio (C_6/C_5 resp. C_{20}/C_{19}) of the oscillator tank circuit should be calculated corresponding to following equation

$$\text{CTR} = \frac{\sqrt{R_p}}{\sqrt{(R_s + r_e)}} - 1 \quad \text{A.2-2C}$$

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The tuning capacitance C_{TUNE} or C_{21} should be as small as possible but large enough to compensate the spreads of the used Inductance and capacitance. In the following one finds a number of diagrams, which may help to design the tank circuit.

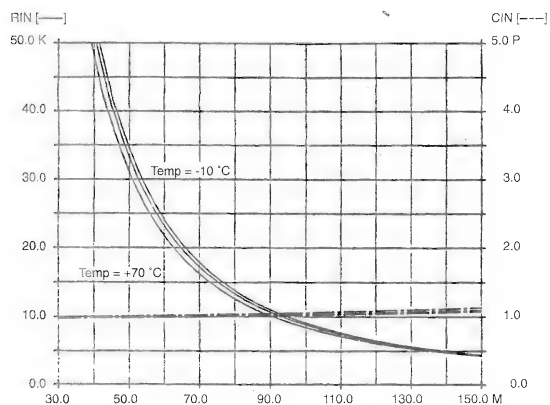


Figure 7.1.3-3 Input resistance and capacitance (parallel) UAA2050T oscillator pin 6

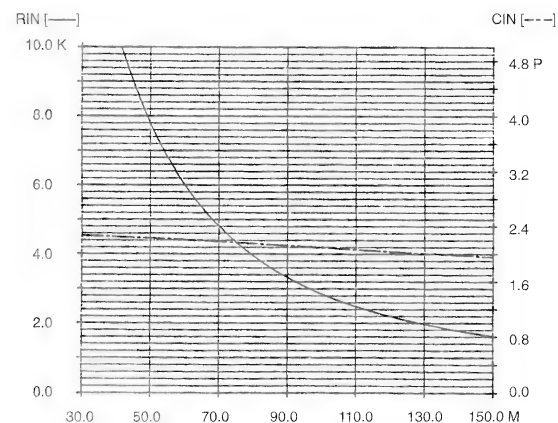


Figure 7.1.3-4 Input resistance and capacitance (parallel) UAA2033T oscillator pin 19

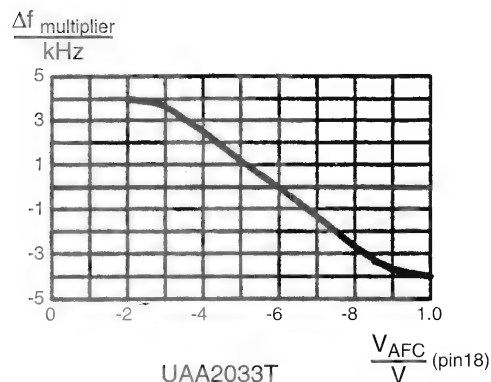
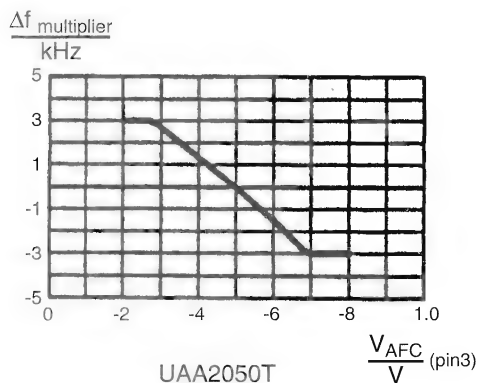


Figure 7.1.3-5 Oscillator frequency as function of AFC voltage (test circuit)

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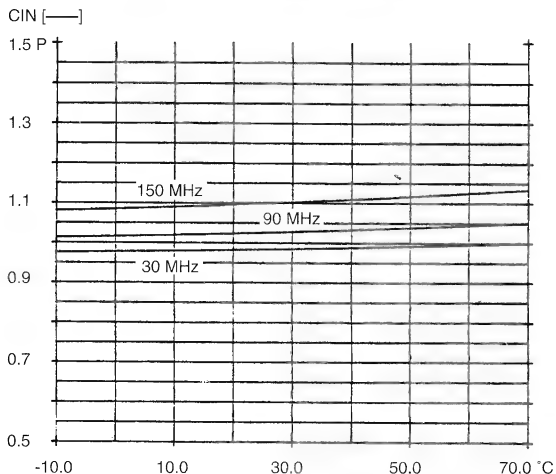


Figure 7.1.3-6 Input capacitance UAA2050T oscillator over temperature

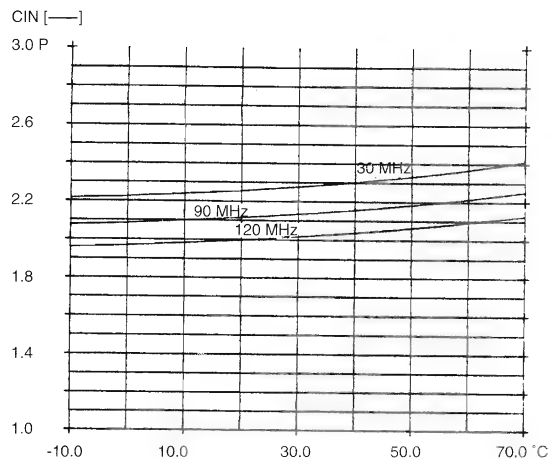


Figure 7.1.3-7 Input capacitance UAA2033T oscillator over temperature

7.14 Frequency multiplier

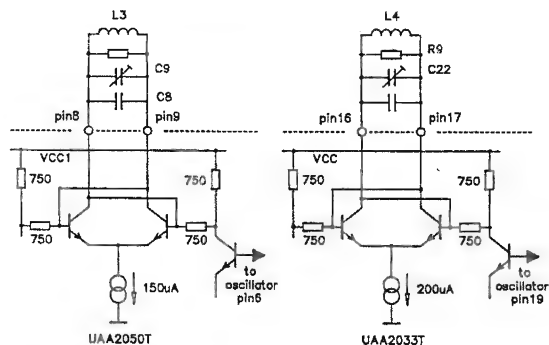


Figure 7.1.4-1 Principle circuit of the frequency multiplier

The multiplier circuit incorporates a damping resistor, too; a measure by which the synchronization range is widened. This leads to better spectral purity of the multiplier oscillator signal, especially in case of slightly mistuned multiplier tank circuit (a mistuned synchronized oscillator shows asymmetric sideband noise spectra). Mistuning can occur because of adjustment tolerances, ageing, and in case of AFC operation.

To guarantee proper operation of the mixer, i.e. sharp transitions in the double balanced stage, under the aspect of noise a drive level of the mixer stage of at least 150 mV peak oscillator level is required. Thus a certain equivalent parallel resistance in the multiplier circuit should be provided as this resistance is a measure of the amplitude of the multiplier oscillator voltage. The component values of the multiplier circuitry should be calculated using the following relations:

$$C_{EXT} = \frac{1}{(2 * \pi * (f_{RX} + f_{OFFS}))^2 * L_M} - C_{IM} \quad A.3-1A$$

In the case the multiplier is operated as an amplifier ($A = 1$, see 7.1.3), the capacitive and inductive components at the multiplier terminals may be omitted. However, a resistor of about 1 k Ω should be provided across the terminals, in order to avoid an overloading of the mixer.

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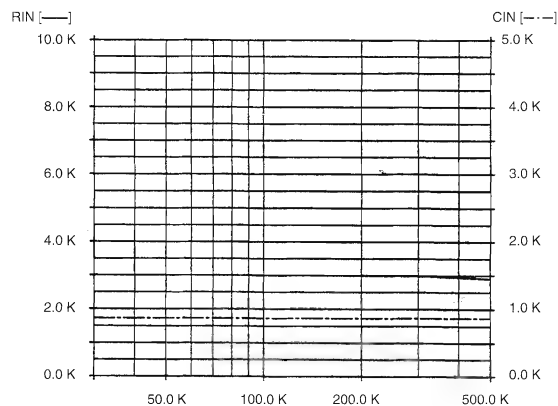


Figure 7.1.4-2 Input resistance and capacitance (parallel) UAA2050T multiplier

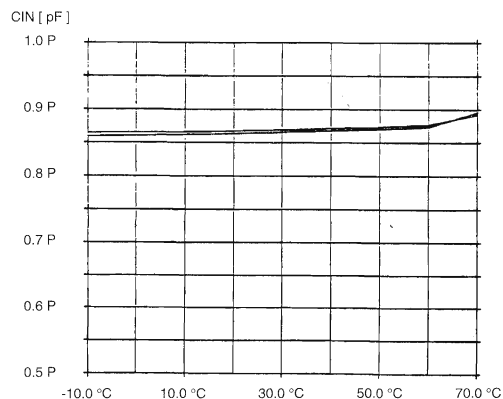


Figure 7.1.4-4 Input capacitance UAA2050T multiplier over temperature

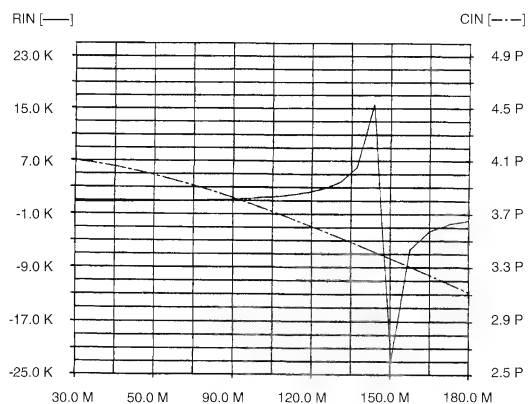


Figure 7.1.4-3 Input resistance and capacitance (parallel) UAA2033T multiplier

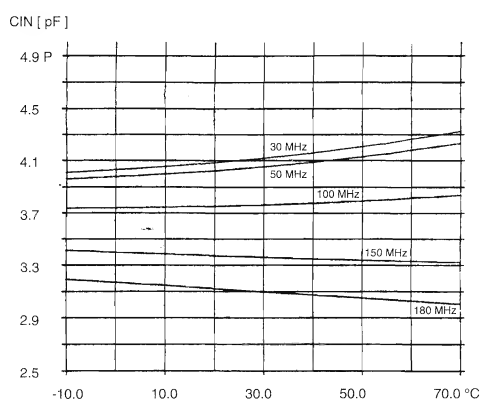


Figure 7.1.4-5 Input capacitance UAA2033T multiplier over temperature

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7.1.5 Crystal specification

The receiver crystal determines the radio receive frequency of the pager. The allowed total difference between transmit and receive frequency is composed of a transmit frequency offset and a local oscillator frequency error, which is caused by temperature drift and ageing of the receiver crystal.

The local oscillator frequency (f_{LO}) is generated by a multiplier circuit, which is normally locked to the 3rd (VHF) or 5th (UHF) harmonic of crystal oscillator. The crystal oscillator itself, normally uses an overtone crystal in series resonance to determine the crystal oscillator frequency (f_{XOSC})

7.1.5.1 Required crystal precision

The automatic frequency control (AFC) of the receiver circuits can operate to a theoretical maximum frequency error which is equal to the transmitter frequency deviation used. The AFC controls the crystal oscillator frequency so as to decrease the frequency error and finally make it disappear. In practise the maximum frequency error (Δf_{AFC}) is reduced to the value given as AFC lock-in-range in the data sheet, see also section 7.2.1 .

$$\Delta f_{AFC} \leq \Delta f_{LOCK}$$

A.2-3A

A lock-in-range of $\Delta f_{LOCK} = \pm 3$ kHz is specified for the UAA2050T, whereby it is $\Delta f_{LOCK} = \pm 4$ kHz for the UAA2033T. This holds for a transmitter frequency deviation of $\Delta f_{TX} = \pm 45$ kHz as specified in the data sheet. These figures give the maximum tolerable error between receive and transmit frequency at the beginning of the AFC frequency correction process. Please note that the frequency offset required for the offset receiver operation does not contribute to this difference!

It is easily seen that above mentioned limits impose a constraint on the stability of the local oscillator frequency and thus on the receiver crystal. The tolerable absolute frequency error is translated into a relative frequency error (S_{MAX}) according to

$$S_{MAX} = \frac{\Delta f_{LOCK}}{f_{RX}}$$

A.2-3B

S_{MAX} is measured in parts per million (ppm) and f_{RX} is the nominal receive frequency. Table 7.1.5-1 shows S_{MAX} for various values Of Δf_{LOCK} and receive frequency f_{RF}

Δf_{LOCK}	f_{RX}	S_{MAX}
± 4 kHz	130 MHz	$\pm 30,8$ ppm
± 4 kHz	30 MHz	± 133 ppm
± 4 kHz	170 MHz	$\pm 23,5$ ppm
± 3 kHz	170 MHz	$\pm 17,6$ ppm
± 3 kHz	470 MHz	$\pm 6,4$ ppm

Table 7.1 .51 S_{MAX} for various values of Δf_{LOCK} and f_{RX}

As can be seen from table 7.1.5-1, S_{MAX} gets smaller and smaller as the radio frequency f_{RX} increases. S_{MAX} is composed of a transmitter frequency offset and a receiver frequency error.

The relative transmitter frequency offset (S_{TX}) is defined as a deviation (f_{TXOFS}) from the nominal transmitter centre frequency (f_{TX}). It is intentionally introduced in some paging systems to decouple the transmitters of adjacent paging cells. The relative transmitter frequency offset S_{TX} can be expressed as follows

$$S_{TX} = \frac{f_{TXOFS}}{f_{TX}}$$

A.2-3C

Table 7.1.5-2 gives some values S_{TX} for typical values of the transmitter offset and nominal channel frequencies.

f_{TXOFS}	f_{TX}	S_{TX}
± 50 Hz	30 / 170 / 470 MHz	$\pm 1,6 / 0,3 / 0,1$ ppm
± 250 Hz	30 / 170 / 470 MHz	$\pm 8,3 / 1,5 / 0,5$ ppm
± 800 Hz	30 / 170 / 470 MHz	$\pm 26,7 / 4,7 / 1,7$ ppm
± 1200 Hz	30 / 170 / 470 MHz	$\pm 40 / 7,0 / 2,6$ ppm

Table 7.1.5-2 S_{TX} for various values of Δf_{TXOFS} and f_{TX}

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According to the maximum tolerable frequency error (S_{MAX}) and the relative transmitter frequency offset (S_{TX}), the upper limit (S_{RXMAX}) imposed on the relative receiver error (S_{RX}) can be written as

$$S_{RXMAX} = S_{MAX} - S_{TX} \quad \text{A. 2-3D}$$

The relative receiver frequency error (S_{RX}) is defined as a deviation (Δf_{RX}) from the nominal receive centre frequency (f_{RX}), caused by temperature drift (ΔT , given in ppm over temperature range) and ageing effects (ΔA , given in ppm per year) in the crystal oscillator frequency. It can be expressed as follows

$$S_{RX} = \frac{\Delta f_{RX}}{f_{RX}} = \Delta T + N \cdot \Delta A \quad \text{A. 2-3E}$$

If the radio pager is designed for a product life time of N years and if the pager has to fulfil the specification over temperature range after N years, following relation has to be become true

$$S_{RX} \leq S_{RXMAX} \quad \text{A. 2-3F}$$

Thus, the first design steps are to compute S_{RXMAX} and to select a crystal with parameters temperature drift and ageing that fulfil the above mentioned relation. If after N years operation the operating temperature range can be reduced compared to the original specification, appropriate weighing factors for the temperature drift ΔT have to be introduced. This will normally reduce the crystal cost, because in the first place no ageing is present and S_{RX} is determined by ΔT alone. However, proper design philosophy will take both components, temperature drift and ageing, fully into account.

Example:

With

$$\Delta f_{LOCK} = \pm 4 \text{ kHz}, f_{RX} = f_{TX} = 170 \text{ MHz}, f_{TXOFS} = \pm 250 \text{ Hz}$$

you get

$$S_{MAX} = \pm 23,5 \text{ ppm}, S_{TX} = \pm 1,5 \text{ ppm} \text{ and } S_{RXMAX} = \pm 22 \text{ ppm.}$$

A crystal with $\Delta T = \pm 7,5 \text{ ppm}$ and $\Delta A = \pm 3 \text{ ppm per year}$ can be used in a pager designed for $N=4$ years operating life, since

$$S_{RX} = \Delta T + N \cdot \Delta A = \pm (7,5 \text{ ppm} + 12 \text{ ppm}) = \pm 19,5 \text{ ppm}$$

$$S_{RX} \leq S_{RXMAX} (\pm 22 \text{ ppm}).$$

7.1.5.2 Crystal series resonant frequency

In our pager receiver circuits the crystal oscillator is operated as a voltage controlled oscillator (VCO). Therefore, the two properties series resonant frequency and pullability of the crystal have to be specified to guarantee save operation over a limited frequency range.

An inductive component is placed in series to the crystal to pull it towards lower frequencies whereas a capacitor in series to the crystal pulls its operating frequency upwards. The series resonant frequency of the crystal is specified without any component connected in series to it. This is equivalent to putting a capacitor of infinite value in series to the crystal ($C_L = \infty$). Unfortunately the inductive pulling range (df_L) is only a fraction of the capacitive pulling range (df_C), see figure 7.1.5-1 for an illustration.

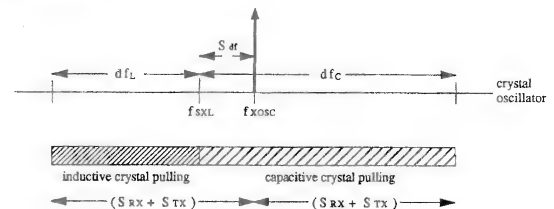


Figure 7.1.5-1 Crystal series resonant frequency selection

Let the capacitive range be α -times wider than the inductive range

$$\alpha = \frac{df_C}{df_L} \quad \text{A.2-4A}$$

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Values for α range from 1 to 5 normally. Obviously, the unloaded crystal resonant frequency (f_{SXL}) is located below or equal to the desired crystal oscillator frequency (f_{XOSC}), according to the value of α . In the case α is not equal 1, the crystal series resonant frequency cannot be set exactly for the nominal crystal oscillator frequency, but must be lowered in favour of a reduced inductive pulling range, in order to achieve a symmetrical pulling range, refer to figure 7.1.5-1.

The relative frequency difference (S_{df}) between the crystal series resonant frequency and the crystal oscillator frequency is calculated according to

$$S_{df} = \frac{(\alpha - 1)}{(\alpha + 1)} * |S_{RX} + S_{TX}| \quad A.2-4B$$

The absolute crystal series resonant frequency (f_{SXL}) is calculated according to

$$f_{SXL} = f_{XOSC} - S_{df} * f_{XOSC} \quad A-2-4C$$

The crystal oscillator frequency (f_{XOSC}) is computed according to the transmitter system parameter and the multiplier application, refer to the voltage controlled XTAL oscillator (7.1.3).

7.1.5.3 Crystal pullability and related load capacitance

With the AFC pulling capacitor C_{AFC} fully placed in series to the crystal, the frequency change results as

$$P_{MIN} = S_{df} + |S_{RX} + S_{TX}| \quad A.2-5A$$

P_{MIN} is the minimum frequency change necessary in order to jump to the highest receive frequency required, refer to figure 7.1.5-1.

However, there is also an upper limit (P_{MAX}) on the usable crystal pullability, introduced by the maximum frequency error that the AFC circuit can handle in theory. For the offset receiver principle, used for the UAA2050T and UAA2033T, in theory this is two times the receiver frequency offset provided. Thus, according to the offset

frequency (f_{OFFS}) and receive channel frequency (f_{RX}) the upper limit is calculated as follows

$$P_{MAX} = 2 * \frac{f_{OFFS}}{f_{RX}} + S_{df} + |S_{RX}| \quad A.2-5B$$

Example:

With the results from the above example and $\alpha=3$ and $f_{XOSC} = 56,6674$ MHz you get

$$S_{df} = 10,5 \text{ ppm and } f_{SXL} = 56,6668 \text{ MHz}$$

further

$$P_{MIN} = 31,5 \text{ ppm and } P_{MAX} = 56,5 \text{ ppm.}$$

As ageing effects normally move the crystal resonant frequency towards lower frequencies a pulling range between P_{MIN} and P_{MAX} should be specified.

In order to calculate the load capacitor required to cause a change in resonant frequency of P_{MIN} , two parameters of the crystal need to be known, the static capacitance (C_{0XL}) and the dynamic capacitance (C_{1XL}). These values are normally given by the crystal manufacturer in his data books. Then the crystal load capacitor can be calculated as follows

$$C_L = \frac{C_{1XL}}{2 * P_{MIN}} - C_{0XL} \quad A.2-5C$$

Example:

$$\text{With } C_{0XL} = 7 \text{ pF, } C_{1XL} = 1,5 \text{ fF and } P_{MIN} = 31,5 \text{ ppm}$$

you get

$$C_L = 16,8 \text{ pF.}$$

From the crystal load capacitor (C_L) the real AFC pulling capacitor (C_{AFC}) can be calculated by subtracting parasitic and inherent capacitors (C_{PAR}), present between pins from C_L . The sum of those capacitors can be closely approximated by 4 pF to 6 pF.

$$C_{AFC} = C_L - C_{PAR} \quad A.2-5D$$

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If in practise the AFC pulling range should prove to be too wide, the AFC pulling capacitor must be increased. If it is too narrow, the AFC capacitor should be decreased in value. However, the designer should not expect the AFC pulling range to become more than what is given as AFC lock-in-range in the appropriate data sheet.

For example, the final crystal specification would be:

- | | |
|---|---|
| a) Series resonant crystal | 3rd overtone mode |
| b) Series resonant frequency without load | $f_{SXL} = 56,6668 \text{ MHz}$ |
| c) Cutting tolerance | $\pm 10 \text{ ppm}$ |
| d) Temperature range | as required |
| e) Temperature drift over specified range | less than $\pm 7.5 \text{ ppm}$ |
| | 25°C as reference point |
| f) Pullability of the crystal | min. 31.5 ppm |
| | max. 56.5 ppm |
| | with a series load capacitor of $C_L = 16.8 \text{ pF}$ |
| g) Ageing per year | less than $\pm 3 \text{ ppm}$ |

In most applications it will be useful to let the crystal manufacturer perform some preageing on the crystals prior to delivery. Preageing can compensate for the relatively large frequency change in the first year while in the following years the relative amount of frequency change per year is typically smaller.

7.2 Backend

This part of the IC circuitry processes the low-frequency signal train, available at the mixer output. The backend consists of a high selectivity 5 stage IF-filter section, a limiter, a data- and an AFC-discriminator, to recover the data signal original transmitted and to derive a tuning signal for fine tuning the local oscillator by an afc feedback loop, and a data filtering and data forming, see figure 7.2-1 for a block scheme.

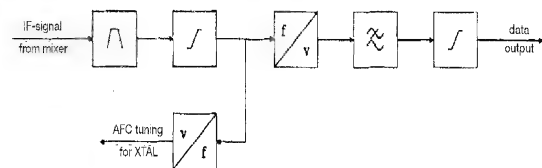


Figure 7.2-1 Backend block scheme

The characteristic of the backend is mainly determined by the components applied externally to the receiver.

Therefore, the receivers UAA2050T and UAA2033T may be used in a wide range of applications.

7.2.1 Design determining parameters

The design of the external components depend on the demands of the system, the receiver is to be used in. The important parameters are:

- transmitter frequency deviation
- offset frequency
- frequency lock-in range
- data rate
- required adjacent channel rejection

7.2.1.1 Transmitter frequency deviation

The discriminator centre frequency (f_{DIS}), for the data- and AFC-discriminator, will be chosen according to the transmitter frequency deviation (Δf_{TX}). The discriminator centre frequency applied to the UAA2050T and UAA2033T standard application is selected as follows:

$$f_{DIS} = |\Delta f_{TX}| \quad \text{A. 6-1A}$$

7.2.1.2 Offset frequency

The offset frequency (f_{OFFS}) is determined by the transmitter frequency deviation (Δf_{TX}). In general, the offset receiver principle requires the frequency offset to be less than the transmitter frequency deviation. The UAA2050T and UAA2033T are intended to operate with a offset frequency, which is half the value of the transmitter frequency deviation, because of AFC-function reasons.

$$f_{OFFS} = \frac{1}{2} * |\Delta f_{TX}| \quad \text{A. 2-1A}$$

The offset frequency and the transmitter frequency deviation determine the IF-filter cutoff frequencies and the IF-filter bandwidth (BW_{IF}). The two tone frequencies, which shall pass the IF-filter, are:

$$f_{IF1} = |\Delta f_{TX}| - f_{OFFS} \quad \text{A.4-1A}$$

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$$f_{IF2} = |\Delta f_{TX}| - f_{OFFS} \quad A.4-1B$$

This implies a minimum IF-filter bandwidth (BW_{IF}) of:

$$BW_{IF} > 2 * f_{OFFS}$$

The IF-filter bandwidth is increased according to the frequency lock-in range applied to the receivers.

7.2.1.3 Frequency lock-in range

Within the frequency lock-in range, the receiver compensates drifts of the frequency determining components and any uncertainty of the transmitter frequency. Although the lock-in range is set by the application of the crystal oscillator (see frontend), two further parameters have to be considered, which limit the AFC lock-in range applicable. It is the offset frequency and the upper IF-filter cutoff frequency.

The lower side (def.: accurate transmitter and receiver oscillator frequency decreases) of the lock-in range ($-\Delta f_{AFC}$) is limited by the offset frequency used and must not exceed two times the offset frequency.

$$|\Delta f_{AFC}| < 2 * f_{OFFS} \quad A.2-4A$$

Otherwise the receiver may lock to the inverted position, where the receiver will receive the same data channel, but with inverted data polarity, see fig. 7.2.1 - 1.

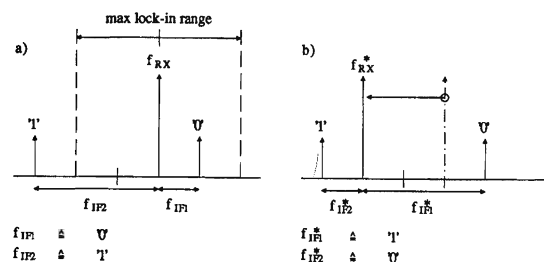


Figure 7.2.1-1 Lock-in range limitation within the IF-bandwidth

Figure 7.2.1-1a shows the normal position. If the frequency drift exceeds two times the offset frequency (e.g. local oscillator frequency f_{XOSC} drops), the receiver locks to the inverted position, see figure 7.2.1-1b. The lock-in range limitation is independent from the IF-filter bandwidth.

The upper side (def.: accurate transmitter and receiver oscillator frequency increases) of the lock-in range ($+\Delta f_{AFC}$) is limited by the IF-filter bandwidth. The lower (f_{IFCL}) and upper (f_{IFCU}) IF-filter cutoff frequencies may be estimated according to:

$$f_{IFCL} = |\Delta f_{TX}| - f_{OFFS} - |\Delta f_{AFC}|$$

$$f_{IFCU} = |\Delta f_{TX}| + f_{OFFS} - |\Delta f_{AFC}|$$

The lower cutoff frequency may become very low-valued or may drop to DC, dependent on the frequency drift assumed. Because of AFC-biasing reasons (noise shaping) it is of disadvantage to introduce a very low-valued lower IF-filter cutoff frequency. The standard application uses a lower IF-filter cutoff frequency of about 800 Hz. You will recognize that the lock-in range upper side ($+\Delta f_{AFC}$) is therefore limited to about 1,45 kHz, if only one transmitter frequency ($f_{TX} + |\Delta f_{TX}|$) is transmitted. Please consider that this fact will not force a problem in a real pager system environment, because the transmitter is modulated by an alternating signal during preamble and synchronization codeword transmission at least. If the receiver not able to lock, while the transmitter frequency (f_{TX}) is $f_{TX} = f_{TX} + |\Delta f_{TX}|$, it will lock during the time period, where the transmitter frequency is $f_{TX} = f_{TX} - |\Delta f_{TX}|$. Provided that the upper IF-filter cutoff frequency matches the requirements given in the equation above.

Therefore, the upper IF-filter cutoff frequency is decisive, if the transmitter is found to transmit alternating frequencies at regular intervals.

$$f_{IFCU} = |\Delta f_{TX}| + f_{OFFS} + |\Delta f_{AFC}| \quad A.4-1D$$

The maximum AFC lock-in range recommended for the standard application UAA2050T is $\Delta f_{LOCK} = 3$ kHz and $\Delta f_{LOCK} = 4$ kHz for the UAA2033T.

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7.2.1.4 Data rate

The offset frequency (and therefore the transmitter frequency deviation used) applied, limits the maximum efficient data rate applicable. The higher the data rate is, the more difficult it becomes, to identify the IF-signal frequencies within a single data bit period, which will result in a loss of sensitivity. The receivers are recommended to be used at data rates up to 1200 bps. Further increasing the data rate reduces the sensitivity much stronger. For 2400 bps operation the loss in sensitivity is more than 16 dB. This might be acceptable, if for example the UAA2050T or UAA2033T are used for the second mixer and IF-stage of a double superhet receiver. However, the data rate else doesn't affect the IF-filtering section. It is of signification for the data filtering only, which applies after the data discriminator (see data filtering).

7.2.1.5 Adjacent channel rejection

One further important parameter is the required adjacent channel rejection, which is given by the system specification. The IF-filter has to have a sufficient attenuation at the stopband frequency (f_s), which is determined by the transmitter frequency deviation (Δf_{TX}) the offset frequency (f_{OFFS}) and the channel spacing (f_{TXCH}), as follows:

$$f_s = f_{TXCH} - f_{OFFS} - |\Delta f_{TX}| \quad A.4-1E$$

Together with the upper IF-filter cutoff frequency (f_{IFCU}), the stopband frequency (f_s) determines the IF-filter order required. The standard application UAA2050T and UAA2033T are shown to use a 7th order low-pass. The adjacent channel rejection is better than 60 dB, if 25 kHz channel spacing and 4,5 kHz transmitter deviation are used. A reduction of the AFC lock-in range may be used to improve the selectivity. Designed for 2 kHz minimum AFC range, the standard application will be found to have an AFC lock-in range of 3 kHz typical.

However, other filter orders and types may be implemented, to satisfy stronger specification requirements or to simplify the design, when possible.

7.2.2 IF-Filtering

The IF-filter is responsible for the adjacent channel selectivity and for some gain, to be able to drive the limiter. The IF-filtering is achieved by a series combination of a 1st order low-pass, a 2nd order Salen & Key low-pass, an 3rd order Causer low-pass, a 1st order high-pass and a second 1st order low-pass, see figure 7.2.2-1.

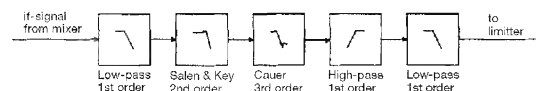


Figure 7.2.2-1 IF-filter block scheme

The required adjacent channel selectivity is achieved by low-pass filtering, whereby the main selectivity is achieved by the operation of the Causer and Salen & Key low-pass. The high-pass filter is provided to form a dc blocking at the limiter input and also attenuates any $1/f$ noise. Figure 7.2.2-2 shows a typical attenuation characteristic.

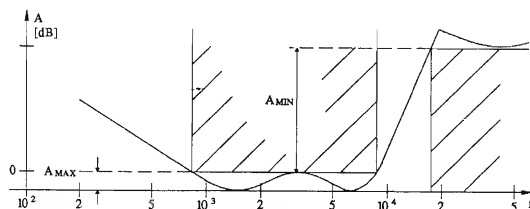


Figure 7.2.2-2 Typical IF-filter characteristic

The passband ripple (A_{MAX}) should be as low as possible. A passband ripple of 1 dB is acceptable. The higher the passband ripples becomes the more the loss in dynamic sensitivity is. The frequency characteristics of the filter shape, low-pass fraction, results from:

$$f_D = f_{IFCU} \quad A.4-1C$$

$$f_{IFCU} = |\Delta f_{TX}| + f_{OFFS} + |\Delta f_{AFC}| \quad A.4-1D$$

$$f_s = f_{TXCH} - f_{OFFS} - |\Delta f_{TX}| \quad A.4-1E$$

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The upper IF-filter cutoff frequency is approximately equal to the passband frequency, because of the strong filter slope, although the cutoff frequency usually is defined to be the 3 dB attenuation frequency.

The whole IF-filter is build of different finer types. Each filter section is separated from each other and can be designed without influencing the remaining stages. The amplifiers itself have a quite acceptable gain and phase characteristics up to 100 kHz. The filter characteristics may be modified by the choice of the component values and, if necessary, by the use of other than the shown filter types. To find the filter characteristic which matches the particular application best, some empirical evaluations will be necessary. Fig. 7.2.2-3a to 7.2.2-3e show the particular filter characteristics and Fig. 7.2.2-3f the superimposed over-all characteristic for the standard application. A quick design for other specifications may be found by scaling the component values given for the standard application accordingly.

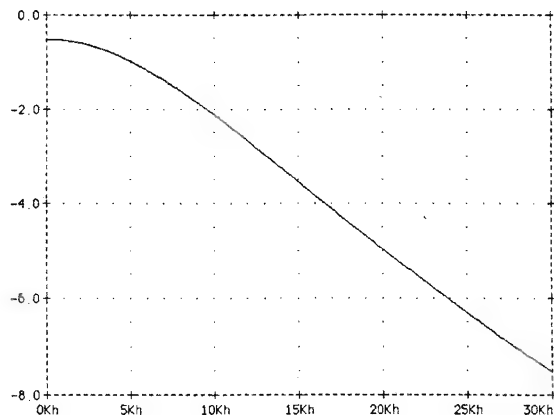


Figure 7.2.2-3a First low-pass, 1st order

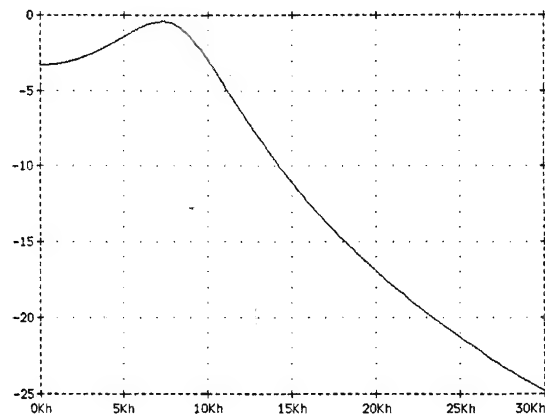


Figure 7.2.2-3b Salen & Key low-pass, 2nd order

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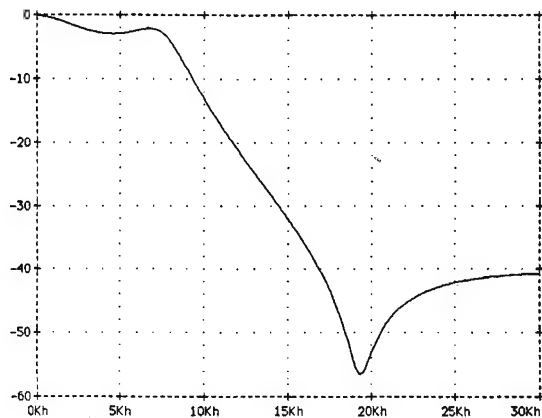


Figure 7.2.2-3c Cauer low-pass, 3rd order

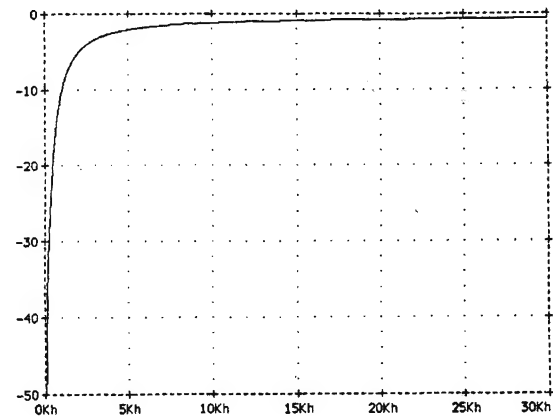


Figure 7.2.2-3d High-pass, 1st order

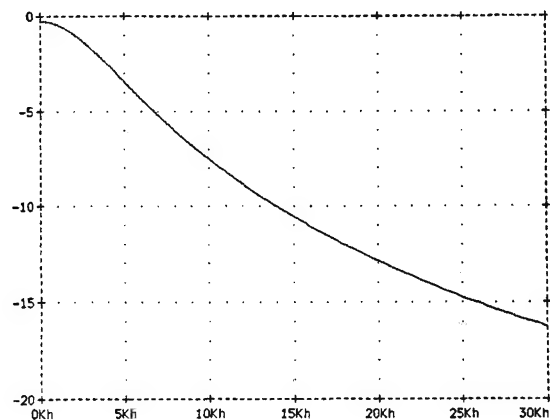


Figure 7.2.2-3e Second low-pass, 1st order

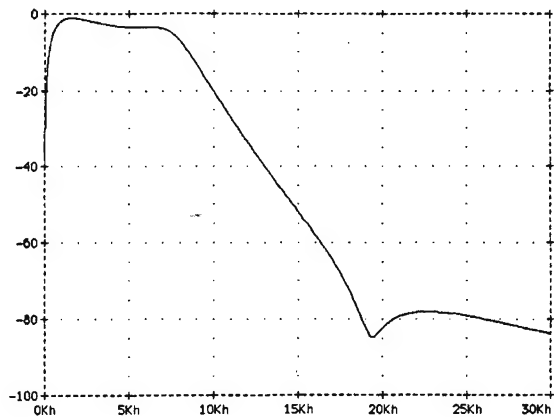


Figure 7.2.2-3f Superimposed IF-filter shape

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7.2.2.1 First Low Pass

The first low-pass filter is formed of a simple 1st order RC low-pass, which is included between the mixer output and the first IF-amplifier input, see fig. 7.2.2-4.

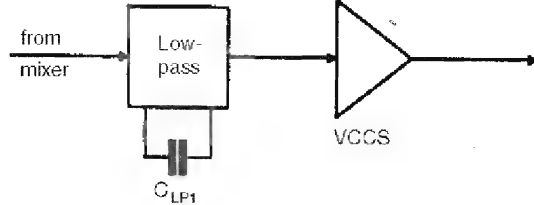


Figure 7.2.2-4 First RC low-pass block scheme

This passive low-pass attenuates any out-band intermodulation signals generated by the mixer, which may cause an overloading of the following IF-amplifiers. The cutoff frequency (f_{3dB}) is selected by a capacitance external to the UAA2033T if used, whereby it is fixed into the UAA2050T application. The UAA2050T is designed to have a 14 kHz cutoff frequency for this low-pass. To calculate the capacitance, external to the UAA2033T, for a particular cutoff frequency, the following equation is used:

$$C_{LP1} = \frac{1}{2 * \pi * 2,4 \cdot 10^3 [\Omega] * f_{3dB}} \quad A.4-2$$

The source impedance, of total 2, 4 k Ω is provided internal to the receiver. For the standard application, the cutoff frequency is chosen to be $f_{3dB} = 14$ kHz, therefore the capacitance is $C_{LP1} = 4,7$ nF. The input impedance of the following IF-amplifier needn't be taken into account. This amplifier is a differential type one, forming a VCCS (voltage-controlled-current source).

7.2.2.2 Sallen & Key Low Pass

The Sallen & Key low-pass is build around a kind of emitter follower, which serves the function of a VCVS (voltage-controlled-voltage-source) (2). The Sallen & Key low-pass itself is driven by a VCCS (voltage-controlled-current-source), see fig 7.2.2-5.

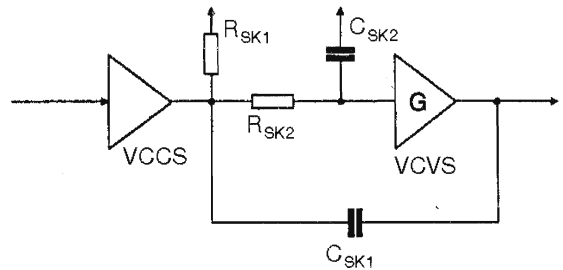


Figure 7.2.2-5 Sallen & Key 2nd order low-pass block scheme

The load resistance (R_{SK1}) of the VCCS is connected externally and serves two functions:

It will determine the operating point of the following IF stages, which is the most important effect. And it will set the DC-gain of the VCCS, which has less signification, although some gain is necessary. This is because the signal to noise ratio is much more important than the absolute gain.

The resistor is recommended to be:

$$R_{SK1} = 3 \text{ k}\Omega \quad A.4-3A$$

The DC operating point at the VCCS output will be set to a voltage of about -0,3 V, with the main positive power supply as reference. This will guarantee save operation for the following IF-stages, even at the lower limit of the supply voltage. The DC-gain thereby established is about 6 (15,6 dB).

For the standard application, the Sallen & Key filter has been chosen to be a 2nd order Chebyshev low-pass, having a passband ripple of 3 dB. The filter is formed of two capacitors and one additional resistor connected externally, see fig 7.2.3-5. The additional resistor R_{SK2} has been chosen to have the same value as the load resistor R_{SK1} , to simplify the design.

$$R_{SK2} = R_{SK1} \quad A.4-3B$$

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Its value may be modified, if the filter characteristic selected don't meet standard values for the capacitors. The effects of the input and output impedance of the VCVS needn't to be taken into account, furthermore its gain is assumed to be $G = 1$. For the shown filter type the transfer function becomes (4):

$$H_{(s)} = \frac{G * b_0}{s^2 + b_1 * s + b_0}$$

Allowing 3 dB passband ripple and Chebychev characteristic, the coefficients are found to be (normalized to a cutoff frequency of 1 rad/sec) (4):

$$\begin{aligned} b_0 &= 0,70795 \\ b_1 &= 0,64490 \end{aligned}$$

After rescaling the component values are found according to the following equations:

$$C_{SK1} = \frac{R_{SK1} + R_{SK2}}{b_1 * 2 * \pi * f_T * R_{SK1} + R_{SK2}} \quad A.4-3C$$

$$C_{SK2} = \frac{b_1}{b_1 * 2 * \pi * f_T * (R_{SK1} + R_{SK2})} \quad A.4-3D$$

The terminal frequency (f_T) is defined to indicate the end of the ripple channel and not the conventional 3 dB cutoff point. For the standard application it has been selected to be $f_T = 10$ kHz.

7.2.2.3 Cauer Filter

The main stopband attenuation is achieved with a 3rd order passive Cauer low-pass (3), which follows immediately the VCVS forming the Sallen & Key low-pass, see fig. 7.2.2-6

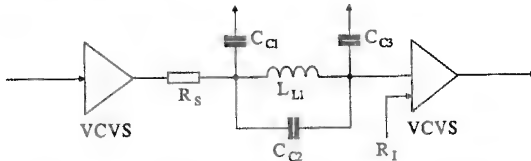


Figure 7.2.2-d 3rd order Cauer low-pass block scheme

The driving VCVS at the Sallen & Key stage can be assumed to have a very low output impedance, so the resistor in front of the Cauer filter (R_S) determines the driving impedance. The load impedance is determined by the input impedance (R_I) of the following VCVS, which is about:

$$R_I \approx 200\Omega \quad A.4-4A$$

The Cauer filter has to be designed in order to achieve an attenuation pole (f_{INF2}) at the closest adjacent channel frequency.

$$f_{INF2} = f_{TXCH} - f_{OFFS} - |\Delta f_{TX}| \quad A.4-4B$$

The standard application uses a 3rd order Cauer filter, having a passband ripple of 1,25dB. This filter type fits for a channel spacing of 25kHz and a transmitter frequency deviation of 4,5 kHz.

For example, the attenuation pole frequency calculated for the standard application is:

$$f_{INF2} = 18,25 \text{ kHz}$$

The filter coefficients are found according to the normalized attenuation pole (Ω_{INF2}), which is calculated from the attenuation pole frequency (f_{INF2}) by normalization to a reference frequency:

$$\Omega_{INF2} = \frac{f_{INF2}}{f_B}$$

The reference frequency (f_B) is normally equal to the passband frequency (end of ripple channel). The Cauer filter passband frequency selected for the standard application is:

$$f_B = 8 \text{ kHz}$$

The normalized attenuation pole for the standard application results in:

$$\Omega_{INF2} = 2,28$$

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Normalized component values may be found in (7), because of the relative high input impedance of the following VCVS, the Cauer filter can be assumed to operate in open-circuit configuration. The normalized component values for the standard application, obtained from the filter catalogue are:

$$C_{c3} = 0,9647$$

$$C_{c2} = 0,1715$$

$$L_{c2} = 1,1316$$

$$C_{c1} = 1,4717$$

The real component values are calculated according to the reference frequency and according to the reference resistor (R_s) in front of the Cauer filter.

$$L_x = L_x * \frac{R_s}{2 * \pi * f_B}$$

$$C_x = C_x * \frac{1}{2 * \pi * f_B * R_s}$$

The reference resistor, selected for the standard application, is:

$$R_s = 3\Omega$$

The component values selected for the standard application are as follows:

$$C_{c3} = 10 \text{ nF (6,4 nF calculated)}$$

$$C_{c2} = 1 \text{ nF (1, 1 nF calculated)}$$

$$L_{c2} = 68 \text{ mH (67, 5 mH calculated), Q 10 at 10 kHz}$$

$$C_{c1} = 10 \text{ nF (9, 8 nF calculated)}$$

See appendix A.4-4C for component reference to the application diagram.

7.2.2.4 High Pass

A DC blocking is achieved by the operation of a single 1st order RC high-pass. see fig 7.2.2-7.

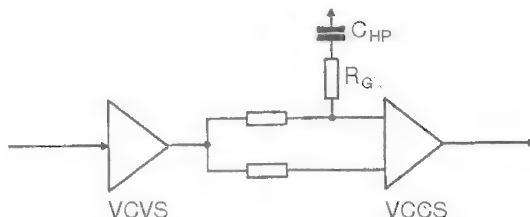


Figure 7.2.2-7 High-pass block scheme

The cutoff frequency is selected by the capacitance C_{HP} . An additional resistor (R_G) will allow to reduce the maximum gain of the high-pass. This is necessary for the standard application UAA2050T, where the gain is attenuated by $AG = 6 \text{ dB}$. The attenuation is provided, to influence the noise level at the limiter input. Especially under weak input signal conditions the AFC biasing is improved. The resistor is calculated according to the following equation:

$$R_G = \left(\frac{1}{10^{(AG*0,05)}} - 1 \right) * 10^3 [\Omega] \quad \text{A.4-5A}$$

The capacitance determining the high-pass cutoff frequency, is chosen according to:

$$C_{HP} = \frac{1}{2 * \pi * f_{3dB} * (R_G + 10 * 10^3 [\Omega])} \quad \text{A.4-5B}$$

The standard application UAA2050T and UAA2033T are designed to have a cutoff frequency of $f_{3dB} = 800 \text{ Hz}$

7.2.2.5 Second Low Pass

The IF-filtering is completed by the operation of a 1st order RC low-pass and is then supplied to the limiter, see fig 7.2.2-8.

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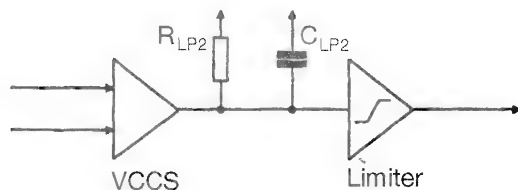


Figure 7.2.2-8 Low-pass block scheme

To introduce a new DC operating point for the following stages the low-pass is driven by a VCCS. The output load resistor (R_{LP2}) is connected externally. For save operation of the limiter, even at the lower limit of the supply voltage, the resistor is recommended to be:

$$R_{LP2} = 33 \text{ k}\Omega \quad \text{A.4-6A}$$

The capacitance (C_{LP2}) to select a specific low-pass cutoff frequency is determined by:

$$C_{LP2} = \frac{1}{2 * \pi * R_{LP2} * f_{3dB}} \quad \text{A.4-6B}$$

For the standard application the capacitance has been selected to obtain a cutoff frequency of $f_{3dB} = 4.8 \text{ kHz}$.

7.2.3 Limiter

The limiter is a multiple stage amplifier with offset compensation, providing an overall gain of about 80 dB. The two feedback loops compensate input signal offset and offsets internal to the limiter, to care for a proper limiter operation. The feedback loops are based on an integration action controller. The integration behaviour of the feedback loops are not dominant in terms of settling time. The settling time is of interest in applications, where the receiver is switched OFF and ON periodically (via the receiver enable input RE).

The capacitance for the feed back loops are selected as follows:

$$C_{L1} = 100 \text{ nF} \quad \text{A.5-1A}$$

$$C_{L2} = 100 \text{ nF} \quad \text{A.5-1B}$$

The capacitors type (especially for the second feedback loop) are recommended to have a very low leakage current, otherwise a loss in sensitivity occurs.

$$I_L \leq 0,5 \cdot 10^{-6} \text{ A} \quad \text{A.5-1C}$$

7.2.4 Data and AFC Discriminator

The operation of the data and AFC discriminator is based onto a phase-shift and multiplier arrangement see fig. 7.2.4-1.

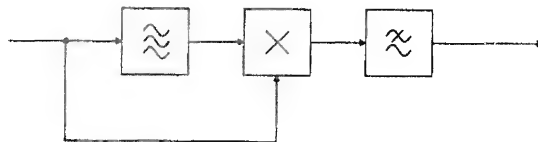


Figure 7.2.4-1 Discriminator principle

Its job is to produce an output signal that depends on the input frequency of the applied signal. The fundamental operation corresponds to the mathematics as follows.

Discriminator input signal:

$$A = a * \sin(\omega t)$$

Phase shifter output signal:

$$B = b * \sin(\omega t - \Theta(\omega))$$

The multiplier output signal thereby obtained is as follows:

$$C = c * \cos(\Theta(\omega)) - c * \cos(2 * \omega t + \Theta(\omega))$$

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A post filtering applied to the output signal has to remove the unwanted frequency component ($2 \cdot \omega\tau$). The output voltage is now a function of the input radian frequency (ω).

$$D = d \cdot \cos(\Theta(\omega))$$

The phase-shift is based on a delay circuit, which generates a constant time delay for the applied signal. The phase-shift (Θ) depends on the relationship between the time delay (t_{DLY}) and the period (T) of the input signal and can be expressed by:

$$\Theta = t_{DLY} \cdot \frac{2 \cdot \pi}{T} = t_{DLY} \cdot \omega [\text{rad}]$$

The value of the time delay determines the phase-shift and therefore the discriminator characteristic.

7.2.4.1 Data Discriminator

Fig. 7.2.42 shows the block scheme of the data discriminator and data filtering, implemented into the receiver.

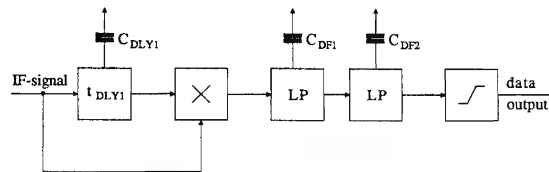


Figure 7.2.4-2 Data discriminator block scheme

The delay circuit characteristic is determined by a capacitance (C_{DLY1}) externally to the receiver. After the multiply operation a two stage low-pass filtering is applied to the signal. The integration characteristic is determined by two capacitances (C_{DF1} and C_{DF2}) external to these stages. After impulse forming by the operation of a limiter the data is available at the data output.

The delay circuit has to be designed to generate a phase-shift of 90° for the discriminator centre frequency (f_{DIS}). The discriminator centre frequency is selected to be equal to the transmitter frequency deviation (Δf_{TX}) normally, like recommended for the standard application.

$$f_{DIS} = |\Delta f_{TX}| \quad \text{A. 6-1A}$$

Varying the discriminator centre frequency will influence the duty cycle of the data output signal. The duty cycle is 40% (logic one) to 60% (logic zero), for the standard application UAA2050T and UAA2033T. This unsymmetrical duty cycle has been implemented, due to the fact that the logic zero is less sensitive (e.g. because of its lower IF-frequency). If this is undesirable, the discriminator centre frequency has to be reduced to increase the data output duty cycle (increasing C_{DLY1}). The capacitance is chosen according to the following equation:

$$C_{DLY1} = \frac{8,1 \cdot 10^{-6}}{f_{DIS}} \frac{1}{[\Omega]} \quad \text{A.6-1B}$$

The phase-shift generated is calculated as follows:

$$\Theta = f \cdot C_{DLY1} \cdot \frac{360^\circ}{3,24 \cdot 10^{-5}} [\Omega] [\text{deg}]$$

Assuming a transmitter frequency deviation (Δf_{TX}) of 4.5 kHz and a receiver offset frequency (f_{OFFS}) of 2.25 kHz the two IF-frequencies will undergo a phase-shift of 45° ($f_{IF1} = |\Delta f_{TX}| - f_{OFFS}$) and 135° ($f_{IF1} = |\Delta f_{TX}| + f_{OFFS}$).

7.2.4.2 Data Filtering

After the multiply operation of the original and the delayed signal train, a low-pass filter is provided, to attenuate all unwanted frequency components. The main unwanted frequency components start at two times the IF-frequency processed. The data filter is formed of two separate 1st order RC low-passes. They form an integration operation onto the multiplier's output signal before it is supplied to the limiter circuit. The integration characteristics are determined by two capacitances external to the receiver. Resistors, 30 k Ω each, are provided internal to the receiver.

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Each filter stage will be designed for a 1,5 dB attenuation at the cutoff frequency. The capacitances are selected according to the following equation:

$$C_{DF1} = C_{DF2} = \frac{0,644}{\pi * 30 \cdot 10^3 [\Omega] * DR}$$

A.6-2

The designer will come into conflicts if high data rates (DR) shall be processed. However, the 3 dB attenuation condition should be fulfilled even if the integration behaviour gets worse.

The filtered signal train is than supplied to a limiter amplifier to form a rectangular output signal train. The limiter amplifier is set to have a little offset, so that the signal train is limited asymmetrical. This results in an output signal duty cycle of 40 % (logic one) to 60 % (logic zero) typical, for the standard application. If undesirable, the discriminator centre frequency may be modified (see data discriminator). The signal waveforms obtained after filtering are shown into fig 7.2.4-3a and 7.2.4-3b.

Fig. 7.2.43a shows the signal train after the first data filter and fig. 7.2.4-3b after the second data filter, in relation to the data output signal train. They are measured at the UAA2033T for a 512 bps application and a RF-level of 0.3 µV.

The data output signal train contains some jitter, which is generated by the data discriminator and the way in which the signal frequencies change. Fig 7.2.3-4a and 7.2.3-4b show the typical data output jitter for the UAA2033T operating at 512 bps. fig. 7.2.4-4a and 1200 bps. 7.2.44b for a RF-Level of 0,3 µV.

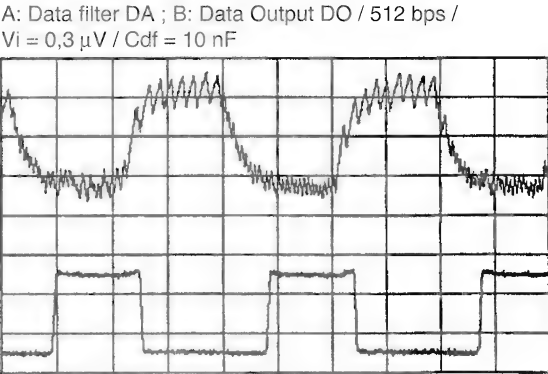


Figure 7.2.4.-3a Data filtering first stage

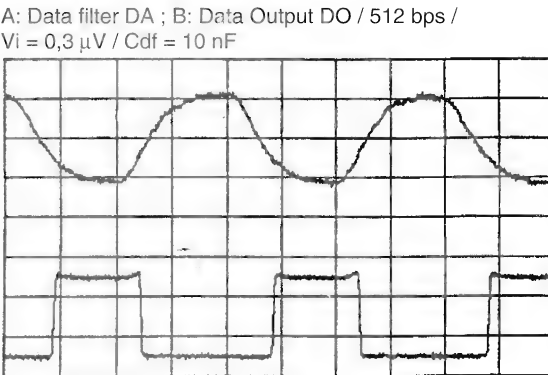


Figure 7.2.4-3b Data flitefing second stage

DISPLAY PARAMETERS

VERTICAL		HORIZONTAL	
Channel A		Sec/div	1E-03
Coupling	AC	TRIGGER	
Volts/div	.1E+00		
Channel B			
Coupling	DC	Channel	EXT
Volts/div	1E+00	Slope	POS
		Coupling	AUT

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Data output Jitter 512 bps / $V_i = 0,3 \mu\text{V}$ / UAA2033T /
Cdf = 10 nF

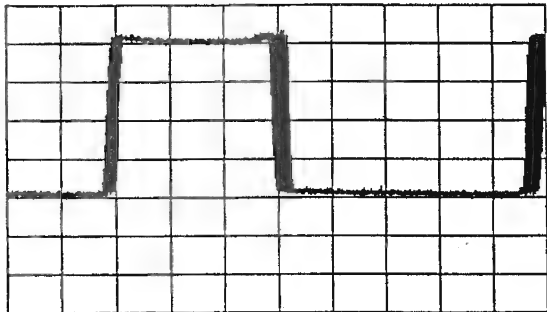


Figure 7.2.4-4a Typical data output jitter for a 512 bps application

Data output Jitter 1200 bps / $V_i = 0,3 \mu\text{V}$ / UAA2033T /
Cdf = 5,5 nF

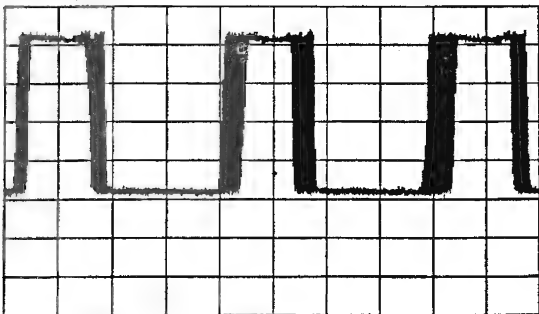


Figure 7.2.4-4b Typical data output jitter for a 1200 bps application

DISPLAY PARAMETERS

VERTICAL

Channel B
Coupling DC
Volts/div .5E+00

TRIGGER

Channel
Slope
Coupling AUT

EXT
POS
AUT

HORIZONTAL

Sec/div 5E-03

The minimum jitter is determined by the occurrence of a phase-jump during the change from one IF-signal frequency to the other. An additional jitter is generated by the 2nd harmonic frequency component in the multiplier's output signal. Proper data filtering will minimize this additional jitter. The capacitors, provided external for the data filter, may be increased to minimize the additional jitter. But this will enlarge the integration time constant and so, flatten the signal swing. The data signal ratio decreases, because of the offset at the following limiter. Furthermore a loss in sensitivity occurs, because of the increased data signal attenuation.

7.2.4.3 AFC Discriminator

An AFC function is provided to compensate drifts (e.g. temperature drift, ageing) in the frequency determining components at the receiver side and an uncertainty in the transmitter frequency. Fig. 7.2.4-6 shows the block scheme of the AFC discriminator section. It's the same phase-shift and multiplier arrangement as for the data discriminator. In addition, the discriminator output signal (DIS_{OUT}) is supplied to an integrating circuit. The integration operation is based on a capacitor (C_i), which is charged or discharged by a current (I_{CI}) controlled from the discriminator output signal. Finally, the voltage obtained at the capacitor is used to control the crystal oscillator frequency. Consequently, the AFC is based on a integral action controller, which implies a zero position error.

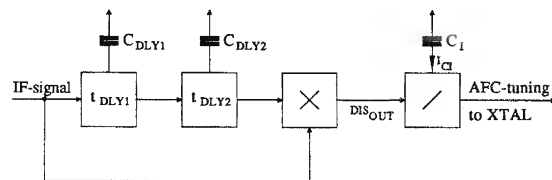


Figure 7.2.4-6 AFC discriminator block scheme

The AFC function is achieved by detection of the two nominal IF-signal frequencies. The delay circuit is designed in such a manner that the discriminator characteristics is set to have two centre frequencies (f_{DIS1} , f_{DIS2}), within the used frequency range. Each of them is related to one of the two nominal IF-signal

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frequencies generated. The principle discriminator characteristics is shown in fig. 7.2.4-7.

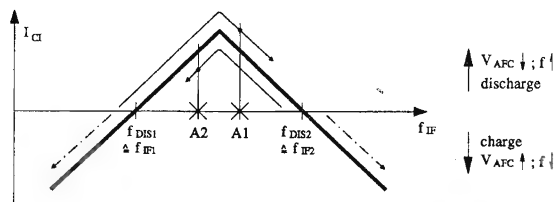


Figure 7.2.4-7 Principle AFC discriminator characteristics

If the nominal mark or space IF-frequency (f_{IF1} , f_{IF2}) is detected, no discriminator output signal occurs. Thus the capacitance charge is not altered and the crystal oscillator maintains its current frequency. The AFC discriminator will operate either at the one or at the other centre frequency (f_{DIS1} , f_{DIS2}), according to the signal frequency received. The demodulation point will jump from one to the other side and vice versa, if the mark and space are transmitted alternately.

If a frequency drift occurs, the mark and space frequencies move beside the AFC discriminator centre frequencies. For example, if it is assumed that the offset between the transmitter frequency and the multiplier frequency (mixer injection signal) is reduced, the IF-frequencies, forming the mark and space, get closer together, see figure 7.2.4-7 (solid line). One increases and the other decreases, according to the absolute value of the frequency drift occurred. Let the new IF-frequencies be A1 and A2. Consequently, the point of demodulation will move to the region, where a positive signed current (I_C) is generated. As a result the integration capacitor (C_i) is discharged and its voltage reduced. According to the crystal oscillator operation, the crystal oscillator frequency is increased, when the AFC voltage is reduced. Because the multiplier frequency tracks with the crystal oscillator frequency (1st, 3rd or 5th harmonic, depending on the multiplier application), its frequency is increased also, see figure 7.1.3-5. Discharging of the capacitance stops, when the offset between the transmitter frequency and the multiplier frequency is restored.

In the other case, if the IF-signal frequencies remove from each other (dashed line in figure 7.2.4-7), a negative signed current (I_C) is generated and the multiplier frequency is reduced, in order to restore the frequency offset necessary.

In fact, the frequency tracking at crystal oscillator level is only a fraction of the frequency tracking at mixer level ($1/5$ th, $1/3$ rd or $1/1$ th, depending on the multiplier application).

The appropriate AFC discriminator characteristic is obtained, if the delay circuit are designed to perform a phase-shift of 90° for the one and 270° for the other nominal IF-signal frequency. For the standard application the offset frequency is half the value of the transmitter frequency deviation, which is necessary for appropriate AFC operation. The upper IF-signal frequency is 3 times the value of the lower one. This exactly meets the phase-shift ratio (90° to 270°).

The delay circuit for the AFC discriminator, shown in fig 7.2.4-7, is implemented to consist of two separate stages. The first one is the one used for the data discriminator and is used for the AFC discriminator also. Its design has been discussed already, see data discriminator. The second delay stage is provided, to enlarge the phase-shift performed by the first one, to meet the requirements for the AFC discriminator. The capacitance external to the second delay circuit has to be chosen according to following equation:

$$C_{DLY2} = 2 * \frac{8,1 \cdot 10^{-6}}{f_{DIS}} \frac{1}{[\Omega]} - C_{DLY1} \quad \text{A. 6-3}$$

The overall phase-shift performed is now:

$$\Theta = f * (C_{DLY1} + C_{DLY2}) * \frac{360^\circ}{3,24 \cdot 10^{-5}} [\Omega][\text{deg}]$$

As mentioned above, the AFC discriminator output signal is then supplied to an integration section. The integration operation is formed by a capacitance (C_i), connected externally to the receiver. The regulating time for the AFC is determined by the value of the integration capacitance. Although component value drift is a slowly moving process, the value has been chosen to be:

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$$C_1 = 220\text{nF}$$

A. 6-4

This results into a regulating time of some milliseconds, which meets the requirements even if the receiver is switched ON and OFF periodical. The capacitance voltage may occur to be within the range - 0, 2 V to -1, 1V, according to the strength and direction of the drift occurred. If no receiver input signal is present, an AFC biasing circuit is provided to establish a balanced AFC operating point. The voltage established is about -0,5 V for the UAA2050T and -0,59 V for the UAA2033T.

7.3 Controlling

In this chapter all blocks will be described, which are not directly involved in the signal path:

- Current control circuit with receiver settling time and receiver power on/off
- Battery low indicator circuit
- AFC-circuit and -behaviour
- Settling time

7.3.1 Current control

The current control circuit takes care, that the receiver performance will be constant over voltage and temperature range. The circuit consists of an internal bandgap reference voltage, where all internal and external currents are derived from, and the receiver on/off switch. The value of the external reference resistor R_{CC} is determined by the design. An UAA2050T application demands

$$R_{CC} = 68\text{ k}\Omega$$

A. 7-1

while an UAA2033T application demands

$$R_{CC} = 47\text{ k}\Omega$$

A. 7-1

7.3.2 Battery low indicator

The battery low indicator output (pin BL) is "high" if the battery voltage is below the battery low indicator threshold voltage. This threshold voltage is different for both circuits.

7.3.2.1 Battery low detection UAA2050T

Due to the fact that the UAA2050T has two supply voltages depending on whether a single or a double cell operation for the low noise amplifier has been chosen, the battery low information will be detected at pin MIX₂ (pin 24). To cope with both application possibilities, the battery low indicator detection characteristics provides two threshold voltages. Figure. 7.3.2-1 shows the typical detection characteristics.

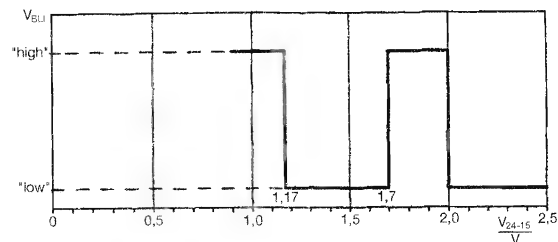


Figure 7.3.2-1 Battery low indicator detection characteristic UAA 2050T

7.3.2.2 Battery low detection UAA2033T

The UAA2033T battery voltage will be directly detected at V_P , i.d. between pins 14 and 15.

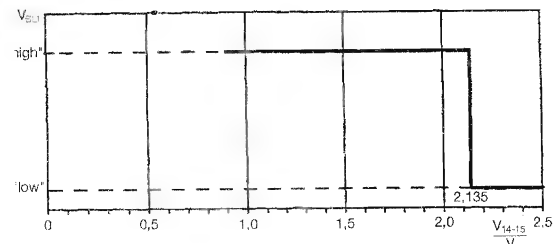


Figure 7.3.2-2 Battery low indicator detection characteristics UAA2033T

7.3.3 AFC

The integrating AFC takes care, that the frequency offset between the frequency multiplier and the wanted RF

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signal will be constant over the altering of the XTAL, supply voltage and temperature range. As shown in the figure above the AFC voltage will be derived by demodulation of the IF signal corresponding to the diagrams below. The maximum AFC range is equal to the frequency shot of the received FSK modulated signal. The AFC demodulator current and phase characteristics as a function of the IF- frequency is shown in fig. 7.3.3-2.

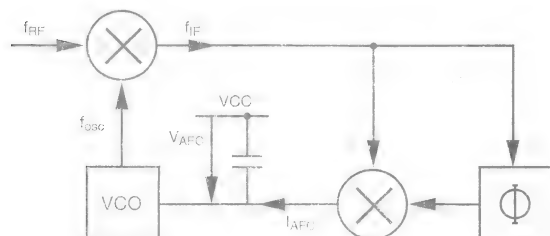


Figure 7.3.3-1 Principle block diagram of the AFC circuit

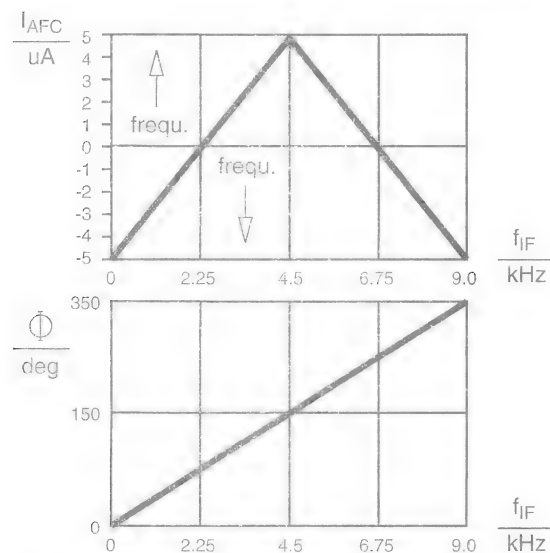


Figure 7.3.3-2 AFC demodulator current and phase characteristics

7.3.4 Receiver settling time

The settling time of the whole receiver is mainly determined by the behaviour of the crystal oscillator (rise time), the AFC-feed back loop and the limiter offset compensation. The settling time is also a function of the power down duration (receiver enable input). While the settling time only depends on the crystal rise time, when the power down duration is very short, the DC biasing settling determines the receiver settling time for long power down durations. For the latter case the standard application has been found to be operational after approximately 15 ms. For short power down durations the DC biasing is going to be stable, because of the external capacitors and little leakage currents into the receiver IC. For a power down duration of about 1 sec and less (e.g. within a POCSAG system) the standard application has been found to be operational after approximately 5 ms for the nominal AFC position. AFC locking from the nominal position to one of the two extreme positions approximately last 7 ms. The receiver will generate an output signal during settling, but valid data at the data output can be expected after completion of settling, at the earliest.

7.4 Power supply concept

Originally intended to be powered by two battery cells (2 times 1,5 V nominal) the receivers may also be supplied from one cell (1,5 V), using a voltage doubler to provide the necessary supply voltage level. Powering the receiver by two battery cells offers the longest battery lifetime, because the battery load current forced by the receiver is the lowest, in comparison to the one cell operation with voltage doubler. The battery load current forced by the receiver is equal to the receiver supply current, apart from other supply currents. Figure 7.4-1 shows the power supply principle for both receivers using a two cell powering.

Sometimes a two cell powering is undesired and a one cell powering has to be used. Providing a voltage doubler will allow to use the receivers even for this power supply concept. The UAA2050T supports this kind of powering by offering a separate power supply pin for the LNA (low noise amplifier). The LNA may be connected directly to the battery voltage ($V_B > 1\text{ V}$), whereby the remaining circuitry may be supplied from a voltage doubler

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($V_{OUT} > 1.9\text{ V}$). Because the battery low detection circuitry is connected to the LNA supply voltage, the battery voltage may be monitored directly.

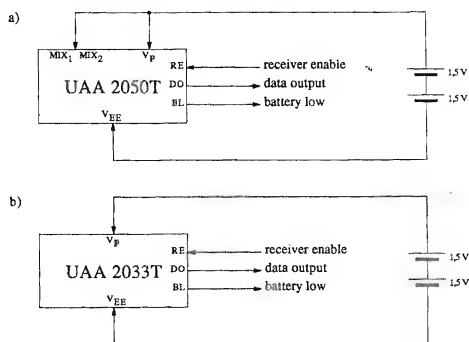


Figure 7.4- 1 Two cell power supply concept for UAA2050T (a) and UAA 2033T (b)

The UAA2033T doesn't provide two separate power supply pins and therefore has to be fully powered from a voltage doubler. The battery detection circuitry monitors the doubled supply voltage and therefore the battery voltage indirectly. The powering principle for both receivers are given in figure 7.4-2

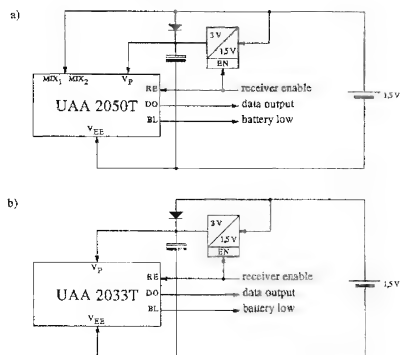


Figure 7.4-2 One cell power supply concept for UAA2050T (a) and UAA2033T (b)

During receiver operation, the voltage doubler should provide a constant supply voltage (low noise) for the receivers, in order to obtain best receiver performance. However, the supply voltage may be allowed to vary over ageing of the application, but the lower and upper supply voltage range has to be considered. The supply current for the receivers is nearly independent of the applied voltage. Since a voltage doubler will be found to sink some quiescent current, even if it is unloaded, one may demand to power down the voltage doubler during this time, to increase the battery lifetime. Such kind of operation has been suggested in fig. 7.4-2, where the voltage doubler is being powered down by the receiver enable signal (RE), together with the receiver itself. Since the receiver on/off period is about 1 sec. normally or even less (e.g. POCSAG paging at 512 bps) a smoothing capacitance may be used to hold the doubled receiver supply voltage for some time, during power down conditions. This will shorten the settling time for the voltage doubler output voltage. During long power down conditions an additional diode may be introduced to prevent the doubled receiver supply voltage dropping below the battery voltage, which will fasten the voltage doubler restart duration. While in power down mode, the receiver sinks very less current, so that the self-discharge and additional leakage currents (e.g. voltage doubler) are decisive for selection of the capacitance.

8. TEST RESULTS

The AC test results presented have been measured for UHF and VHF, using the testboards given in appendix C and additional test applications. The tuning procedure and AC test conditions applied to the applications are explained first. The test signal, used as a reference signal for the following AC tests, is a sine-wave signal with a frequency ($f_{TX-TEST}$) of 470 MHz resp. 174 MHz, modulated by a square wave, using a modulation frequency of 256 Hz (512 bps) resp. 600 Hz (1200 bps). The frequency deviation ($\Delta f_{TX-TEST}$) is 2,5 kHz, 4,0 kHz resp. 4,5 kHz.

8.1 Tuning procedure for AC tests

Figure 8.1-1 shows the measurement set-up for tuning the receiver test applications.

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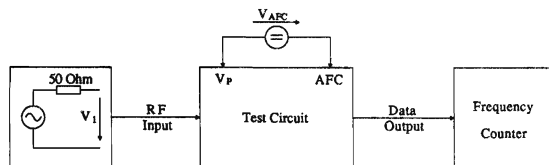


Figure 8.1-1 Measurement set-up for tuning of a test application

- A) Connect the application under test to a power supply. Apply a voltage source of $V_{AFC} = -0,5$ V using UAA2050T resp. $V_{AFC} = -0,59$ V using UAA2033T to the test point AFC (AFC, see appendix D.1 and D.2 for pin number).

Measure the oscillator frequency and tune oscillator tank circuit to set the XTAL oscillator to a frequency of:

$$f_{XOSC} = \frac{f_{TX-TEST} + f_{OFFS}}{A} \pm 100 \text{ Hz}$$

With:

$$f_{OFFS} = \frac{1}{2} * \Delta f_{TX-TEST}$$

$A = 1, 3$ resp. 5 , depending on the RF signal frequency and application. The testboards shown in appendix C use $A = 5$ for the UAA2050T at UHF and $A = 3$ at VHF for the UAA2050T resp. UAA2033T.

- B) Remove test voltage source at AFC test point and turn on the signal generator with testmodulation (RF input level = 1 mV). Note that in the following tests the RF signal generator level has to be reduced as the receiver is tuned to ensure that the peak-to-peak output voltage at the limiter input LIM IN (LIM IN, see appendix D.1 and D.2 for pin number) lies between 20 mV and 100 mV.
- C) Tune the multiplier tank to obtain peak audio level output at LIM IN (LIM IN, see appendix D.1 and D.2 for pin number).

- D) Tune the RF input matching circuit and additional the RF filter circuit following the LNA, provided in the UAA2050T, to obtain peak audio level output at LIM IN (LIM IN, see appendix D.1 and D.2 for pin number).

- E) Disconnect any frequency measurement set-up, if connected, from the oscillator circuitry. Measure the voltage at AFC (AFC, see appendix D.1 and D.2 for pin number) and check that it is within the range $-0,48$ to $-0,52$ V for the UAA2050T and $-0,58$ to $-0,60$ V for the UAA2033T. If the AFC level is found to be outside this range, than tune the oscillator tank until the AFC level comes within the limits.

- F) Check the data output DO (DO, see appendix D.1 and D.2 for pin number) signal train for correct polarity and clean wave form, using an oscilloscope.

8.2 AC test conditions

A simple digital method is used to perform an approximate bit error rate (BER) measurement. The RF signal level thereby obtained, is used as a reference level for the following AC measurements. The measurement set-up is shown in figure 8.2-1. The RF signal source is modulated by a square wave of 256 Hz (512 bps system) resp. 600 Hz (1200 bps system). Under strong signal conditions the frequency counter, connected to the data output DO (DO, see appendix D.1 and D.2 for pin number), reads the exact modulation frequency (256 Hz resp. 600 Hz). If it is assumed that the bit error duration is nearly always less than one bit length, bit errors occurring because of weak signal conditions, increase the data output frequency. For a bit error rate of 10^{-2} (1 bit error in 100 bit) the data output frequency changes from 256 Hz to 261 Hz (512 bps system) resp. from 600 Hz to 612 Hz (1200 bps system).

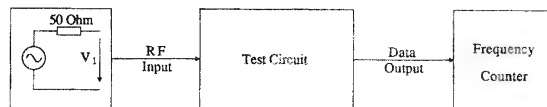


Figure 8.2-1 Sensitivity measurement set-up

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For the remaining AC tests a measurement set-up like the one shown in figure 8.2-2 has been used.

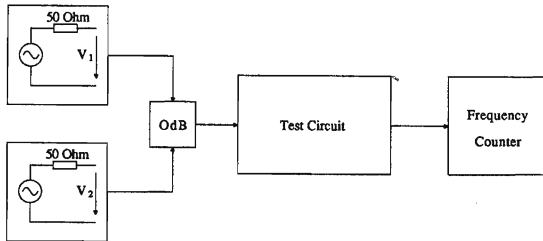


Figure 8.2-2 AC test measurement set-up

8.2.1 Sensitivity

$$G_1 \text{ testsignal} \quad f_1 = f_{\text{TX-TEST}} \quad V_1 = V_{\text{SEN-EMF/2}}$$

Data output signal corresponding to the sensitivity definition.

The signal level obtained is used as a reference signal level for the following AC measurements.

$$V_{\text{REF}} = V_{\text{SEN-EMF/2}}$$

8.2.2 Adjacent channel selectivity

$$G_1 \text{ testsignal} \quad f_1 = f_{\text{TX-TEST}} \quad V_1 = V_{\text{REF}} + 3 \text{ dB}$$

$$G_2 \text{ unmodulated} \quad f_2 = f_1 + f_{\text{TXCH}} \quad V_2 = V_1 + \alpha_{\text{AD}}$$

Data output signal corresponding to the sensitivity definition.

8.2.3 Co-channel selectivity

$$G_1 \text{ testsignal} \quad f_1 = f_{\text{TX-TEST}} \quad V_1 = V_{\text{REF}} + 3 \text{ dB}$$

$$G_2 \text{ unmodulated} \quad f_2 = f_1 \pm 3 \text{ kHz (max)} \quad V_2 = V_1 - \alpha_{\text{CO}}$$

Data output signal corresponding to the sensitivity definition.

8.2.4 Spurious response rejection

$$G_1 \text{ testsignal} \quad f_1 = f_{\text{TX-TEST}} \quad V_1 = V_{\text{REF}} + 3 \text{ dB}$$

$$G_2 \text{ unmodulated} \quad f_2 = f_1 \pm \Delta f; \quad V_2 = V_1 + \alpha_{\text{SR}}$$

$$\Delta f > 2 * f_{\text{TXCH}}$$

$$100 \text{ kHz to } 1 \text{ GHz}$$

Data output signal corresponding to the sensitivity definition.

8.2.5 Intermodulation response

$$G_1 \text{ testsignal} \quad f_1 = f_{\text{TX-TEST}} + 2 * N * f_{\text{TXCH}} \quad V_1 = V_{\text{T}} + \alpha_{\text{IM}}$$

$$G_2 \text{ unmodulated} \quad f_2 = f_{\text{TX-TEST}} + N * f_{\text{TXCH}} \quad V_2 = V_{\text{T}} + \alpha_{\text{IM}}$$

$$V_{\text{T}} = V_{\text{REF}} + 3 \text{ dB}$$

Data output signal corresponding to the sensitivity definition.

8.2.6 Blocking

$$G_1 \text{ testsignal} \quad f_1 = f_{\text{TX-TEST}} \quad V_1 = 3 \text{ dB} \mu V_{\text{EMF}}$$

$$G_2 \text{ unmodulated} \quad f_2 = f_1 \pm \Delta f; \Delta f > 4 \text{ MHz} \quad V_2 = V_{\text{BLK}}$$

Data output signal corresponding to the sensitivity definition.

8.2.7. AFC lock-in-range

$$G_1 \text{ testsignal} \quad f_1 = f_{\text{TX-TEST}} \pm \Delta f_{\text{AFC}} \quad V_1 = V_{\text{REF}} + 3 \text{ dB}$$

Data output signal corresponding to the sensitivity definition.

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8.3 Overview on test results

Receiver type	UAA 2050T				UAA 2033T		
RF test frequency $f_{\text{TX-TEST}}$	470	470	470	174	174	174	MHz
RF deviation Δf_{TX}	4,5	4,0	4,5	4,5	4,5	2,5	kHz
RF channel spacing f_{TXCH}	25	20	25	25	25	12,5	kHz
Data rate DR	512	512	1200	512	512	512	bps
Sensitivity $V_{\text{SEN-EMF}/2}$	0,18	0,18	0,25	0,14	0,21	0,50	μV
Adjacent channel rejection α_{AD}	67	67	65	67	67	67	dB
Co-channel selectivity α_{CO}	-5	-5	-5	-5	-6	-7	dB
Spurious response α_{SR}	58	58	58	58	58	50	dB
Intermodulation response α_{IM}	60	60	57	60	55	50	dB
Blocking V_{BLK}	83	83	80	83	82	1*	$\text{dB}\mu\text{V}$
AFC range Δf_{AFC}	3,0	2,7	3,0	3,0	2,0	2,0	kHz

1* Value not measured

Note: The values listed above represent typical case.

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9. PCB LAYOUT HINTS

In general one should notice that the realizing an RF receiver is a hard job to do, when the frequency approaches UHF. Especially applications operating at UHF, which require minimum space (e.g. pager) and demand a careful layout. It isn't unusual that several attempts are necessary to find an acceptable layout. Hints given in the following sections may be helpful to avoid major problems concerning the layout.

9.1 Parasitic coupling between the RF circuits

Since the wanted signal (receive frequency) and the mixer injection signal (provided by the frequency multiplier) are almost at the same frequency, there is no suppression possible, which avoids the receipt of the injection signal at the mixer input itself. The injection signal may be fed into the mixer input via the antenna or parasitic coupling somehow. In this case, the mixer mixes two signals with the same frequency. According to the phase displacement, an offset voltage at the mixer output results. This offset voltage is undesirable and will influence the biasing of the whole IF section. Sometimes it becomes difficult to avoid an offset, because of minimum space requirements. A rule of thumb is that an offsets of about 50 mV has been found not to cause problems.

Magnetic coupling of the rf-filter components can be minimized by positioning the inductances in a way that the magnetic fields produced, are at an angle of 90° to each other. The area enclosed by the components being in resonant has to be kept very small. Notice that the signal power within the resonant circuit is Q^2 times greater than the driving power. So, the components being in resonance should be placed as close together as possible.

Capacitive coupling can be minimized by avoiding crossings of rf interconnections with common lines (i.e. ground). In addition there should be proper spacing between different RF interconnections.

In general the RF circuits should be built up as compact and close to the corresponding IC pins as possible. This minimizes the parasitic reactances and the coupling with the IF and data processing sections. Avoiding ground

plates under the rf interconnections gives the opportunity to use larger capacitances for the RF circuits offering easier tuning and temperature drift compensation of the RF section.

A simple procedure may help to locate parasitic couplings. Since the parasitic couplings will produce an offset, the IF filter biasing can be monitored to identify parasitic couplings. The IF filter biasing (do voltage) may be monitored at IFF₁ (IF-filter input, see appendix D.1 and D.2 for pin number). For example, to monitor the dc voltage while the frequency multiplier outputs are shortened and not shortened may indicate an offset and its source.

9.2 Parasitic coupling between the front- and backend

The RF sensitivity may be reduced by coupling of frontend related components with backend related components. Special care should be taken on the components related to the sections following the limiter, because these sections produce signals with fast transitions.

To monitor the IF signal at the limiter input LIM IN (IF filter output, limiter input, see appendix D.1 and D.2 for pin number) may help to check for undesired cross couplings, using an oscilloscope. A coupling between the data discriminator and the RF section or between the data output and the RF section is characterized by an overshoot resp. a fade at every transition of the data output signal. An instability or probably an oscillation of the IF section may result from a coupling between the limiter and RF section.

Further investigation, using a spectrum analyzer to monitor the IF spectrum, may identify a coupling between the discriminator delay stage and the RF section. The IF spectrum than found contains harmonics of the wanted signals, especially the second. The 2nd order harmonics will be found to be nearly independent from the input level. To simplify the interpretation of the IF spectrum, one may transmit only one carrier ($f_{TX} - |\Delta f_{TX}|$ or $f_{TX} + |\Delta f_{TX}|$).

All these parasitic effects can be minimized by avoiding crossing of RF interconnections with IF interconnections or the discriminator interconnections. In addition the

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signal ground for the RF, IF and the discriminator section should be separated from each other before they meet. This should be as close as possible to the signal ground connection VP (positive power supply, see appendix D.1 and D.2 for pin number) of the IC.

9.3 Parasitic coupling influencing the IF filter

Similar parasitic couplings to the ones mentioned between the frontend and the backend (see 9.2) may occur within the backend. Since the signal level obtained in the IF filter section may be very small, parasitic coupling between the IF filter and the limiter or the discriminator or the data output may influence the IF filtering behaviour. They can be identified by the some methods described earlier (see 9.2).

9.4 AFC

The capacitance attached to the pin AFC (see appendix D.1 and D.2 for pin number) used for afc integration should have a separate ground interconnection to the signal ground VP (positive power supply, see appendix D.1 and D.2 for pin number). Because any voltage drop produced at this interconnection will directly tune the XTAL oscillator and therefore may appear as an additional undesired frequency modulation.

9.5 Data output

Apart from the receiver enable input (RE) the data output (DO) (see appendix D.1 and D.2 for pin number) interconnection should be as short as possible, since these lines are the ones with the largest voltage swing appearing. Operating the receiver at UHF, an additional resistor introduced within the data output interconnection may be helpful to reduce a cross coupling from the data output signal. A resistor of 100 k Ω has been found to operate proper together with the CMOS PCA5000T paging decoder. The resistor has to be provided close to the data output pin DO (see appendix D.1 and D.2 for pin number).

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Pager receivers

Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

APPENDIX

A. Formulae symbols

α	= Crystal pulling ratio
ΔA	= Relative frequency drift over ageing (per year)
Δ_{AFC}	= AFC range
Δf_{LOCK}	= Maximum AFC lock-in-range
Δf_{RX}	= Receiver frequency error
Δf_{TX}	= Transmitter frequency deviation
ΔT	= Relative frequency drift over specified temperature range
Θ	= phase-shift
$\Theta(\omega)$	= phase-shift as a function of ω
A	= Receiver device dependent
A_G	= Gain attenuation [dB]
b_0	= Chebychev coefficient
b_1	= Chebychev coefficient
C_{0XL}	= Static crystal capacitance
C_1	= Matching circuit capacitance
C_{1XL}	= Dynamic crystal capacitance
C_2	= Matching circuit capacitance
C_{AFC}	= AFC pulling capacitance
C_{COM}	= Compensation capacitance
C_{COUP}	= Coupling capacitance
C_{EXT}	= Tank circuit capacitance
C_{IN}	= Receiver input capacitance
C_{IM}	= Multiplier circuit capacitance internal
C_L	= Effective AFC pulling capacitance
C_P	= Matching circuit capacitance
C_{TOT}	= Total matching circuit capacitance
C_{PAR}	= Parasitic capacitances
df_c	= Crystal capacitive pulling range
df_L	= Crystal inductive pulling range
DR	= Data rate
f_{3dB}	= Cutoff frequency
f_D	= Upper passband limit frequency
f_{DIS}	= Discriminator center frequency
f_{IF1}	= Lower IF tone frequency (logic zero normally)
f_{IF2}	= Upper IF tone frequency (logic one normally)
f_{IFUC}	= Upper IF-filter cutoff frequency
f_{INF2}	= Attenuation pole frequency
f_{OFFS}	= Receiver frequency offset
f_{RX}	= Receive centerfrequency
f_S	= Stopband limit frequency
f_{SXL}	= Crystal series resonant frequency, without load
f_T	= Terminal frequency (End of ripple channel)

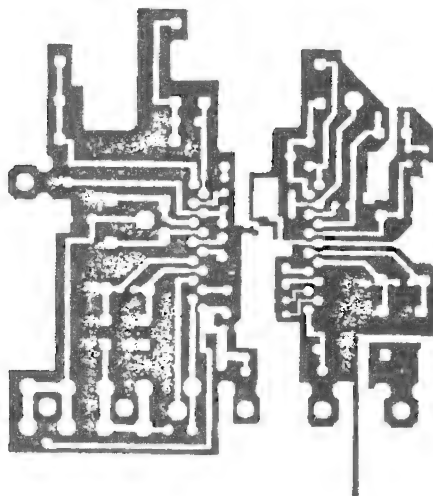
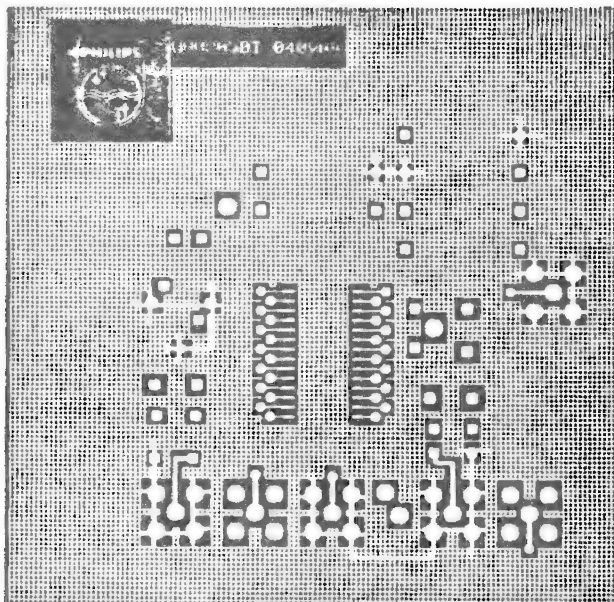
f_{TX}	= Transmitter center frequency
f_{TXOFS}	= Transmitter frequency offset
f_{XOSC}	= Receiver crystal oscillator frequency
f_{TXCH}	= Transmitter channel spacing
I_L	= Capacitance leakage current
IMR	= Impedance matching ratio
L_{ANT}	= Antenna inductance
L_M	= Tank circuit inductance
N	= Pager operation in years
P_{MIN}	= Minimum crystal pullability
P_{MAX}	= Maximum crystal pullability
R_{ANT}	= Antenna impedance real part
R_G	= Resistor for gain attenuation
R_i	= Input impedance of the following stage
R_{IN}	= Receiver input impedance real part
R_{LP2}	= Load resistor at amplifier output
R_S	= Source impedance
S_{df}	= Relative frequency difference
S_{RX}	= Relative receiver frequency error
S_{RXMAX}	= Maximum tolerable relative receiver frequency error
S_{TX}	= Relative transmitter frequency error

Pager receivers

Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

B. PCB Layout Testboard

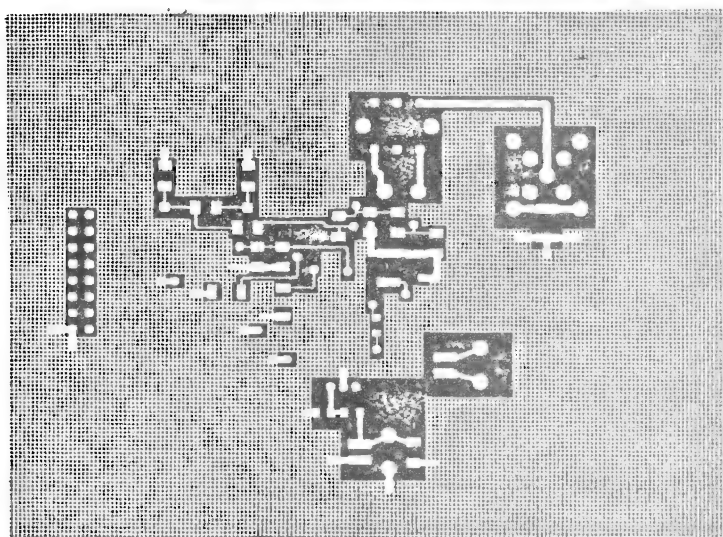
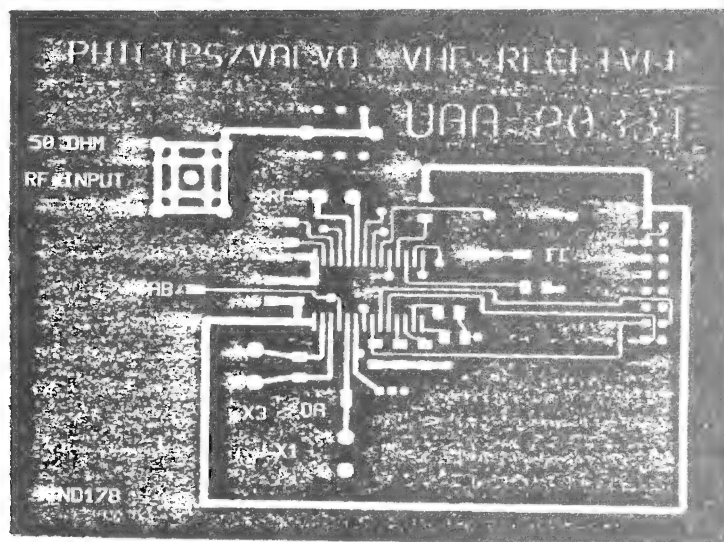
B.1 PCB Layout Testboard UAA2050T



Pager receivers

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B.2 PCB Layout Testboard UAA2033T



Pager receivers

Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

C. Pinning

C.1 UAA2050T

pin	mnemonic	description
1	IFF ₂	If-filter 2
2	IFF ₁	If-filter 1
3	AFC	afc (test point)
4	OSC IN	oscillator input
5	OSC AFC	oscillator afc pulling
6	OSC OUT	oscillator output
7	VP	positive supply voltage
8	MC ₁	multiplier coil 1
9	MC ₂	multiplier coil 2
10	AFCD	afc delay
11	DEMOKD	demodulator delay
12	DATF ₁	data filter 1
13	DAT F ₂	data filter 2
14	DAT OUT	data output
15	VEE	negative supply voltage
16	RE	receiver enable input
17	CC	current control input
18	BL	battery low indicator output
19	PREAMP ₁	pre-amplifier input 1
20	PREAMP ₂	pre-amplifier input 2
21	LC ₂	limiter decoupling 2
22	LC ₁	limiter decoupling 1
23	MIX ₁	mixer input 1 (pre-amplifier output)
24	MIX ₂	mixer input 2 (pre-amplifier output)
25	LIM IN	limiter input(testpoint)
26	IFF ₅	if-filter 5
27	IFF ₃	if-filter 3
28	IFF ₄	if-filter 4

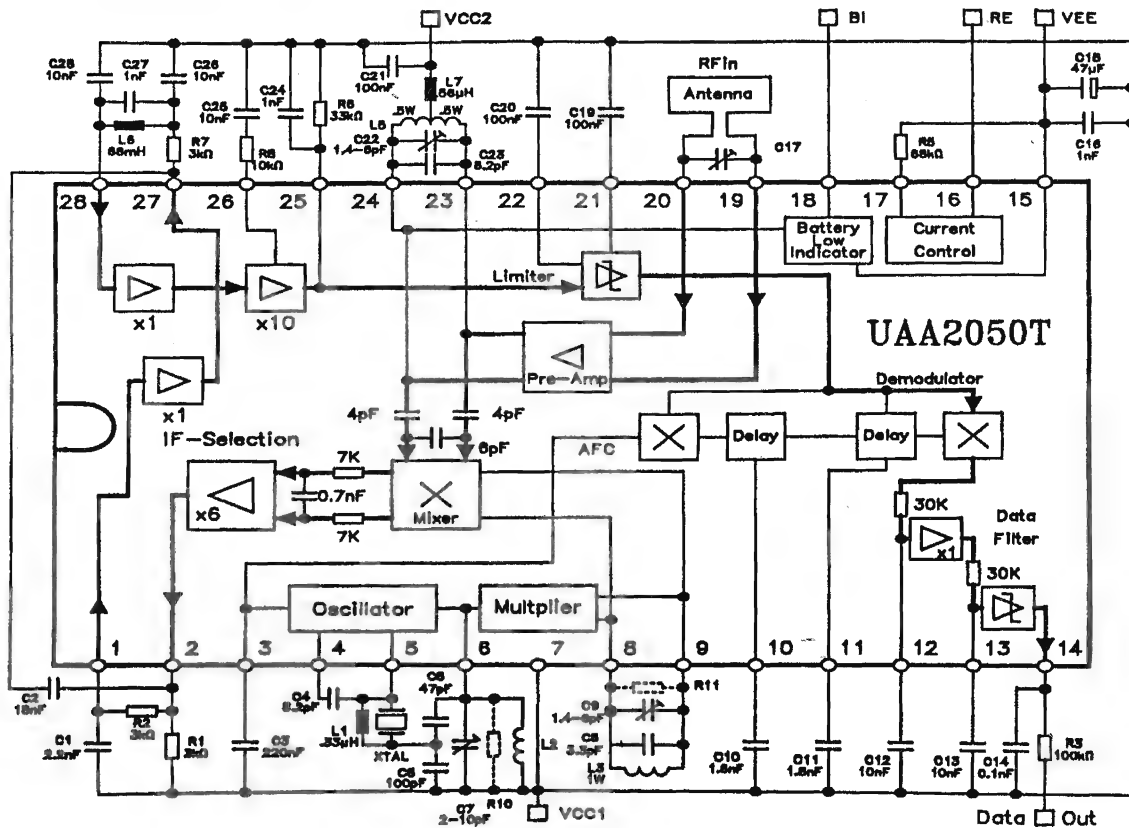
C.2 UAA2033T

pin	mnemonic	description
1	LC ₂	limiter decoupling 2
2	LC ₁	limiter decoupling 1
3	IFF ₅	if-filter 5
4	CC	current control input
5	LIM IN	limiter input (testpoint)
6	IFF ₄	if-filter 4
7	IFF ₃	if-filter 3
8	IFF ₁	if-filter 1
9	MIX ₂	mixer input 2
10	MIX ₁	mixerinput 1
11	IFF ₂	if-filter 2
12	MIX _B	mixer output B
13	MIX _A	mixer output A
14	VP	positive supply voltage
15	VEE	negative supply voltage
16	MC ₂	multiplier coil 2
17	MC ₁	multiplier coil 1
18	AFC	afc (test point)
19	OSC OUT	oscillator output
20	OSC IN	oscillator input
21	OSC AFC	oscillator afc pulling
22	BL	battery low indicator output
23	RE	receiver enable input
24	DAT OUT	data output
25	DAT F ₂	data filter 2
26	DAT F ₁	data filter 1
27	DEMOKD	demodulator delay
28	AFCD	afc delay

Pager receivers

Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

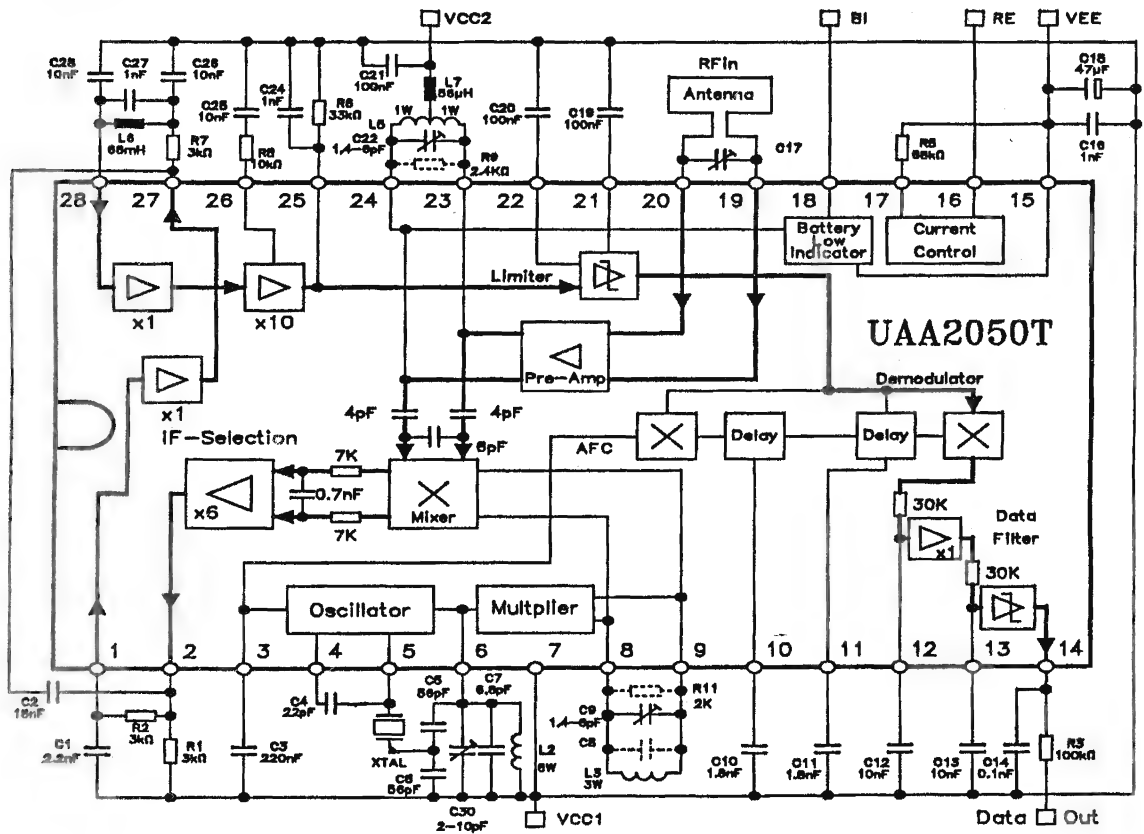
D.1 UAA2050T UHF application



Pager receivers

Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

D.2 UAA2050T VHF application



Digital Paging VHF/UHF Receivers UAA2050T and UAA2033T

Pager receivers

UAA2080T VHF/UHF paging receiver

Summary:

This report is intended to provide application support for designing paging receivers with the UAA2080 integrated circuit. It contains worked-out examples of application circuits at three widely differing frequencies of 173, 288 and 470 MHz. The necessary theory and simulation results have been included, to enable the designer to operate at other frequencies. Designing receivers usually require a trade off between sensitivity and spurious rejection. Fortunately, with the novel features of the UAA2080T, the decrease in sensitivity (around 1dB only) is marginal compared to the large spurious rejection that can be attained (about 70 dB at 173 MHz), when measured at multiples of the crystal frequency.

The first chapter contains the three application circuits along with a list of components, and hints regarding tuning and PCB (printed circuit board) layout. The remaining chapters provide the necessary theory along with worked-out application examples for the three selected frequencies. Chapter 2 gives complete theoretical background into designing the UAA2080 Colpitts Oscillator using a crystal. However, the detailed equations may not be required if the crystal specifications and the application circuit are adhered to. Chapter 3 covers the design of the frequency multiplier. The phase-shifter to obtain quadrature phase between the I and the Q channels, is described in chapter 4. Graphs of simulated component values are given so that quadrature phase can be obtained for a required frequency of operation. Chapter 5 gives useful equations for input noise and output power matching for the low-noise RF amplifier. Formulas to calculate intercept point and intermodulation immunity are included. Noise, impedance and gain characteristics of the RF amplifier are included to aid in proper circuit design. The mixer and IF stages, including the demodulator, are described in chapter 6. These stages, which are fully integrated, require little or no application circuit designing.

Pager receivers

UAA2080T VHF/UHF paging receiver

INTRODUCTION

1.1 UAA2080T Advanced Paging Receiver Architecture

The UAA2080 is a single-chip radio receiver for VHF and UHF wide-area paging transmissions up to 512 MHz with FSK data rates up to 2400 baud. It integrates low-pass filters which perform all adjacent channel selectivity. Off-chip passive components are required only for local oscillator frequency determination and RF filtering. At 1200 baud, the IC gives -126 dBm sensitivity, 70 dB adjacent channel immunity and 60 dB intermodulation (IEC method) to satisfy POCSAG pager requirements.

The spurious rejection is close to 70 dB for VHF applications.

A zero intermediate frequency (IF) receiver is used to make channel filtering possible with low-power integrated low-pass filters. This is a single superhetrodyne receiver in which the nominal IF is zero. To separate the signal below and above the carrier frequency, two IF channels are used that carry signals mixed down from RF in phase quadrature. Fig. 1.0 shows the receiver architecture. The pager antenna is coupled to the RF amplifier amplifier input, and the demodulated digital output is connected to a CMOS decoder IC (e.g. PCF5001T for the POCSAG code) designed for the paging format in use.

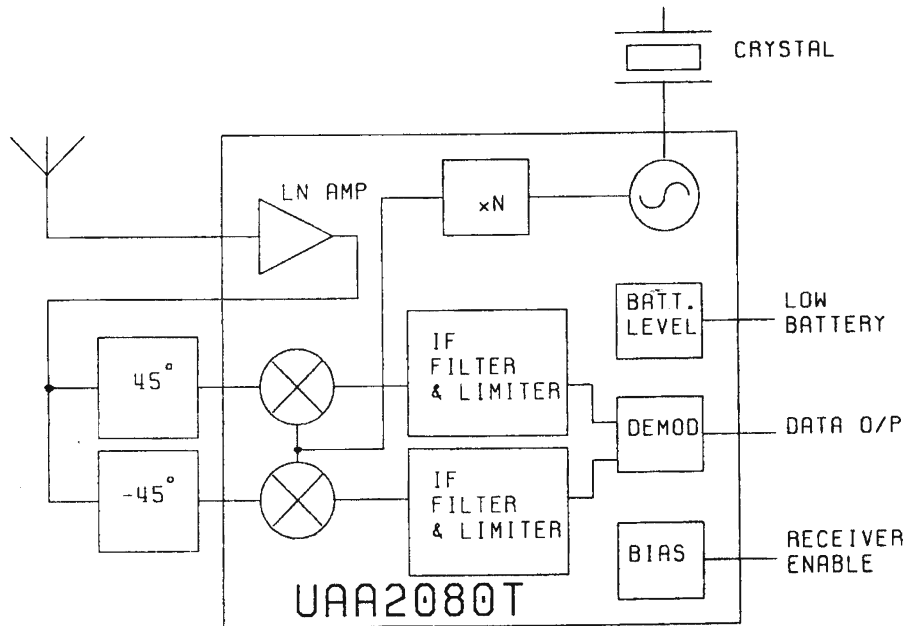


Figure 1.0 UAA2080 Pager Receiver Architecture

Pager receivers

UAA2080T VHF/UHF paging receiver

Figure 1.1 gives further details of the UAA2080. The RF amplifier is a fully differential cascode stage, driving off-chip LC networks to apply quadrature phase shifted RF signals to the two mixer inputs. The common-base input Gilbert-Multiplier mixers provide a controlled load impedance to the quadrature phase-shift network. A frequency multiplier derives the local oscillator (LO) signal from a fixed crystal oscillator for single channel operation. External resistors set the current in the crystal oscillator, frequency multiplier and RF amplifier stages to

suit the operating frequency. The mixer outputs feed two identical signal channels in phase quadrature. In each channel a single-pole RC filter precedes the first low-noise amplifier. Together with the following fully differential Sallen and Key stage this gives a third order filter that protects the following gyrator filter from strong adjacent channel signals. The unwanted dc offset from the mixer and succeeding stages is removed by a differential input single-ended output high-pass filter.

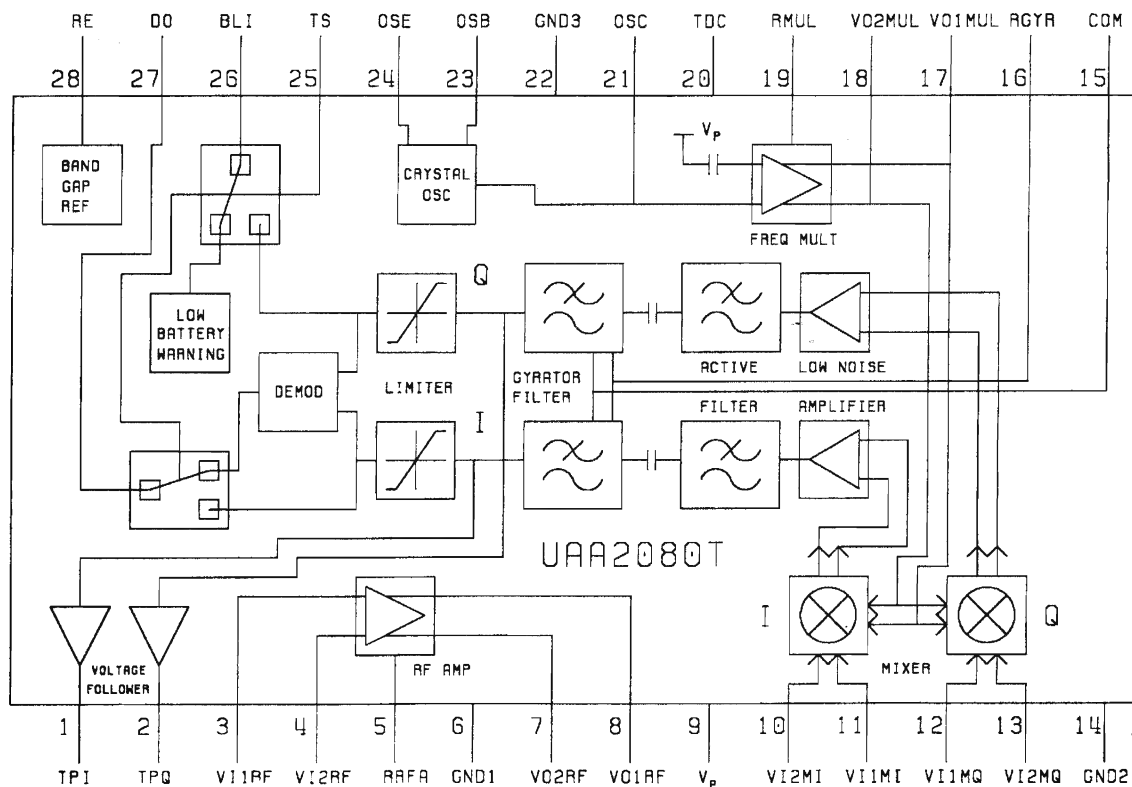


Figure 1.1 UAA2080T Pager Receiver internal blocks

Pager receivers

UAA2080T VHF/UHF paging receiver

The main channel filter is a gyrator-capacitor implementation of a seven-pole elliptic filter. The elliptic filter minimises the total capacitance required for a given selectivity and dynamic range. Two-input-one-output linearised tunable transconductors are used in a leap-frog topology. Normalised to a 150 kΩ gyration resistance (set by a 47 kΩ external resistor for 25 kHz or 20 kHz channel spacing, so that the IF bandwidth is 9 kHz), each filter consumes 3 µA. An 100 kΩ external resistor lowers the cut-off frequency for use with 12.5 kHz channel spacing. Base current compensation reduces offset voltage build-up in the filter, and a voltage limiter gives rapid recovery from overload. The following limiter amplifier provides 75 dB small signal gain before the demodulator. It contains fully differential dc block circuits that provide 150 Hz cutoff frequencies with 330 pF capacitors. This leads to the dc blocks using only 15% of the total on-chip capacitance. This dc coupled differential structure gives short turn-on times despite the long RC time constants.

The demodulator is a 2 µA/gate current-mode logic circuit that detects the relative phase of the I and the Q channel signal at each zero crossing in either channel. If the I channel signal leads the Q channel, the FSK tone frequency lies above the LO frequency (POCSAG data '0'). If the I channel lags the Q channel, the FSK tone lies below the LO frequency (POCSAG data '1'). The demodulator uses all the information contained in the hard limited IF signal to give a 80% call success rate with the PCF5001T decoder when the S/N at the limiter input is about 1dB. The CMOS compatible data output buffer has controlled output slew rate and a constant drive current to minimise interference with low-level signals on chip. A battery-level indicator detects supply voltages below 2.05 V and gives a warning logic output to the decoder IC. The UAA2080 can be powered up and down in 5 ms by enabling and disabling the main bandgap voltage reference that biases the entire chip. (Paging codes such as POCSAG allow the receiver to be turned off periodically to conserve the battery.)

Typical performance at 470 MHz (from a 50 Ω source) measured with 4 kHz deviation 1200 baud PRBS

Data Rate	1200 baud (250 µs rise/fall time for frequency modulation)
Channel Spacing	20 kHz-30 kHz
Sensitivity	-126 dBm at 80% call success rate using PCF5001T decoder
Adjacent Channel Rejection	70 dB
Intermodulation rejection, IM3	60 dB
Spurious Rejection	> 60 dB at multiples of crystal frequency
Frequency Offset	better than +/- 2.5 kHz for 3 dB loss in sensitivity
Blocking (1MHz off)	82 dB
Power Consumption	2.7 mA at 2 V typical
Power Down Current	< 1 µA typical

Pager receivers

UAA2080T VHF/UHF paging receiver

1.2 UAA2080T Pin Description

SYMBOL	PIN	DESCRIPTION
TPI	1	IF test point (I channel)
TPQ	2	IF test point (Q channel)
VI1RF	3	low-noise RF amplifier input 1
VI2RF	4	low-noise RF amplifier input 2
RRFA	5	external emitter resistor of low-noise RF amplifier
GND1	6	ground 1 (0V) (ground for IF LNA, and substrate)
VO2RF	7	low-noise RF amplifier output 2
VO1RF	8	low-noise RF amplifier output 1
VP	9	2.05–3.5V positive supply voltage, Vcc
VI2MI	10	I-channel mixer RF input 2
VI1MI	11	I-channel mixer RF input 1
VI1MQ	12	Q-channel mixer RF input 2
VI2MQ	13	Q-channel mixer RF input 1
GND2	14	ground 2 (0V) (ground for mixers)
COM	15	gyrator filter resistor (common line)
RGYR	16	gyrator filter resistor
VO1MUL	17	frequency multiplier output / mixer LO input 1
VO2MUL	18	frequency multiplier output / mixer LO input 2
RMUL	19	external emitter resistor for frequency multiplier
TDC	20	dc test point (not to be connected)
OSC	21	oscillator cascode output
GND3	22	ground 3 (0V) (ground for IF stage)
OSB	23	oscillator base
OSE	24	oscillator emitter
TS	25	test switch (selects DO and BLI, or I&Q limiter o/p)
BLI	26	battery low indicator / limiter Q output
DO	27	data output / limiter I output
RE	28	receiver enable

Pager receivers

UAA2080T VHF/UHF paging receiver

1.3 Principle of Operation

The UAA2080T paging receiver accepts FSK (frequency shift keyed) signal from the antenna, and provides the demodulated binary data at its data output terminal. The application circuit is designed to receive only a single channel i.e. at a fixed carrier frequency. The data rate, modulation frequency deviation, and transmitter-receiver frequency offset should be such that the signal power lies within ± 10 kHz of the receiver LO frequency. This corresponds to the 10 kHz maximum upper cutoff frequency that can be set for the IF filter of the UAA2080T.

Ideally, the received signal's carrier frequency is shifted down to zero hertz by multiplying by a LO (local oscillator) signal having the same frequency as the carrier. This means that ideally the original signal spectrum has been folded about the carrier frequency, that has further been translated down to zero Hertz. The received signal is split into two channels (I and Q) with a relative phase difference of 90° , prior to the multiplication with the common LO. The I and the Q IF signals that emerge after multiplication by the common LO, maintain the same relative phase. In order to have positive and negative phase differences for data one and data zero respectively, the frequency offset between the carrier and the LO, must be less than the modulation frequency deviation, as explained below.

The received signal is

$\cos(\omega_o - \Delta\omega_1)t$ for data one, and $\cos(\omega_o + \Delta\omega_0)t$ for data zero. ω_o is the carrier frequency. $\Delta\omega_1$ is the deviation for data one, and $\Delta\omega_0$ is the deviation for data zero.

After phase splitting the received signal into the I and the Q channels, the signals become

$\cos[(\omega_o - \Delta\omega_1)t + \theta_I]$ for data one, and
 $\cos[(\omega_o + \Delta\omega_0)t + \theta_I]$ for data zero, in the I channel, and
 $\cos[(\omega_o - \Delta\omega_1)t + \theta_Q]$ for data one, and
 $\cos[(\omega_o + \Delta\omega_0)t + \theta_Q]$ for data zero, in the Q channel.

θ_I and θ_Q are the phase shifts introduced in the I and the Q channels respectively, during phase splitting of the received signal.

The LO signal is $\cos[(\omega_o + \omega_{\text{offset}})t]$, where ω_{offset} is the offset (either positive or negative) from the carrier ω_o .

After multiplication with the LO, two IF signals emerge. The upper IF signals are in the RF band, and are filtered off. The lower IF signals are in the audio band. They are as follows.

$\cos[(\omega_{\text{offset}} + \Delta\omega_1)t - \theta_I]$ for data one, and
 $\cos[(\omega_{\text{offset}} - \Delta\omega_0)t - \theta_I]$ for data zero, in the I channel, and

$\cos[(\omega_{\text{offset}} + \Delta\omega_1)t - \theta_Q]$ for data one, and
 $\cos[(\omega_{\text{offset}} - \Delta\omega_0)t - \theta_Q]$ for data zero, in the Q channel.

The relation $2\cos(A)\cos(B) = \cos(A+B) + \cos(A-B)$ is used to obtain the above result. The term $\cos(A-B)$ corresponds to the lower IF in the audio band, and the term $\cos(A+B)$ corresponds to the upper IF in the RF band.

The I and the Q channel audio IF signals are represented as phasors in Fig. 1.2. During data '1' bit period, the phasors revolve anticlockwise at an angular speed of $\Delta\omega_1 + \omega_{\text{offset}}$, while during the data '0' bit period they revolve clockwise at an angular speed of $\Delta\omega_0 - \omega_{\text{offset}}$. The instantaneous I and Q channel IF voltages are the projections of their respective phasors on the X-axis. Whenever a phasor coincides with the positive or negative Y-axis, the instantaneous voltage of its channel is zero, and corresponds to an edge in the hard-limited waveform at the output of the limiter. During data '1' the I channel edges lead the Q channel edges by $\theta_Q - \theta_I$ degrees, because the I channel phasor crosses the Y-axis first (due to anticlockwise rotation). During data '0' the Q channel edges are ahead by the same amount i.e. $\theta_Q - \theta_I$ degrees, since now the Q channel phasor crosses the Y-axis first (due to clockwise rotation). The data demodulator is simply a lead-lag phase detector that updates the data output at every zero-crossing (i.e. edge) in each channel. For maximum sensitivity, $\theta_Q - \theta_I$ should be 90° degrees, so that the zero in one channel occurs with the peak in the other. The magnitudes of the phasors (i.e. amplitudes of I and Q channel signals) should also be equal for better sensitivity.

It is important to note that the phasors must rotate in opposite directions for data '1' and data '0' in order to have a change in the polarity of the relative phase. This implies that $|\omega_{\text{offset}}| < \Delta\omega_1$ and $|\omega_{\text{offset}}| < \Delta\omega_0$ must always hold i.e. the received signal frequency must always cross the LO frequency during 1-0 or 0-1 data transitions.

Pager receivers

UAA2080T VHF/UHF paging receiver

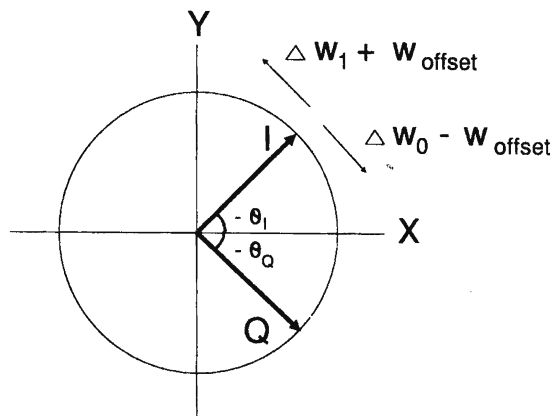


Figure 1.2 I and Q channel phasor representation

1.4 Receiver Tuning Procedure

a) Coarse tuning of the crystal

The three application circuits which are given in the next section, are to be tuned as follows. The signal generator (50 Ω source) is connected to the RF input of the receiver, and the frequency is kept at the nominal receiver frequency. The RF signal amplitude is initially kept very large, at about 50 mV. The audio IF signal at TPI or TPQ is displayed on an oscilloscope (time base at 200 μ s/division). The crystal is tuned (by C16 or C17) till a signal of approximately 2-4 kHz is observed. The amplitude could be very small, so the voltage setting on the oscilloscope should be 1-5 mV/division. If a damping resistor R6 is used, then it must be kept at the maximum value.

b) Tuning all tank circuits

After the coarse tuning of the crystal, the receiver's LO frequency is within a few kHz of the correct frequency, and therefore all the tank circuits can now be tuned. All other tuning capacitors are carefully adjusted in order to maximise the IF amplitude. The signal generator level is decreased and adjusted so that the IF amplitude is always less than 25mV (this avoids gain compression in the IF signal path). For the 470 and 288 MHz applications, C12 will have a large range over which the

IF amplitude remains maximum. This is due to overdrive signal level at pin 21. Proper tuning of C12 is given below under the section on Spurious Rejection.

c) Fine tuning of the crystal

The crystal is again tuned till there is no signal displayed, or the signal frequency is very small (this occurs when the LO frequency is nearly equal to the signal generator frequency, so that the difference in frequency which is the IF, is very small, say within 100 Hz). Under this condition, turning the tuning capacitor (C16 or C17) very slightly in either direction from the optimal position, increases the IF frequency.

The oscilloscope time-base is increased to 1 ms/division, and the crystal is carefully further fine-tuned to display the lowest possible frequency on the oscilloscope. At this stage, the LO has been tuned to the nominal receiver frequency, with an error equal to the frequency of the IF signal that is displayed on the oscilloscope.

d) Spurious Rejection

The IF signal is made 4 kHz (deviation frequency) at 20 mV amplitude by changing the signal generator frequency by 4 kHz from the nominal receiver frequency, and adjusting its attenuation. Next, R6 is reduced so that the IF amplitude decreases by half. This removes the overdrive at pin 21, thus enabling the proper tuning of C15, which is now tuned again, along with C12, to maximise the IF level. R6 is then made maximum and the signal generator adjusted to give 20 mV IF level. R6 is reduced till the IF amplitude drops to 17 mV. This ensures that the LO level is just sufficient to switch the mixers, and not larger, as that would degrade spurious rejection. With this final adjustment, the receiver is fully tuned, and its spurious rejection (for VHF receivers) can be close to 70 dB. Reducing the IF level even further would result in an even better spurious rejection, with a slight decrease in sensitivity. In circuits that do not use the damping resistor R6, the IF level is finally reduced from 20 mV to 17 mV by detuning C15.

Pager receivers

UAA2080T VHF/UHF paging receiver

1.5 APPLICATION CIRCUITS

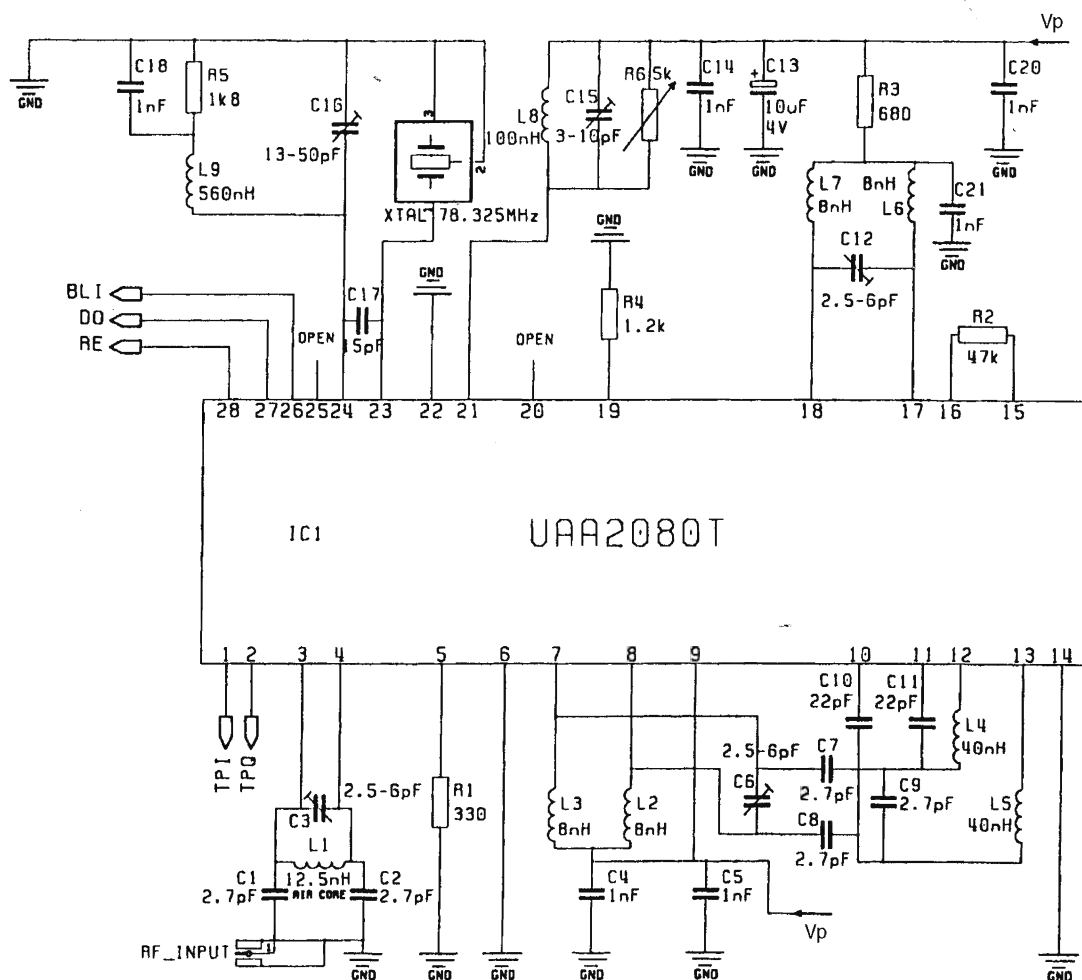


Figure 1.3 469.95MHz Application

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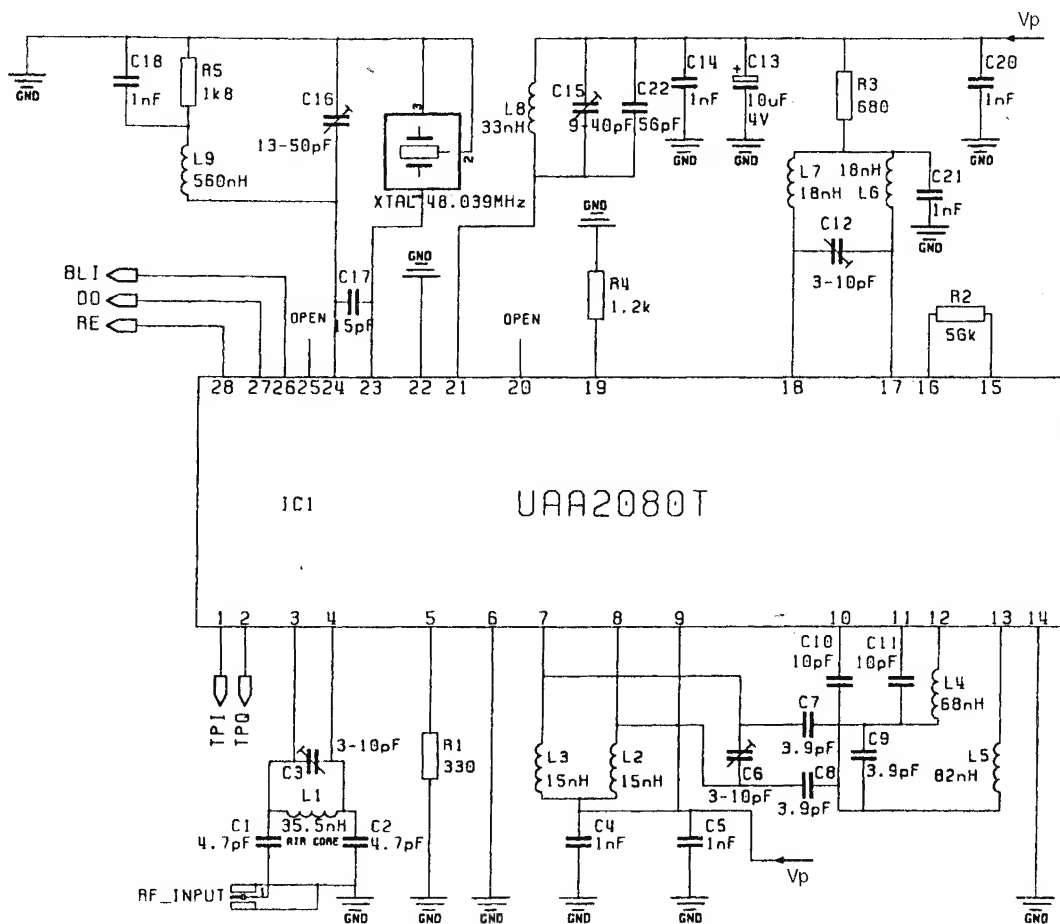


Figure 1.4 288.234MHz Application

Pager receivers

UAA2080T VHF/UHF paging receiver

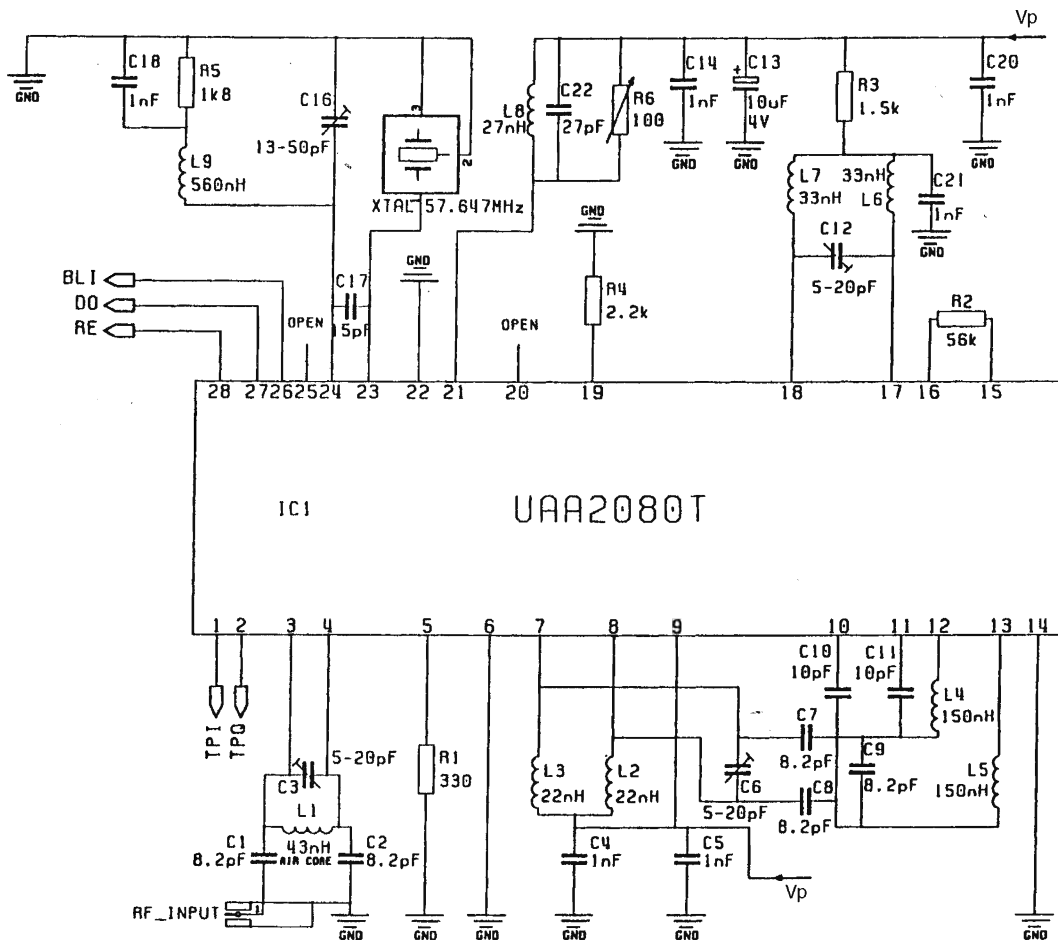


Figure 1.5 172.941MHz Application

Pager receivers

UAA2080T VHF/UHF paging receiver

List of Components

COMPONENT	VALUE		
	470MHz	288MHz	173MHz
R1	330 Ω	330 Ω	330 Ω
R2	47k Ω	56k Ω	56k Ω
R3	680 Ω	680 Ω	1.5k Ω (680 Ω)
R4	1.2k Ω	1.2k Ω	2.2k Ω (1.2k Ω)
R5	1.8k Ω	1.8k Ω	1.8k Ω
R6	5k Ω pot.	—	100 Ω pot.
C1	2.7pF	4.7pF	8.2pF
C2	2.7pF	4.7pF	8.2pF
C3	2.5–6pF	3–10pF	5–20pF
C4	1nF	1nF	1nF
C5	1nF	1nF	1nF
C6	2.5–6pF	3–10pF	5–20pF
C7	2.7pF	3.9pF	8.2pF
C8	2.7pF	3.9pF	8.2pF
C9	2.7pF	3.9pF	8.2pF
C10	22pF	10pF	10pF
C11	22pF	10pF	10pF
C12	2.5–6pF	3–10pF	5–20pF
C13	10 μ F tant.	10 μ F tant.	10 μ F tant.
C14	1nF	1nF	1nF
C15	3–10pF	9–40pF	— (13–50pF)
C16	13–50pF	13–50pF	13–50pF
C17	15pF	15pF	15pF
C18	1nF	1nF	1nF
C19	—	—	—
C20	1nF	1nF	1nF
C21	1nF	1nF	1nF
C22	—	56pF	27pF (82pF)
L1	12.5nH air core	35.5nH air core	43nH air core
L2	8nH	15nH	22nH
L3	8nH	15nH	22nH
L4	40nH	68nH	150nH
L5	40nH	82nH	150nH
L6	8nH	18nH	33nH
L7	8nH	18nH	33nH
L8	100nH	33nH	27nH (68nH)
L9	560nH	560nH	560nH
CRYSTAL	78.325 MHz	48.039 MHz	57.647 MHz

The values in brackets for the 173MHz circuit, are an alternative, that may give a slightly worse spurious rejection.

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1.6 PCB Layout Guidelines

Proper layout of components and copper tracks is required in order to attain optimal receiver performance, both in terms of sensitivity, and spurious rejection. At UHF, the PCB layout of a pager tends to be a rather critical issue, and it is not uncommon to have 3 or more redesigns. The following are some general guidelines that assist in proper layout design.

a) Keep the loop area of an RF current path as small as possible, as it minimises outgoing radiation, as well as spurious pickup. This implies that components of a tank (parallel resonant) circuit should be very close together. The Colpitts Oscillator circuit comprising C16, C17 and the crystal, form a tank. C18, R5 and L9 should be close to C16. The oscillator draws a large RF current from the supply, and the loop is closed by the supply and ground points. Therefore, the supply point of L8-C15/22-R6 and the ground point of crystal-C16-R5-C18, should be close together. The frequency multiplier circuit comprising R3, R4, C12, C21, L6 and L7, along with the ground and supply points, should enclose a minimal area. The ground points at R4 and C21, should be close together so that the common mode current (which is bypassed by C21) produces minimal signal in the ground line. In general, all RF circuits should be compact and close to the IC pins to which they connect. Also, the RF current loops of the oscillator and the frequency multiplier, should not touch the circuitry of the frontend (RF amplifier and phase shifter).

b) The ground of the low noise IF amplifier (immediately following the mixer) is at pin 6. This is also the connection to the common substrate of the UAA2080T. The mixer ground is at pin 14, while the rest of the circuits have their ground at pin 22. These three pins should be directly connected to a ground plane under the IC so that they are at the same reference level.

c) Parasitic coupling of the oscillator and frequency multiplier, with the RF amplifier should be minimised in order to improve spurious rejection and sensitivity. Coupling between the mixer LO and the RF amplifier produces a dc offset voltage at the mixer output. This reduces the gain of the following IF section. Unfortunately, the dc offset cannot be measured directly

since it is not available at external pins. It manifests as a reduction in sensitivity. Large coupling shows sudden change between the I and the Q channel gains with slight tuning of tank circuits around their resonant point. This is due to large changes in phase between the mixer LO and the mixer RF inputs. This parasitic coupling is best reduced by physical separation and proper coil orientation (minimising inductive coupling). The input section of RF amplifier (including R1) should have a grounded guard ring to minimise coupling with signals from the oscillator and frequency multiplier. To reduce coupling with the antenna, L6 and L7 should be kept antiparallel side-by-side so that the magnetic far-field is minimised (due to the individual fields being in opposite directions).

d) The PCB tracks to the digital interface (pins 25, 26, 27 and 28) and the IF output (pins 1 and 2) should be as short as possible. Long tracks (more than 5 cm) reduce sensitivity and may require RF decoupling capacitors at the IC pins.

e) To maintain a balanced RF signal at differential inputs and outputs, it should be ensured that the lead lengths are equal so that equal inductances (1 nH/mm) are added to the positive and the negative paths of the differential signal. For example, the track length from pin 17 to L6 and pin 18 to L7, should be equal. C21 should connect midway on the track joining L6 and L7. Tracks from C12 should only join at the IC pins 17 and 18 to tune out the inductance. This ensures that the maximum signal level is available to the mixer LO-input path. If the reactance was not killed directly at the pins, but say at the inductor terminals instead, then there would be a voltage drop across the inductance of the track which is between the pins and L6/L7.

f) While on the one hand, the ground point of all circuits should be close together at the same reference level, on the other hand, the positive supply line carrying the battery voltage V_p , should be RF-isolated for each circuit, especially for the low noise RF amplifier. LC low pass filtering has been incorporated in the application circuit. The inductance L is due to the long track length of the V_p supply in the board layout. The C is the 1nF decoupling capacitor at the various supply points in the layout (e.g at the common supply point of L2 and L3, and at pin 9). The

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upper -3 dB cutoff frequency of the LC filter should be about 10 times smaller than the crystal frequency. If long tracks are not possible, then large series inductances may be used in the supply line.

g) It was observed that the bypass capacitor C21 reduced the receiver sensitivity when used in some board layouts, due to the bypassed RF current interacting with the front end. If this occurs, then it is better not to use C21 in the circuit.

DESIGN OF CRYSTAL OSCILLATOR

The UAA2080 is a direct conversion receiver, implying a zero IF. Thus the local oscillator frequency should be equal to the received frequency. A crystal oscillator is employed for the generation of a stable and precise oscillation frequency. For received frequencies higher than the crystal oscillator frequency, a frequency multiplier has to be designed with a suitable multiplication factor.

2.1 FREQUENCY MULTIPLICATION FACTOR AND CRYSTAL FREQUENCY

There are various possibilities of combining crystal frequencies with multiplication factors, to produce the mixer's LO injection frequency, which is also the pager receiver frequency. There are two stages of frequency multiplication: 1) oscillator output tank, tuned to m_1 times the oscillation frequency, f_L , and 2) differential amplifier frequency multiplier, whose output tank is tuned to m_2 times its input drive frequency (which is $m_1 f_L$)

Thus, the receiver frequency f_{RX} , is given by

$$f_{RX} = m_1 m_2 f_L$$

For best receiver performance, the highest crystal frequency (f_L) and the lowest multiplication factor ($m_1 m_2$) should be chosen. The reason for this is to keep spurious rejection as large as possible. Strong spurious responses (called spurs, at frequency $f_{spurious}$) occur due to spurious components in the mixer's LO injection that come from the oscillator and the frequency multiplier. These frequencies are given by

$$f_{spurious} = f_{RX} \pm N \cdot f_L \quad \text{with } N = 1, 2, 3, \dots$$

Due to various tuned circuits in the RF signal path and the frequency multiplication path, the spurious rejection, $\alpha_{spurious}$, is proportional to the separation of the spurious frequency from the receiver frequency i.e.

$$\alpha_{spurious} \propto |f_{spurious} - f_{RX}| / f_{RX}$$

$$\propto N f_L / f_{RX}$$

$$\propto N / m_1 m_2$$

Strongest spurs occur at frequencies $f_{RX} - f_L$ and $f_{RX} + f_L$ (corresponding to $N = 1$). The spurs tend to weaken as N increases. In order to have large spurious rejection (larger $\alpha_{spurious}$), the product $m_1 m_2$ should be kept small. However m_2 should be kept smaller, in preference to keeping m_1 small. Smaller m_2 requires a smaller signal amplitude to drive the frequency multiplier, thus giving better spurious rejection.

The maximum crystal frequency f_L , at which the circuit in Fig. 2.0 oscillates, is given approximately by this rule of thumb:

$$f_{LO} = \frac{4000}{(C_0 + C_{L0}) \sqrt{R_1}} \quad (2.0)$$

with f_{LO} in MHz, R_1 in ohms, C_0 and C_{L0} in pF. R_1 is the motional resistance of the crystal, C_0 its static capacitance and C_{L0} its nominal load capacitance. The factor 4000 in the numerator, is related to the common-emitter transconductance (g_t) of transistor T2. The dc current, which determines the transconductance, is set by the external emitter bias resistor R_E .

The above formula is a simplification of the gain equation that is described later in detail (section 2.2), and it serves only as a starting point for the oscillator design. It assumes that the oscillator, as shown in Fig. 2.0, is biased by a 1.8 k external emitter resistor, and that the crystal is sufficiently pullable in order to tune it over the required range with $1/3 \leq C_1/C_2 \leq 3$. The transconductance g_t is taken as 3 millimhos, which is a third of that given in the Y - parameter curves, to provide sufficient

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gain margin over the tuning range. The oscillator circuit will be described in more detail later.

In general, third overtone crystals with $C_0 \leq 5$ pF, C_{L0} around 8 pF, and $R_1 \leq 30$ ohms, fit comfortably in the frequency bracket of 50 to 60 MHz, as dictated by (2.0). Based on this, the choice of the frequency multiplication scheme is given in Table 2.0.

Table 2.0 Crystal Frequency and Multiplication Factors

Oscillator Tank multiplication factor, m1	Diff. Amp. multiplication factor, m2	Total multiplication factor	Receiver Frequency range, fRX (MHz)	Crystal Frequency range, fL0 (MHz)
1	1	1	≤ 60	≤ 60
2	1	2	60 - 120	30 - 60
(1)	(3)	3	120 - 180	42 - 60
3	1	3	120 - 180	42 - 60
(1)	(5)	(5)	(180 - 300)	36 - 60
2	3	6	≥ 180	≥ 30

Bracketed option gives worse spurious rejection

Multiplication factor of $m_1 = 3$ or more is not recommended when $m_2 > 1$, because of large variation in the oscillator current amplitude at m_1 harmonic, over tuning range. Factor m_2 takes only odd values, and should normally not be more than 5 (for reasonable mixer conversion gain).

The above table is only a rough guideline. For still lower multiplication factors, frequencies higher than that mentioned above for the crystal, may be used, if a smaller R_1 or C_0 is available, or if a larger oscillator bias current is used. On the other hand, a higher multiplication factor, and thus a lower crystal frequency may be used if the R_1 is too large, or if a smaller bias current is desired. Of course this would increase the number of LO subharmonics and spurious responses, but may not degrade performance if the spurious responses are kept within PTT specifications, by using higher quality factor tank circuits in the RF amplifier stage.

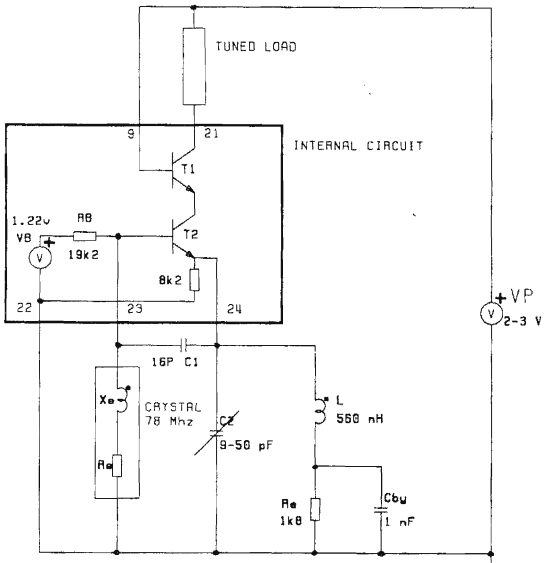


Figure 2.0 78 MHz Colpitts Oscillator

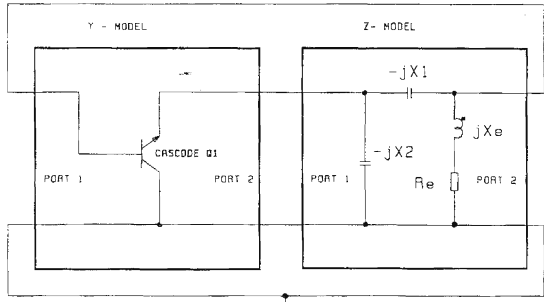


Figure 2.1 Y and Z oscillator model

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2.2 DESIGN OF THE CRYSTAL OSCILLATOR

The UAA2080 crystal oscillator is built around a single transistor having a cascode output. As the collector is virtually grounded, the Colpitts or the Clapp-Gouriet oscillator configurations can be implemented. A typical application circuit for the Colpitts oscillator is shown in Fig. 2.0. Placing a tuning capacitor in series with the crystal would implement the Clapp-Gouriet oscillator.

Oscillation Criterion

The oscillator can be considered as an active two-port network (represented by its common-collector Y-parameters) connected to a feedback network (represented by is Z-parameters), as shown in Fig. 2.1. The condition for stable oscillation (unity loop gain and zero phase shift) implies that

$$y_{11}Z_{22} + y_{22}Z_{11} + y_{12}Z_{12} + y_{21}Z_{21} + d_y d_z + 1 = 0, \quad (2.1a)$$

where,

y_{ij} denotes a common-collector Y-parameter of the active network

z_{ij} denotes a Z-parameter of the feedback network

$$d_y = y_{11}y_{22} - y_{21}y_{12} \quad (2.1b)$$

$$d_z = z_{11}z_{22} - z_{21}z_{12} \quad (2.1c)$$

Substituting the common-collector Y-parameters by the equivalent expression using common-emitter Y-parameters, and substituting the Z-parameters by the equivalent expressions using X_1, X_2, X_e and R_e , and after manipulating considerably, it can be shown that the oscillation criterion becomes

gain:

$$g_f = \frac{R_e - [(g_o + g_r)X_1X_2 - g_oX_2X_e + b_i b_r X_1X_2R_e + g_r b_r X_1X_2X_e]}{\left(1 + \frac{1}{\beta}\right)X_1X_2 - \frac{X_1X_e}{\beta} + \left(\frac{g_o}{\beta} - g_r\right)X_1X_2R_e + b_i b_r X_1X_2X_e}$$

phase (frequency):

$$X_1 \left[1 + \frac{g_f R_e}{\beta} \right] + X_2 [1 + g_o R_e] = X_e + X_1 X_2 \left[b_i + b_r - R_e (g_r b_i + g_i b_r) + X_e \left\{ g_f \left(\frac{g_o}{\beta} - g_r \right) + b_i b_r \right\} \right] \quad (2.2b)$$

where

$$y_{re} = g_r + j b_i$$

$$y_{re} = g_r + j b_r$$

$$y_{ie} = g_i + j 0 = g_i / \beta,$$

(b_i taken as 0, as C_{be} is included in X_1)

$$y_{oe} = g_o + j 0,$$

(b_o taken as 0, as C_{ce} is included in X_2)

β = beta, ac current gain, about 70 minimum.

X_1 includes $C_{be} = b_i / \omega$ (base-emitter capacitance)

X_2 includes $C_{ce} = b_o / \omega$ (collector-emitter capacitance)

with ω = angular frequency ($2\pi f$, f = frequency)

The terms b_i and b_o are taken as zero and do not appear in equations (2.2a) and (2.2b). This is because the base-emitter and collector-emitter capacitances, C_{be} and C_{ce} , have been combined with X_1 and X_2 respectively.

The simulated common-emitter Y-parameters for practical emitter bias resistor values, are given in Fig. 2.2a to Fig. 2.2d. These curves include the effect of the 19 k Ω base bias resistor, 8 k Ω internal emitter bias resistor, cascode transistor with 5 k Ω tuned load at output, and, lead inductance (2nH) and lead capacitance (0.5pF). The input and output common-emitter Y-parameters have been resolved into parallel resistance and capacitance, as shown in Figures 2.2a and 2.2c.

The curve for g_o does not include the effect of the parallel resistance R_p of the mode selector inductor (which is shown as L in Fig.2.0). The value of g_o read from the curve, must be increased by $1/R_p$ Mhos.

The effect of b_i and b_o are additional capacitances of about 1.2 pF and 1.1 pF which have to be added to C_1 and C_2 respectively. The effective value of C_2 is decreased by the mode selector inductor as given by

$$C_2 = C_2 (\text{component} + \text{parasitics} + C_{ce}) - 1/(L \omega^2) \quad (2.3)$$

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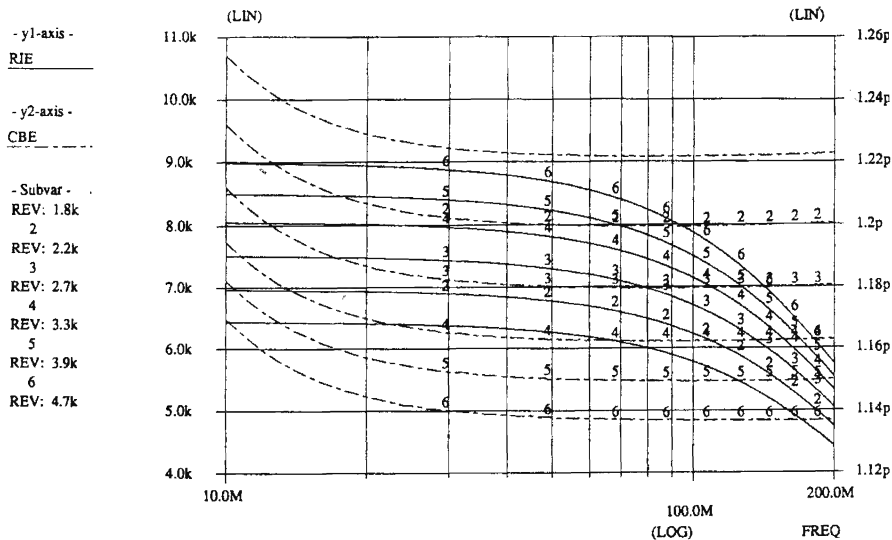


Figure 2.2a Y model parallel input resistance & capacitance

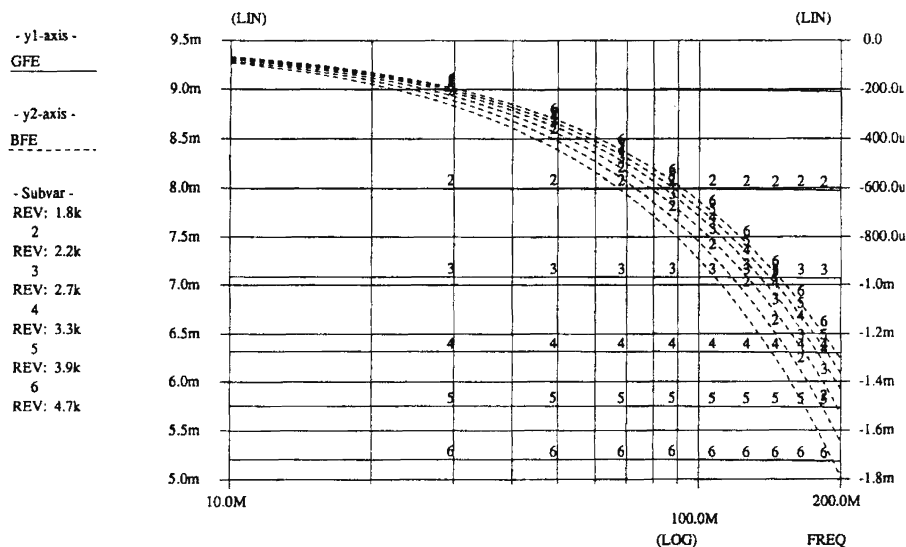


Figure 2.2b Y model forward transfer parameters

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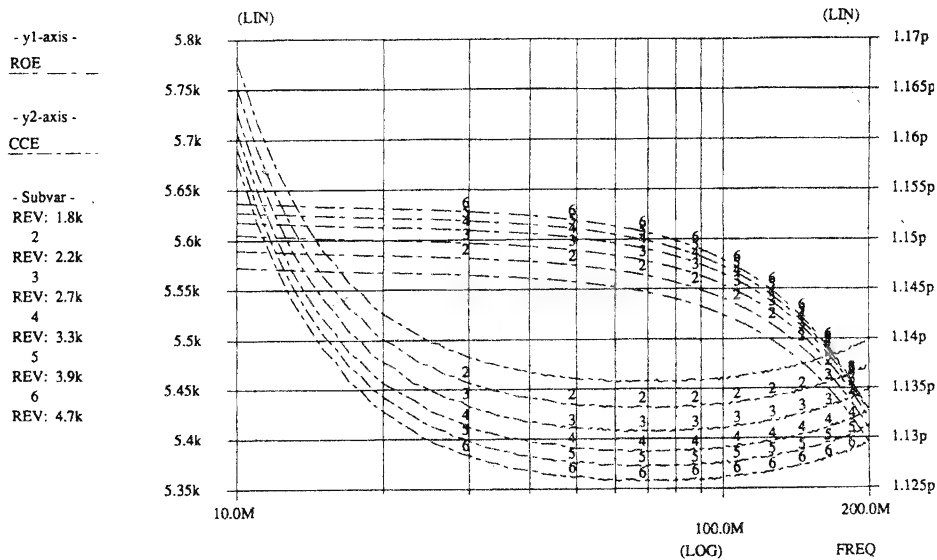


Figure 2.2c Y model output parallel resistance & capacitance

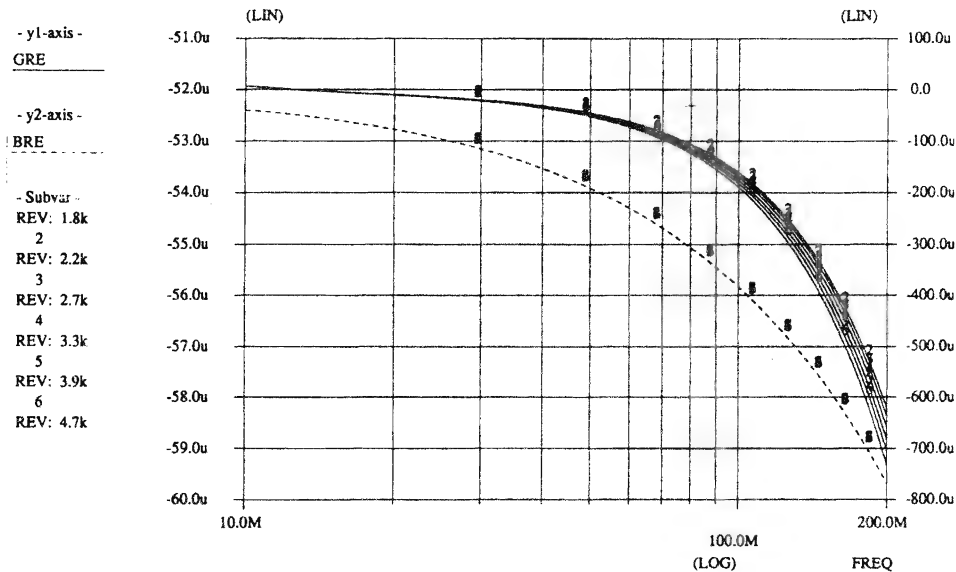


Figure 2.2d Y model reverse transmission parameters

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At frequencies less than 80 MHz the gain and phase equations can be approximated as

$$\text{phase: } X_1 + X_2 = X_e \quad (2.4a)$$

gain:

$$g_f = \frac{\frac{R_e}{X_1 X_2} + \frac{g_0 X_2}{X_1} - (g_r + b_r b_i R_e + g_r b_i X_e)}{1 + \frac{1}{\beta} + (\frac{g_0}{\beta} - g_r) + R_e + b_i X_e - \frac{X_e}{\beta X_2}} \quad (2.4b)$$

or

$$g_f = \frac{\frac{R_e}{X_1 X_2} + \frac{g_0 X_2}{X_1}}{0.95 - \frac{X_e}{70 X_2}} \quad \text{for practical purposes} \quad (2.4c)$$

Equivalent Crystal Circuit

The crystal can be represented by its equivalent circuit as shown in Fig. 2.3a. At the loaded frequency (which is between its unloaded series resonant frequency and its unloaded parallel resonant frequency) the crystal is inductive and it is in resonance with an external load capacitor C_L . In the oscillator, $C_L = C_p + (C_1 \text{ series } C_2)$. C_p is the parasitic board capacitance across the crystal. If C_p is combined with the crystal, then the combination is still inductive, and can be represented by the circuit in Fig. 2.3b, with

$$R_e = \frac{R_1 (C_0 + C_L)^2}{(C_L - C_p)^2} \quad (2.5a)$$

and

$$X_e = 1/[\omega(C_L - C_p)] \quad (2.5b)$$

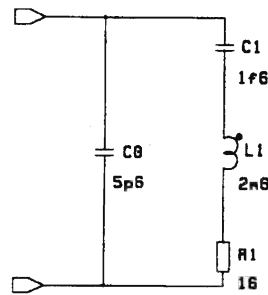
Furthermore, putting $C_1/C_2 = a$, the gain equation (2.4c) becomes

$$g_f = \frac{(\sqrt{a} + 1/\sqrt{a})^2 R_1 \omega^2 (C_0 + C_1)^2 + g_0/a}{0.95 - (1+a)/70} \quad (2.6)$$

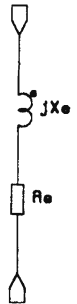
In practice the transconductance is kept 2 times that obtained from the above equation, over the entire tuning

range, in order to ensure sufficient oscillation amplitude. This is achieved by appropriate biasing, as given later.

78.325 MHz CRYSTAL



(a)



(b)

Figure 2.3 Crystal Equivalent Circuits

Crystal Pullability and Capacitance Ratio

Define the crystal pullability

$$F = \frac{f_{L0} - f_r}{f_r} 10^6 \text{ ppm} = \frac{C_1}{2(C_{L0} + C_0)} 10^6 \text{ ppm}, \quad (2.7)$$

where f_{L0} is the loaded antiresonance frequency of the crystal, with nominal load capacitance C_{L0} , and f_r is its unloaded series resonance frequency.

If the crystal is to be pulled by P ppm from f_{L0} to f_L , the corresponding load capacitance C_L that is required, is given by

$$\frac{C_1}{C_{L0}} = 1 - \frac{P(1 + C_0/C_{L0})}{P + F} \quad (2.8)$$

where, P is negative when $f_L < f_{L0}$

If C_1 is used for tuning, then the capacitance ratio $a = C_1/C_2$ is given by

$$a = (1 + x)/(1 - x), \quad (2.9a)$$

and

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if C_2 is used for tuning, then $a = (1 - x)/(1 + x)$. (2.9b)

$$\text{Here } x = \frac{P(C_{L0} + C_p)}{(P+F)(C_{L0} - C_p)} \quad (2.10)$$

It is assumed that $a = 1$ when $P = 0$ ppm.

The crystal should be chosen with just a large enough pullability, F , so that at the limits of tuning range of $-P$ ppm and $+P$ ppm, a or $1/a$ (which ever is greater than unity) is within a maximum limit as dictated by the gain equation. If F is too large, then the crystal will be very easily pulled with small changes in C_L , and this may cause undesirable drift in frequency.

As a final remark, the gain is given by

$$g_t = \frac{(\sqrt{a} + 1/\sqrt{a})^2 R_1 \omega^2 [C_0 + C_p + 2(C_{L0} - C_p)/(1 + A)]^2 + g_0/a}{0.95 - (1 + a)/70} \quad (2.11)$$

where $A = a$ when C_1 is tuned, and $A = 1/a$ when C_2 is tuned. The relation between the capacitance ratio $a = C_1/C_2$ and the pulling by P ppm, for the two cases, is as given before.

Phase and Frequency Stability

For good phase and frequency stability, the effective loop gain must have a narrow peak at the oscillation frequency.

effective loop gain = $G \cdot \cos(\text{Phase})$, G = loop gain magnitude, Phase = loop phase shift

Simulations show that when tuning with C_2 , the effective loop gain has a very broad peak at the upper limits of the tuning range, while when tuning with C_1 , the peak is broader at the lower frequencies, as shown in Figures 2.4a and 2.4b. The variation in loop gain is smaller when tuning with C_2 . To pull to higher frequencies, C_1 tuning capacitor must have much smaller values compared with C_2 tuning capacitor whose effective value is reduced by the inductance L . A practical rule of thumb in selecting crystals for good phase-frequency stability is

$$[2\pi f_L (C_0 + C_L) R_1]^{-1} > 4 \quad (2.12)$$

Suppression of Lower Order Modes

If the crystal is operated at other than the fundamental tone, then the lower order modes must be suppressed to prevent oscillation at those frequencies. This is achieved by the inductor L which is parallel resonant with C_2 capacitor, at a frequency which is below the oscillation frequency, but above the next lower crystal response. Since the L - C_2 tank is inductive at frequencies below its parallel resonant frequency, the oscillation criterion will not be met for those frequencies.

$$C_2 = C_{2act} - \Delta C_2, \text{ with}$$

$$C_{2act} = C_2(\text{component} + \text{parasitics} + C_{ce}) \quad (2.13a)$$

$$\Delta C_2 = 1/L\omega^2 \text{ and } \omega = 2\pi f_L, f_L = \text{oscillation frequency} \quad (2.13b)$$

L is chosen so that C_2 has the desired positive value at the oscillation frequency, and is negative (inductive) at the next lower crystal overtone or spurious response (in case the spurious response is not sufficiently suppressed by the crystal manufacturer). By suppression of the spurious response it is meant that the R_1 of the crystal at that spurious frequency, should be large enough in order for the gain criterion to be unfulfilled by at least a margin of 6 dB.

If the crystal is operated at the 3rd overtone, then ΔC_2 (at fundamental tone) = $9 \Delta C_2$ (at 3rd overtone) = $9/L\omega^2$

In case C_2 is used for tuning, then,

$$C_{2act} < 9/L\omega^2 \text{ or } C_2 < 8/L\omega^2 \quad (2.14)$$

Some useful formulas are

$$f_T = 1/[2\pi\sqrt{(LC_{2act})}] \quad (2.15a)$$

the mode selector tank resonance frequency

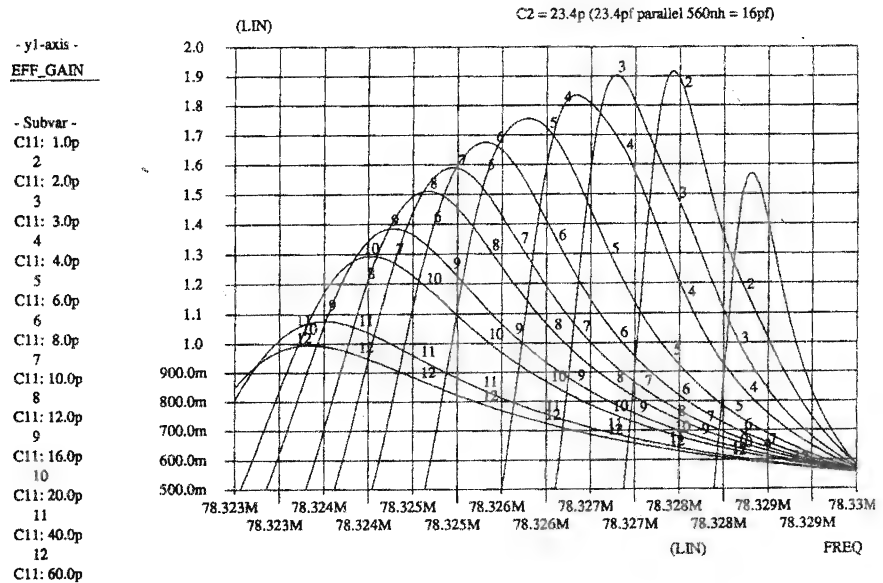
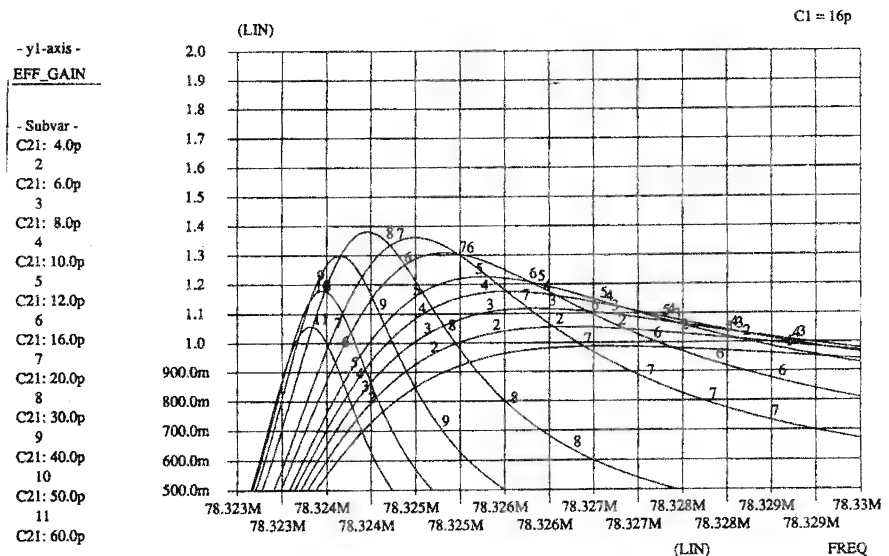
$$C_{2act} = C_2/[1 - (f_T/f_L)^2] = [1 + \omega^2 LC_2]/[L\omega^2] \quad (2.15b)$$

$$L = [1 - (f_T/f_L)^2]/[\omega_r^2 C_2], \omega_r = 2\pi f_T \quad (2.15c)$$

$$C_{2act} = \text{actual component} + \text{parasitic} + C_{ce} \text{ capacitance} \quad (2.15d)$$

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Figure 2.4a Loop voltage gain when C_1 is tunedFigure 2.4b Loop voltage gain when C_2 is tuned

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If the crystal is operated at the fundamental frequency, then L could be a large inductance used as a choke. The tuning range of C_2 is not restricted by the choice of L.

Frequency Sensitivity with Temperature

With C_L defined as $C_p + C_1 C_2 / (C_1 + C_2)$, (2.16a)

$$\frac{dC_L}{C_L} = \frac{dC_p}{C_p} + \frac{dC_1}{C_1} \cdot \frac{[C_2]}{(C_1 + C_2)} + \frac{dC_2}{C_2} \cdot \frac{[C_2^2]}{C_2(C_2 + C_{2act})} - \frac{dL}{L} \cdot \frac{[\Delta C_2 C_1]}{C_2(C_1 + C_2)} \quad (2.16b)$$

Replacing the fractional change in C_p , C_1 , C_2 and L by their respective temperature coefficients, the temperature coefficient of C_L can be directly determined from the above equation. The frequency of oscillation solely depends on the crystal, so the frequency drift due to temperature, caused by components (other than the crystal itself) is given as

$$S \cdot dC_L, \text{ where } S = -\frac{C_1}{2(C_0 + C_L)^2} \quad (2.16c)$$

i.e. the pulling sensitivity of the crystal.

This frequency drift coefficient due to components has to be added to the temperature coefficient of the crystal itself, to obtain the overall temperature coefficient for the oscillator frequency. However, in practice, the frequency drift due to the components is much smaller than the drift due to a crystal that usually has about ± 5 ppm frequency drift in the operating temperature range.

Crystal Tolerance, Aging and Frequency Drift

The tuning range of the oscillator should be large enough to compensate for the calibration tolerance of the crystal, plus its aging tolerance taken over the life of the paging receiver. Thus

$$P = -(N + nt) \text{ where} \quad (2.16d)$$

P = the tuning range of the oscillator in ppm.

N = calibration tolerance of the crystal in ppm.

n = aging coefficient of the crystal in ppm/year.

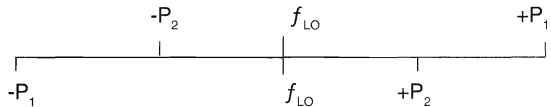
t = life of the pager in years.

Only the maximum magnitude of n, and not its sign (positive or negative), is guaranteed by the crystal manufacturer, so the tuning range P should compensate for both positive as well as negative values of n.

For example, $N = -10$ ppm to $+10$ ppm, $n = 0$ to $+1$ ppm per year, $t = 5$ years. Then, $P = -(-10 \text{ ppm to } +10 \pm 1 \times 5 \text{ ppm})$ i.e. -15 ppm to $+15$ ppm.

Metallic enclosures can give a larger aging coefficient compared with glass enclosures. It should be noted that the crystal's and the oscillator's temperature coefficient of frequency does not influence the oscillator tuning range.

Crystal Tolerance and Aging ($-P_2$ to $+P_1$ ppm)



Oscillator Tuning Range ($-P_1$ to $+P_2$ ppm)

The drift in receiver frequency, f_{RX} , in ppm, is the same as the drift in the crystal frequency when measured in ppm. The total difference in ppm, $\Delta f(\text{ppm})$, between the transmitter and receiver frequency, is given by

$$\Delta f(\text{ppm}) = f_{\text{OFFSET}}(\text{ppm}) + S_T \cdot \Delta \text{Temp} + n \cdot \Delta t, \text{ where} \quad (2.16e)$$

$f_{\text{OFFSET}}(\text{ppm})$ is the frequency offset of the transmitter in ppm, from the nominal frequency at which the receiver is tuned.

S_T is the total temperature coefficient of the oscillator frequency (due to crystal and components) in ppm/°K.

ΔTemp is the change in temperature from room temperature, at which the crystal (i.e. oscillator) was tuned.

n is the aging in ppm/year.

Δt is the time (in years) elapsed since the paging receiver was last tuned.

As $\Delta f(\text{ppm})$ increases, the sensitivity of the receiver decreases. When $\Delta f(\text{Hz}) = \Delta f(\text{ppm}) \cdot f_{RX}$ is more than the deviation in the modulation frequency (e.g. 4 kHz), then the demodulator inside the UAA2080 will not be able to

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decode the received data at all. At UHF the demand for a small S_T and 'n' is rather severe, while at lower frequencies it is more relaxed. For UHF applications, the crystal should be pre-aged, and should have a very small temperature coefficient coefficient (< 5 ppm over the operating temperature range).

2.3 LARGE SIGNAL ANALYSIS

A large signal analysis of the oscillator is required in order to determine the biasing, and to determine the signal current at the fundamental frequency or its harmonics. Denote

V_{BE} = base-emitter dc voltage under large signal condition
 v_{BE} = base-emitter large signal amplitude at oscillation frequency ω
 v_{be} = base-emitter instantaneous voltage
 i_c = instantaneous collector current

Then, $v_{be} = V_{BE} + v_{BE} \cdot \cos(\omega t)$ and $i_c = I_s \cdot \exp(v_{be}/V_T)$ where I_s is the reverse saturation current, and $V_T = 0.026$ V at room temperature.

This gives, $i_c = I_{dco} \exp(v_{BE} \cos(\omega t)/V_T)$, where I_{dco} (the quiescent collector current) = $I_s \exp(V_{BE}/V_T)$

I_{dco} is the quiescent collector current, and is equal to the value of i_c at periodic intervals when $\cos(\omega t)$ is zero i.e. when the instantaneous value of v_{be} is V_{BE} . As oscillation builds up i.e. as v_{BE} increases, the dc component of the collector current increases, thereby increasing the voltage drop across the emitter resistor and also decreasing the base-emitter dc voltage V_{BE} by the same amount. Therefore, the quiescent collector current which is exponentially related to V_{BE} , also decreases as oscillation builds up. It should be noted that even though the quiescent current decreases with increasing v_{BE} , the dc collector current (average of i_c) increases.

Taking the Fourier series representation of i_c , the large signal components are

dc current: $I_{dc} = I_{dco} \cdot I_0(v_{BE}/V_T)$
 Fundamental: $I_{c1} = 2I_{dco} \cdot I_1(v_{BE}/V_T) \cdot \cos(\omega t)$
 nth harmonic: $I_{cn} = 2I_{dco} \cdot I_n(v_{BE}/V_T) \cdot \cos(n\omega t)$
 $I_n(x)$ is the modified hyperbolic Bessel function of order n.

Define

Large signal transconductance, $g_m = I_{c1}/v_{BE}$

Fictitious small signal transconductance, $g_{mo} = I_{dc}/V_T$

Fig. 2.5 shows variation of I_{dc} (normalised to I_{dco}) with the signal amplitude.

In Fig. 2.6 the various collector current components have been normalised to I_{dc} (and not to I_{dco}). Fig. 2.6 also shows variation in g_m/g_{mo} with signal amplitude.

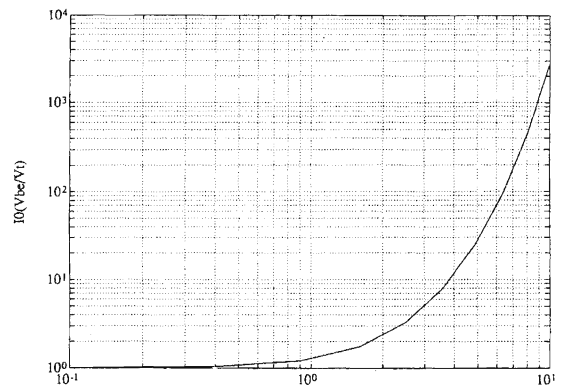


Figure 2.5 I_{dc}/I_{dco} versus v_{BE}/V_T

Basic Design Consideration

For large v_{BE} signal levels, the fundamental component of the collector current approaches $2I_{dc}$. This is true for the higher harmonics too. In fact, whenever $v_{BE} > 3.5 V_T$ or $g_m/g_{mo} < 0.5$, it can be seen from Fig. 2.6 that $I_{c1} > 1.8 I_{dc}$. Hence, if $g_m/g_{mo} < 0.5$ over the tuning range, a stable amplitude of about $2I_{dc}$ can be maintained for the fundamental component of the collector current. This should essentially be the design goal for the Colpitts oscillator, and it can be achieved by an appropriate emitter bias resistor.

As long as the condition $g_m/g_{mo} < 0.5$ is met, the base-emitter signal amplitude can be approximated as

$v_{BE} = 2V_T/(g_m/g_{mo})$ and can be read from the graph in Fig. 2.6.

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Biasing

In order to correctly bias the transistor, the dc current is set so that $g_{m0} = 2 \cdot [\text{maximum } g_i]$, with g_i considered over the tuning range, and given by the gain equation (2.11). With this g_{m0} , the dc current is given as $I_{dc} = V_T g_{m0}$. As oscillations build up, the large signal transconductance g_m becomes smaller, and finally becomes equal to g_i during steady state oscillation. This ensures that $g_m/g_{m0} < 0.5$ over the tuning range. For $g_m/g_{m0} = 0.5$, $v_{BE} = 3.5V_T$ and $\ln[I_0(v_{BE}/V_T)] = 2$ from Figures 2.6 and 2.7. Reverse saturation current, I_s , for the transistor is $2.7973 \cdot 10^{-14}$ mA, base bias resistor $R_B = 19k\Omega$, current gain $\beta = 70$ (taken as minimum), $V_T = 0.026$ V (at room temperature), and the bias voltage $V_B = 1.22$ V.

The effective emitter bias resistor, R_{eff} , is the parallel combination of the internal 8.2 k Ω resistor and the external resistor R_E . It is determined by substituting the above values into the equation

$$R_{eff} = \frac{V_B + V_T \ln[I_0(v_{BE}/V_T)] - V_T \ln(I_{dc}/I_s)}{I_{dc}} - \frac{R_B}{1 + \beta} \quad (2.17a)$$

Finally, the value of the external bias resistor is

$$R_E (k\Omega) = \frac{8.2 R_{eff}}{(R_{eff} - 8.2)} \quad (2.17b)$$

Figure 2.9 shows a plot of R_E versus I_{dc} , with signal amplitude v_{BE} taken as $3V_T$.

An easier approach is to have the biasing so that the actual small signal dc bias current is equal to the computed value of I_{dc} . This will ensure a slightly greater gain margin because the large signal dc current is always marginally larger than that of the small signal.

The simulated small signal dc current versus external bias resistor R_E is given in Fig. 2.8.

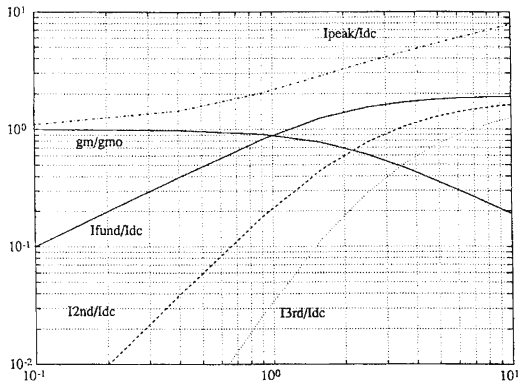


Figure 2.6 Harmonics and g_m/g_{m0} versus v_{BE}/V_T

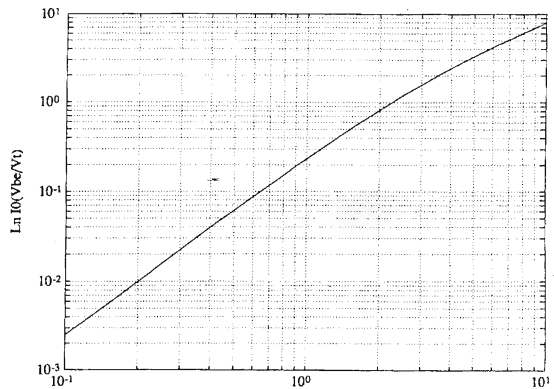
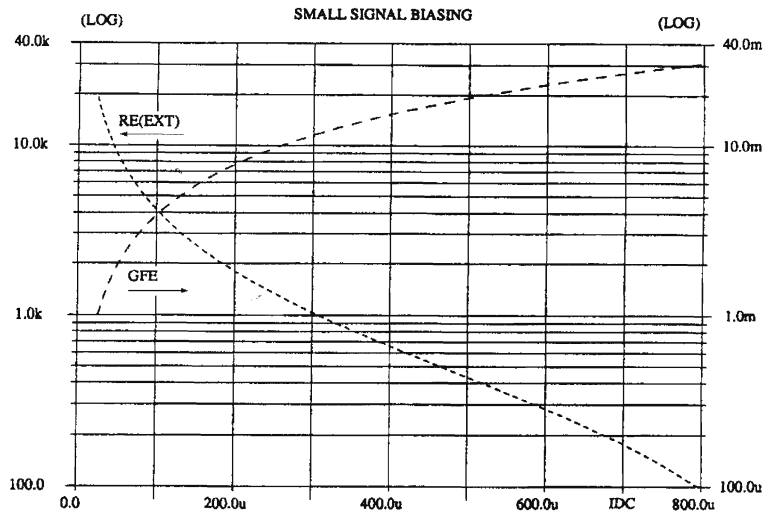
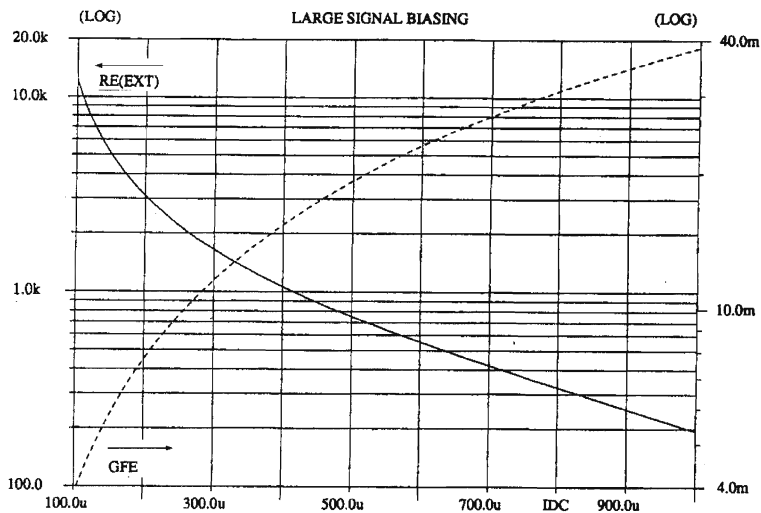


Figure 2.7 $\ln[I_0(v_{BE}/V_T)]$ versus v_{BE}/V_T

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Figure 2.8 R_E and g_f versus small signal dc currentFigure 2.9 R_E versus large signal dc current

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Crystal Power

The power dissipated by the crystal is

$$P_d = 0.5[\omega C_1 V_{BE}]^2 R_1 [1 + C_0 / C_L]^2 \quad (2.18)$$

watts, with $v_{BE} = 2V_T / (g_m / g_{mo})$,
and ω the angular frequency i.e. $2\pi f_{LO}$

Maximum dissipation occurs when $C_1 = C_2$,
corresponding to the largest gain margin (g_m minimal).

2.4 THE CLAPP-GOURIET OSCILLATOR

It is identical to the Colpitts crystal oscillator circuit, except that it has the tuning capacitor C_T in series with the crystal. However the gain margin progressively decreases as the crystal is pulled from lower to higher frequencies, and so it does not compare well with the Colpitts crystal oscillator which has maximum gain near the centre of the tuning range. The Clapp-Gouriet oscillator will have a constant gain with tuning, if an inductor is used instead of a crystal. This assumes that the series resistance of the inductor remains constant with tuning.

Denote C_L as the load capacitance when the crystal is pulled to the lower frequency limit. For maximum gain margin, C_1 and C_2 are chosen equal ($a = 1$), with $C_L = C_1 C_2 / (C_1 + C_2)$ i.e. $C_1 = C_2 = 2C_L$.

Also $C_L = C_T$ series $2C_1 C_2 / (C_1 + C_2) = C_T$ series $2C_L$, so the gain equation is

$$g_i = \frac{R_1 \omega^2 (C_0 + C_L - C_T)^2 + g_0}{0.95 - 2/70} \quad \text{with} \quad C_T = \frac{C_L C_L}{(C_L - C_L)} \quad (2.18)$$

The Clapp-Gouriet oscillator is ideal for the design of voltage controlled oscillator (VCO) in frequency synthesizer application.

2.5 EXAMPLES

1) DESIGN OF A 78.325 MHz COLPITTS OSCILLATOR

The crystal should be selected in order to meet the following criteria:

- Small bias current for the oscillator,
- Adequate tuning range, over which oscillation amplitude is not severely reduced.
- Sufficient phase-frequency stability margin
- Calibration tolerance and aging considering the life time of the paging receiver.
- Small temperature coefficient of frequency, to keep frequency drift within specified limits in the operating temperature range.

A third overtone 78.325 MHz crystal measured as follows on a network analyser.

$R_1 = 16$ ohms
 $C_1 = 1.58$ fF
 $C_0 = 5.61$ pF
 $L_1 = 2.6$ mH
 $C_{L0} = 8.2$ pF at 78.325000 MHz

The pullability F , using (2.7) is 57 ppm.

The board parasitic capacitance C_p measured across the crystal was 1.5 pF.

The variation of g_i with pulling P is shown in Fig. 2.10a, for 40, 50 and 60 ppm crystal pulling sensitivity F . It is a plot of (2.11), with 'a' as a function of 'x' given by (2.9a) and (2.9b). 'x' itself is a function of P , as given by (2.10). The two different set of curves correspond to whether C_1 or C_2 is being tuned.

If the small signal transconductance is 9 mMhos, then for $g_m / g_{mo} < 0.5$, the tuning range can be extended up to $9/2 = 4.5$ milimhos. From Fig 2.10a, the range of P is -17.5 to +7.5 ppm if C_2 is tuned, or -7 to +20 ppm if C_1 is tuned. It is worthwhile considering specifying the crystal with a combined aging and calibration tolerance of say -5 ppm to +15 ppm instead of the usual -10 to +10 ppm, when tuning with C_2 , or specifying -15 to +5 ppm when tuning with C_1 .

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The variation of capacitance ratio $a = C_1/C_2$ with P, is given in Fig. 2.10b, which also shows the variation of $1/a$ with P. The fixed capacitor C_1 or C_2 is taken as $2C_{L0}$ = approximately 16 pF.

If it is desired to tune over -15 to +15 ppm, then, at $P = -15$ ppm, $1/a$ is 5.5 for an F of 60 ppm. The net tuned capacitance then has a value $5.5 \times 16 = 88$ pF

Similarly, at $P = +15$ ppm, $1/a = 2.5$, so the net tuned capacitance has a value $6/2.5 = 6.4$ pF.

Giving a 3 pF margin for parasitic capacitance (board and transistor capacitance), the tuning range for either capacitance becomes 3.4 pF to 85 pF. A value of ΔC_2 (2.13a) should be added to the actual range for C_2 capacitance if it tuned.

If a practical value of up to 50 pF is used for the tuning capacitance, then the lowest value of the pulling range (corresponding to $1/a = 50/16 = 3.13$) is -13 ppm, from Fig. 2.10b. Taking this range for the tuning capacitance, the next step is as follows.

If C_2 is tuned, then from (2.14), 50 pF must be less than $8/L\omega^2$. This implies $L < 660$ nH. The tank resonance frequency f_r (2.15a) should be nearer to oscillation frequency f_1 for larger suppression margin of the fundamental tone. However, this makes ΔC_2 larger, with an attendant increase in C_{2act} as given by (2.13a). By trial, $L = 560$ nH gives $\Delta C_2 = 7.4$ pF using (2.13b) and f_r (minimum) = 30 MHz. So the maximum value of $C_{2act} = 50 + 7.4 = 57.4$ pF, while the component value is lesser by about 3 pF due to parasitics.

With C_2 tuned, the upper range for P is only 7.5 ppm. With a slightly reduced gain margin, P can be extended to about +10 ppm, at which $a = 2$, and $C_2 = 16/2 = 8$ pF, i.e. $C_{2act} = 8 + 7.4 = 15.4$ pF

If C_1 is tuned, then its range should be ideally 3.4 to 85 pF for a +/- 15 ppm tuning range. Considering the gain requirement from Fig. 2.10a, P can go low down to -7 ppm, at which $1/a = 1.7$ i.e. C_1 (maximum) = $1.7 \times 16 = 27.2$ pF. So the range of C_1 component value is 6.4 - 3 to 27.2 - 3 i.e. 3.4 pF to 24.2 pF.

Equation (2.12) gives a value greater than 4 over the tuning range, thus ensuring good phase-frequency stability.

In Fig 2.2b, it is given that the common-emitter small signal transconductance is 9 mMhos when the external bias resistor is 1.8 k. Figure 2.9 shows a plot of external bias resistor versus actual large signal dc current and transconductance. It is a plot of equations (2.17a) and (2.17b), with v_{BE} taken as 3.5 V_T . For the 1.8 k external emitter bias resistor, the large-signal dc current is about 280 μ A in the graph, closely agreeing with measured results.

The crystal power dissipation over the tuning range is a function of both v_{BE} and C_L , as given in (2.18). Moreover, it can also vary with C_1 if that is tuned. As a safe approximation, the maximum dissipation can be taken at the largest gain margin. From Fig. 2.10a, minimum transconductance (C_2 tuned) is about 2.7 mMhos, so $g_m/g_{m0} = 2.7/9 = 0.3$, and from Fig. 2.6, the corresponding $v_{BE} = 6V_T$ i.e. 156 mV. The pulling is about -7 ppm, corresponding to $C_L = 10.1$ pF from (2.8). With $C_1 = 16$ pF, the power dissipation $P_d = 29$ microwatts, which is well within the normal 100 microwatts crystal specification.

To determine the temperature coefficient of frequency, first the coefficients for C_p , C_1 , C_2 and L must be known.

From simulations, for a frequency range 30 to 100 MHz, and external bias resistor range 1.8 k to 5 k, the worst case values are

$$\frac{dC_{be}}{C_{be}} / ^\circ K = -500 \text{ ppm}/^\circ K \quad \text{and} \quad \frac{dC_{ce}}{C_{ce}} / ^\circ K = +100 \text{ ppm}/^\circ K$$

$$C_{be} = 1.2 \text{ pF and } C_{ce} = 1.1 \text{ pF}$$

These have to be combined with the coefficients of C_1 and C_2 components, which are ± 30 ppm/ $^\circ K$ and 700 ± 300 ppm/ $^\circ K$ respectively. If their individual values are 16 pF and 23 pF respectively (at $P = 0$ ppm), then

$$\frac{dC_1}{C_1} = \frac{1.2 \times (-500) + 16 \times (+/- 30)}{1.2 + 16} = -63 \text{ to } -1 \text{ ppm}/^\circ K$$

$$\frac{dC_2}{C_2} = \frac{1.1 \times 100 + 23 \times (700 + /- 300)}{1.1 + 23} = +386 \text{ to } +959 \text{ ppm}/^\circ K$$

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Also $\frac{dL}{L} / ^\circ K$ is given as +25 to +125 ppm/ $^\circ K$

The value of dC_p/C_p depends on the printed circuit board, and is not considered here.

Substituting the values in (2.16b), with $\Delta C_2 = 7$ pF, $C_1 = C_2 = 16$ pF, and $C_{2act} = 23$ pF,

$$\frac{dC_L}{C_L} = (-63 \text{ to } -1) \times 0.59 + (386 \text{ to } 959) \times 0.85 - (25 \text{ to } 125) \times 0.22 = 809 \text{ ppm}/^\circ K \text{ maximum}$$

Therefore

$$dC_L = (809 \times 10^{-6}) \times (8.2 \text{ pF})/^\circ K = 6.63 \times 10^{-3} \text{ pF}/^\circ K$$

S is computed from (2.16c) as

$$4.14 \times 10^6 / \text{Farad i.e. } 4.14 \text{ ppm/pF}$$

The temperature coefficient of frequency from (2.16c) is

$$\frac{df}{f} / ^\circ K = S \cdot dC_L = 4.14 \times (6.63 \times 10^{-6}) = 0.027 \text{ ppm}/^\circ K.$$

For a 30 $^\circ C$ change, this amounts to 0.81 ppm frequency change, and is small compared to say ± 5 ppm (over -20 $^\circ C$ to +70 $^\circ C$) temperature coefficient of the crystal itself.

The impedance of the bypass capacitor C_{by} should be much smaller than the external bias resistor that is in parallel. Otherwise the effective value of g_o (common-emitter output conductance) will increase due to a decrease in the effective Q of L in series with C_{by} (thus decreasing the equivalent parallel resistance R_p). A 1 nF capacitance has a 2 ohm impedance at 78 MHz, and is a good AC short.

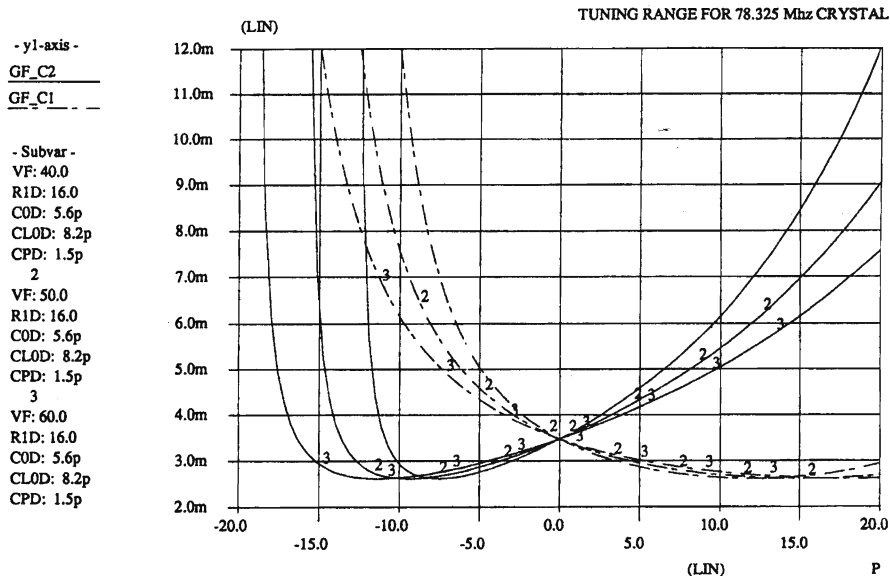


Figure 2.10a Tuning range at 78 MHz

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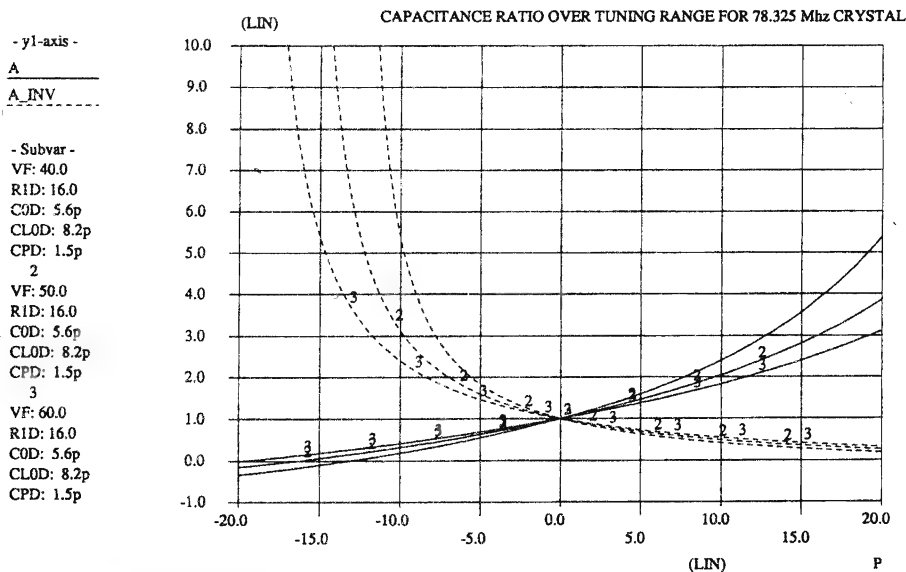


Figure 2.10b Capacitance ratio at 78 MHz

78.325 MHz Crystal Specifications

(All parameters to be measured with metallic holder and one lead grounded)

Application: 469.950 MHz (2 x 3 x 78.325 MHz)

Loaded Parallel Resonant Frequency, f_L : 78.325 MHz

Load Capacitance, C_L : 8 pF

Tolerance on C_L : ± 0.5 pF

Tolerance of f_L :

Calibration: ± 5 ppm at 25 °C

Total (temperature + aging, see Notes):

± 4.2 ppm over -10 °C to +55 °C

(@ 20 kHz TX channel width, ± 4 kHz deviation)

± 5.3 ppm over -10 °C to +55 °C

(@ 25 kHz TX channel width, ± 4.5 kHz deviation)

Overtone: third

Motional Resistance, R_1 : less than 20 Ω

Static Capacitance, C_0 : less than 6 pF

Pullability, F:

Definition: $F = (f_L - f_R)/f_R = C_1/[2(C_L + C_0)]$
in [ppm]

where f_R = unloaded series resonance frequency
 C_1 = motional capacitance

Requirement: $55 \text{ ppm} \leq F \leq 70 \text{ ppm}$ when $C_L = 8 \text{ pF}$

Holder: HC-52-SMD, with ground clamp or connection for metallic holder

Spurious rejection:

$R_N/R_1 \geq 2$ from $f_L/2.5$ to $2f_L$

where R_N is the dynamic resistance at the spurious frequency

Pager receivers

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Notes:

- The total frequency tolerance is based on a 3 dB loss of sensitivity of the UAA2080 due to frequency offset between transmitter and receiver.
- Aging requirements depend on the interval between service adjustments of the paging receiver. System aging is mainly determined by aging of the crystal, the tuning capacitor and the stray capacitance of the printed circuit board.

2) DESIGN OF A 48.039 MHz and 57.647 MHz COLPITTS OSCILLATOR

A third overtone 57.647 MHz crystal was used that gave similar gain margin and capacitance ratio over the tuning range, when compared with the 78 MHz crystal. The entire procedure was repeated as in the previous design. The results are shown in Figures 2.11a and 2.11b, for a crystal that measured the following on a network analyser.

$$\begin{aligned} R_1 &= 23 \, \Omega \\ C_1 &= 1.15 \, \text{fF} \\ C_0 &= 4.33 \, \text{pF} \\ L_1 &= 6.6 \, \text{mH} \\ C_{L0} &= 9.0 \, \text{pF at } 57.647 \, \text{MHz} \end{aligned}$$

The previous circuit of the 78 MHz oscillator thus works equally well with the 57 MHz crystal, except that now the restriction on the upper limit of C_2 tuning capacitor due to the mode selector inductor, is less severe (126 pF instead of 88 pF).

The following specifications for 48.039 MHz and 57.647 MHz are suitable for the UAA2080 oscillator.

48.039 MHz and 57.647 MHz Crystal Specifications

(All parameters to be measured with metallic holder and one lead grounded)

- Applications:
- a) 172.941 MHz (3 x 57.647 MHz)
 - b) 288.234 MHz (2 x 3 x 48.039 MHz)

Loaded Parallel Resonant Frequency, f_L :

- a) 57.647 MHz
- b) 48.039 MHz

Load Capacitance, C_L : 8 pF
Tolerance on C_L : $\pm 0.5 \, \text{pF}$

Tolerance of f_L :

Calibration: $\pm 5 \, \text{ppm}$ at 25°C
Total (temperature + aging, see Notes on previous page):

- a. $\pm 11.5 \, \text{ppm}$ over -10°C to $+55^\circ\text{C}$ (@ 20 kHz channel width, $\pm 4 \, \text{kHz}$ deviation)
 $\pm 14.4 \, \text{ppm}$ over -10°C to $+55^\circ\text{C}$ (@ 25 kHz channel width, $\pm 4.5 \, \text{kHz}$ deviation)
- b. $\pm 6.9 \, \text{ppm}$ over -10°C to $+55^\circ\text{C}$ (@ 20 kHz channel width, $\pm 4 \, \text{kHz}$ deviation)
 $\pm 8.7 \, \text{ppm}$ over -10°C to $+55^\circ\text{C}$ (@ 25 kHz channel width, $\pm 4.5 \, \text{kHz}$ deviation)

Overtone: third

Motional Resistance, R_1 : less than $30 \, \Omega$

Static Capacitance, C_0 : less than $5 \, \text{pF}$

Pullability, F :

Definition: $F = (f_L - f_R)/f_R = C_1/[2(C_L + C_0)]$ in [ppm]

where f_R = unloaded series resonance frequency
 C_1 = motional capacitance

Requirement: $50 \, \text{ppm} \leq F \leq 70 \, \text{ppm}$ when $C_L = 8 \, \text{pF}$

Holder: HC-52-SMD, with ground clamp/connection for metallic holder

Spurious rejection:

$$R_N/R_1 \geq 2 \text{ from } f_L/2.5 \text{ to } 2f_L$$

where R_N is the dynamic resistance at the spurious frequency

Pager receivers

UAA2080T VHF/UHF paging receiver

2.6 GENERAL GUIDELINES

The previous two oscillator designs assumed the availability of crystals with the measured equivalent circuit, based on which the gain and capacitance ratio versus pulling, were plotted using a computer. However, to specify a crystal for a required frequency, we must work the other way round. First an assumption is made for the transconductance. 9 millimhos could be used as a starting point (oscillator biased by a 1.8 K Ω external resistor). Next, equation (2.0) could be used to determine realistic values of C_0 , C_{L0} , and R_1 of the crystal. Finally, the dynamic capacitance C_1 has to be determined. It could either be explicitly specified, or equivalently, a range for the pullability F could be given. For either case, equation (2.11) must be plotted to show the variation of transconductance versus P , the tuning of the crystal in ppm, for various values of F . The range of F that gives the best result, should then be specified. Note that in equation (2.11), P is not directly used. Instead, the variable 'a' changes with 'x' as given in equation (2.9).

while 'x' changes with P as in equation (2.10). F could be translated into C_1 using equation (2.7).

When a large tuning (more than ± 10 ppm) range is required, then either C_2 may be tuned using a 13-50 pF tuning capacitor, or C_1 may be tuned using a 3-40 pF tuning capacitor, for an 8 pF nominal load capacitance. With C_2 tuned, it is more difficult to adjust the frequency precisely, since a small change in turning angle has a greater effect on the frequency. For the same reason, the temperature effect of C_2 is also larger. For tuning range less than ± 10 ppm, it is advisable to tune C_1 which allows easier tuning with smaller temperature effect.

In general, C_0 , R_1 and the parasitic C_p should be small. The load capacitance C_L should be as large as possible in order to minimise the effect of board and transistor capacitances. The pullability defined by F , should be just large enough to allow the required tuning range with practical ratios of C_1/C_0 .

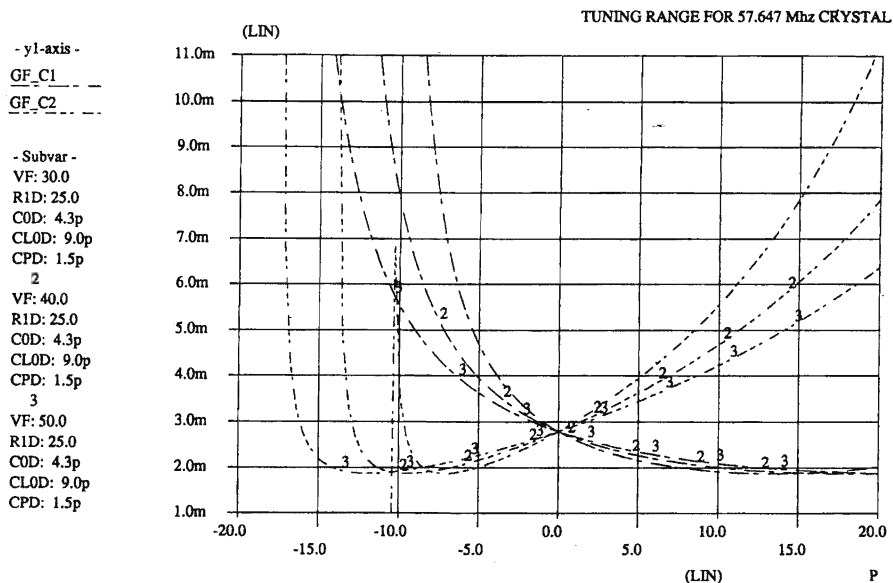


Figure 2.11a Tuning range at 57 MHz

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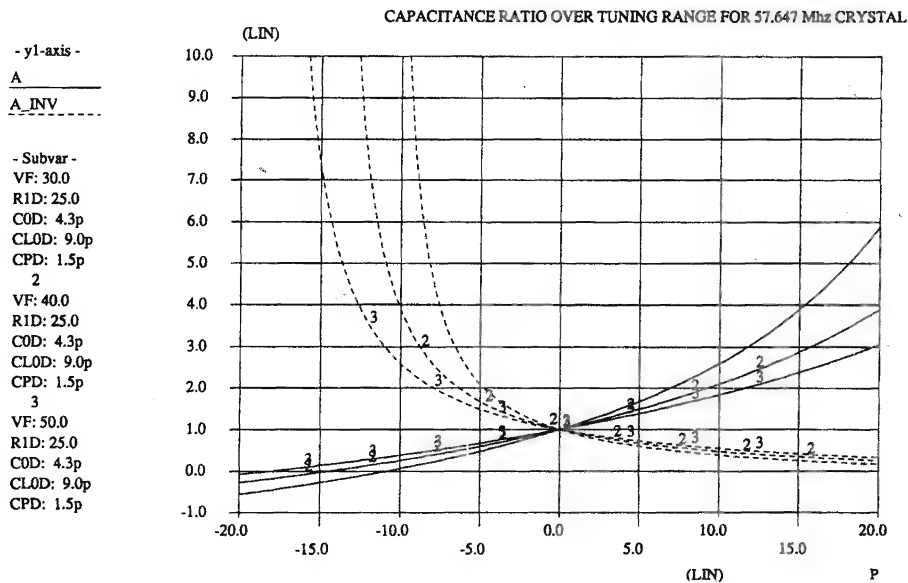


Figure 2.11b Capacitance ratio at 57 MHz.

Pager receivers

UAA2080T VHF/UHF paging receiver

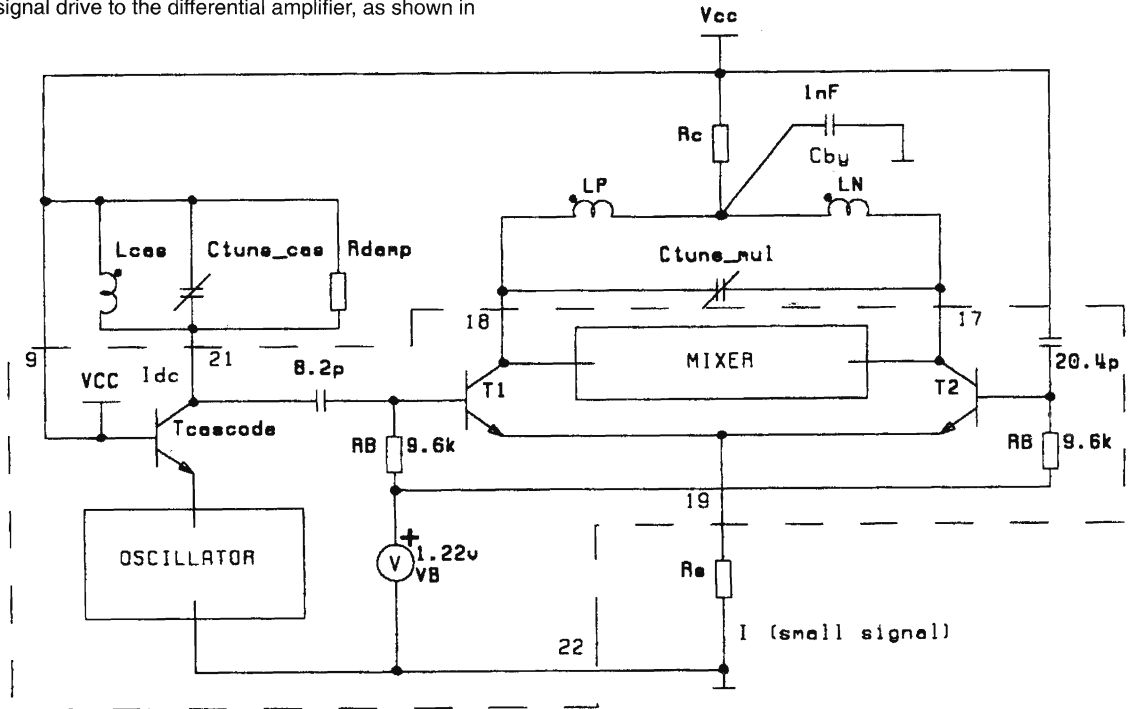
FREQUENCY MULTIPLIER

The Frequency Multiplier circuit in the UAA2080 consists of a) Differential Amplifier Frequency Multiplier, and b) Cascode Output Tank Circuit of the oscillator. Since the diff. amp. frequency multiplier influences component values of the cascode output tank circuit, it should be designed first. At this stage, the frequency multiplication factors m_1 and m_2 , and the oscillator DC current I_{dc} should be known (see previous chapter).

3.1 DESIGN OF DIFFERENTIAL AMPLIFIER FREQUENCY MULTIPLIER

The oscillator output tank provides an unbalanced large signal drive to the differential amplifier, as shown in

Fig. 3.0, where the base of transistor T1 is connected to the oscillator output through the 8.2 pF coupling capacitor. The differential amplifier transistors T1 and T2 are internally connected with the 1.22 Volts band-gap reference, through the two 9.6 k base resistors. The bias current is determined by the external tail resistor R_E . The base of T2 is at AC ground, due to the 20 pF bypass capacitor. The differential amplifier switches its tail current between the two collector outputs, at the frequency of the drive signal. Thus, the two collector currents are ideally square waves, with a relative phase of 180°. The parallel resonant tank circuit across the two collectors of the diff. amp., is tuned to the fundamental, or the 3rd, or the 5th harmonic component of the square wave collector current. The differential amplifier thus provides a frequency multiplication factor m_2 of 1, 3 or 5.



Circuit inside the dashed area is internal to the UAA2080T

Figure 3.0 Frequency Multiplier

Pager receivers

UAA2080T VHF/UHF paging receiver

Biasing

The differential signal voltage of amplitude V_m , across the collectors of T1 and T2, switches the upper sections of the I and the Q channel double balanced mixers. The diff. amp. circuit should be designed to provide a differential amplitude V_m greater than 150 mV, to fully switch the mixer's upper stage. Later, during receiver tuning, this initial large amplitude is reduced to 80-100 mV, in order to improve spurious rejection. This is described later. The tail current of the diff. amp., the quality factor of the tank, and the value of m_2 determine the mixer injection voltage V_m .

I is the small signal DC tail current

β is the current gain, taken as minimum 70

$I_s = 2.7973 \times 10^{-14}$ mA, the reverse saturation current

$R_B = 9.6$ k

$V_B = 1.22$ v

$V_T = 0.026$ mV

Figure 3.1 shows simulated values of R_E versus I . It must be noted that the DC current I is under small signal conditions, and is useful in determining the harmonic components of the collector output current. An R_E of 1.2 k Ω or more is sufficient for frequencies less than 500 MHz.

With reference to Fig. 3.0, the tail resistor R_E is given as

$$R_E = \frac{V_B - V_T \cdot \ln(I/2I_s)}{I} - \frac{R_B}{2\beta} \quad (3.0)$$

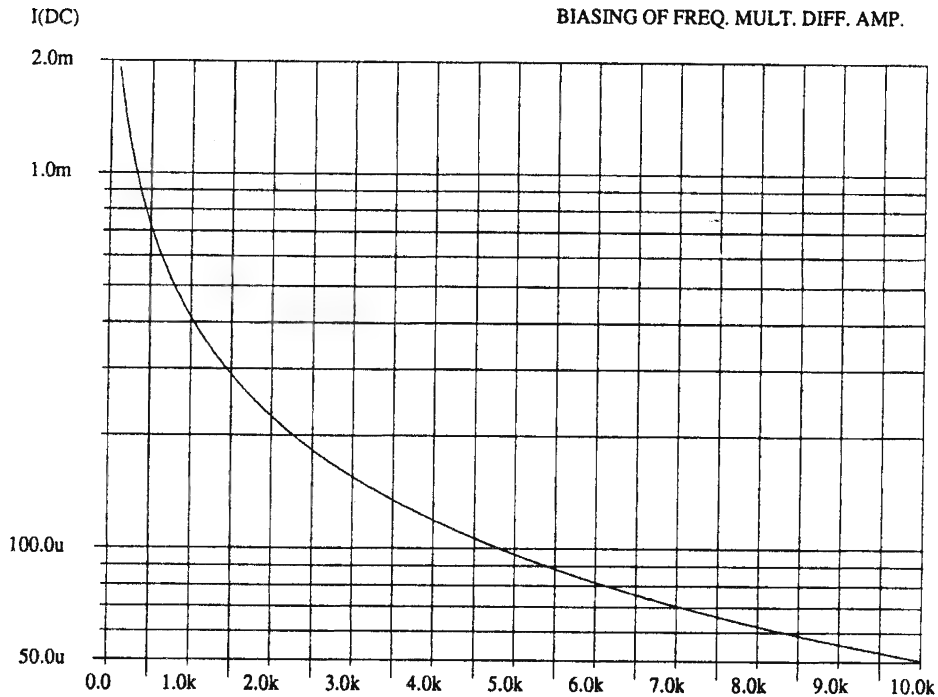


Figure 3.1 R_E versus small signal dc tail current

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Input Drive Level

If the balanced drive to an ideal differential amplifier is $V_D \cos(\omega t)$, as shown in Fig. 3.2, then the differential signal current that flows between the collectors is $I \tanh[V_D \cos(\omega t)/2V_T]$. This collector signal current can be represented by its Fourier series as $I_1 \cos(\omega t) + I_3 \cos(3\omega t) + I_5 \cos(5\omega t) + \dots$ (odd harmonics). As the drive V_D increases, the amplitudes of the harmonics reach their asymptotic values as given below.

$I_1 = 1.4/\pi$ for fundamental collector current (3.1a)

$I_3 = 1.4/(3\pi)$ for the 3rd harmonic collector current (3.1b)

$I_5 = 1.4/(5\pi)$ for the 5th harmonic collector current (3.1c)

(Note: the actual values of I_3 and I_5 are respectively about 85% and 75% of that given above, for reasons as given further below)

These asymptotic amplitude values correspond to the frequency components of an ideal square wave collector current with amplitude I . The variation of the odd harmonic current amplitudes with the drive V_D , is plotted in Fig. 3.3. The amplitudes have been normalised to the maximum value of the fundamental component i.e. $4 I/\pi$. To obtain more than 90% of the asymptotic value, the drive level V_D must be greater than 150, 350, and 500 mV for I_1 , I_3 , and I_5 respectively, for the case of an ideal differential amplifier at low frequencies.

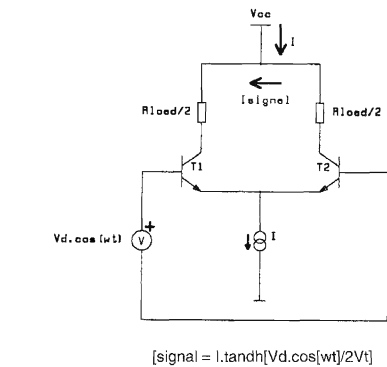


Figure 3.2 Ideal Differential Amplifier

The differential amplifier frequency multiplier of the UAA2080 as shown in Fig. 3.0, is non-ideal because the current source in the tail has been replaced by a bias resistor R_E . The effect is that the transistor T1 follows the drive signal for the positive half cycle, so it's collector current instead of limiting at I , increases proportionally with the instantaneous drive level, thus producing an unbalanced (not present in T2 collector) half-wave rectified sinusoidal current. As a result, there is an increase in I_1 , a decrease in I_3 and I_5 , an increase in the DC current, and an additional presence of even harmonic components in the differential collector current.

As a rule of thumb, due to the voltage following action of transistor T1, the actual asymptotic values of I_3 and I_5 are respectively about 85% and 25% of that shown in Fig. 3.3. There is an additional attenuation of I_3 and I_5 , due to high frequency roll-off, but it is small for frequencies less than 500 MHz.

Also, the actual large signal DC current, I_{act} is substantially greater than I , and is given by

$I_{act} = I + V_D/(\pi R_E)$, where (3.2)

The second term is due to the unbalanced half-wave rectified current in the collector of T1.

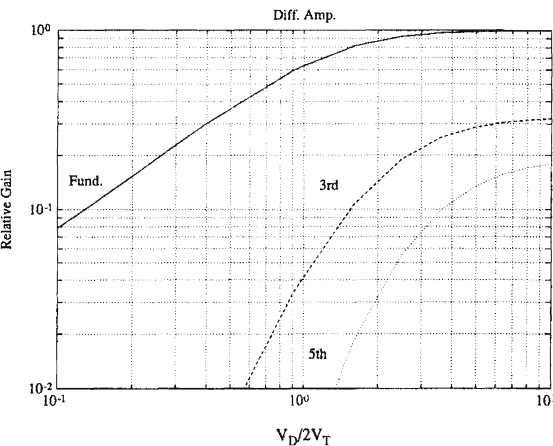


Figure 3.3 Harmonic Components versus Drive Level

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Tank Circuit

If the tank is tuned to the n^{th} harmonic ($n = 1, 3$ or 5) and if R_{mul} is its effective parallel resistance, then the peak differential voltage developed across the two collectors is

$$V_m = I_n R_{\text{mul}}, \text{ with } n = 1 \text{ or } 3 \text{ or } 5 \tag{3.3}$$

The effective parallel resistance of the tank is
$$R_{\text{mul}} = 2R_{\text{par_Lp}} \text{ parallel } R_{\text{par_mix}} \tag{3.4}$$

$R_{\text{par_Lp}}$ is the parallel resistance of either coils with inductance of L_p at the receiver frequency f_{RX} .

$R_{\text{par_Lp}} = Q_{Lp} \cdot (2\pi f_{\text{RX}} L_p)$, where Q_{Lp} is the quality factor of L_p and L_N at the receiver frequency. (3.5)

$R_{\text{par_mix}}$ is the parallel resistance of the LO-input of the mixers connected in parallel with the diff. amp. output. The simulated curve for $R_{\text{par_mix}}$ is given in Fig. 3.4. The simulation was done with the mixer in a non-switched state, and with the diff. amp. tail resistor R_E of $1.2 \text{ k}\Omega$.

The receiver frequency is $f_{\text{RX}} = 1/2\pi\sqrt{L_{\text{mul}} C_{\text{mul}}}$, with (3.6)

$L_{\text{mul}} = 2L_p$ (multiplier tank inductances $L_p = L_N$) (3.7)

$C_{\text{mul}} = C_{\text{tune_mul}}$ (multiplier tuning capacitor) + C_{p_mul} (parasitics & board capacitance) + $C_{\text{par_mix}}$ (mixer & diff. amp. capacitance) (3.8)

The value of $C_{\text{par_mix}}$ may be taken as 2 pF .

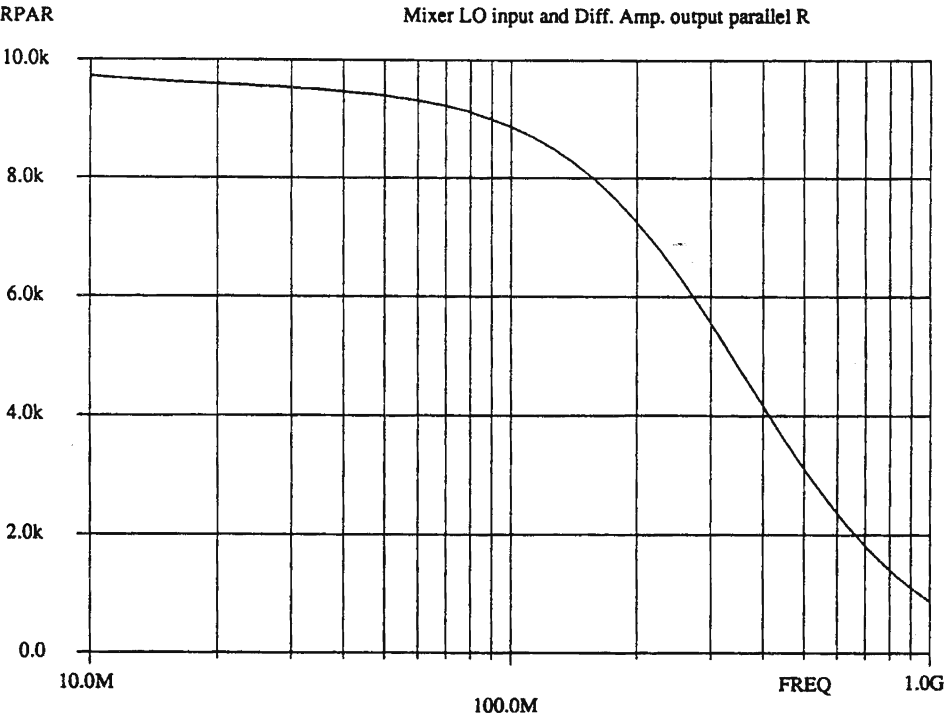


Figure 3.4 Mixer LO-input parallel resistance

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Mixer Biasing

The resistance R_C in the collector circuit provides a DC voltage drop to prevent saturation of the switching transistors in the mixer's upper section (the mixer is a Gilbert Multiplier). If the DC voltage drop is larger, then the upper stage (switching transistors) performance of the mixer improves, but the lower stage of the mixer (RF input) tends to saturate when the battery voltage is low. At a battery voltage of 2 volts, a 300 mV drop across R_C ensures equal collector-emitter voltage for the upper and lower stage transistors. So,

$$R_C = 0.3/I_{act} \text{ [volt/amp] approximately.} \quad (3.9a)$$

To optimise receiver performance at an arbitrary battery supply voltage V_P , the above equation becomes

$$R_C = (0.5V_P - 0.7)/I_{act} \text{ [volt/amp]} \quad (3.9b)$$

With the value of R_C so chosen, the receiver performance would be marginally better for supply voltages more than V_P .

The above equations indicate that the value of R_C depends on the multiplier drive level V_D which strongly influences I_{act} .

Spurious Rejection

In chapter 2, it was mentioned that strong spurs occurred at $f_{RX} \pm N.f_L$ ($N = 1, 2, 3, \dots$), and a general frequency multiplication scheme was devised to improve spurious rejection. Apart from a suitable frequency multiplication scheme, circuit components and the board layout also determine to a large extent the spurious rejection. Strong spurs at the above mentioned frequencies, occur largely due to spurious signals being present at those frequencies, at the mixer LO-input. Therefore the tank circuit at the mixer LO-input (pins 17 and 18) should have a large loaded Q in order to attenuate the spurious signals. The attenuation, A , of the parallel resonant tank, at a frequency Δf away from its tuned frequency f_o , is

$$A = (1+S^2)^{1/2} \text{ where } S \approx 2Q.\Delta f/f_o, \text{ and } Q = R(C/L)^{1/2}$$

R is the loaded parallel resistance, and, L and C are the total parallel inductance and capacitance. To improve

spurious rejection, Q should be increased by increasing the ratio of R/L . The unloaded Q of ceramic core surface mount inductors increases slightly for decreasing inductance values. The largest loaded Q is thus attained when the parallel resistance of the inductance is much lower than the parallel load resistance of the rest of the circuit, and this is achieved by using the lowest possible inductance values. As the value of L is decreased, the required C increases. Large tuning capacitance have smaller Q , and thus should be replaced by a fixed SMD capacitor in parallel with a small tuning capacitor (that covers the spreads in component values of the inductance and the fixed capacitor).

Spurious rejection at harmonics (especially 3rd harmonic) of the receiver frequency can be substantially increased by reducing the LO injection level to the mixer. As is shown in Fig 3.3, for large drive levels (greater than 250 mV peak differential), the 3rd harmonic is attenuated by a factor 3. However, if the drive level is reduced to 100 mV, the 3rd harmonic is about 6 times smaller than the fundamental. At 50 mV drive, the 3rd harmonic is 16 times smaller than the fundamental, while the conversion gain at the fundamental has reduced by a factor 2 when compared with the gain at large drive levels. The optimal mixer LO injection amplitude, V_M , is in the range 80-100 mV.

For larger spurious rejection, the smallest value of inductance (and hence large loaded Q) should be used for L_P and L_N of Fig. 3.0, in order to increase attenuation at frequencies $f_{RX} \pm N.f_L$. The previous equations that lead to the value of L_P and L_N assume that the collector current of the diff. amp. is fully switched. To improve the spurious rejection, the diff. amp. drive level V_D has to be kept minimal, but this leads to a reduction in the collector current of the diff. amp. and thus a reduction in V_M . It is recommended that the lowest inductance for L_P and L_N be used that can be practically tuned, and after that the DC current of the diff. amp. be selected in order to make V_M about 150-200 mV. The cascode tank circuit is then either damped (by reducing the resistance of a parallel trimpot) or detuned (by C_{tune_cas}), to reduce the IF voltage 85-90% of its maximum value. This ensures that the LO injection V_M to the mixer is in the optimal range as mentioned earlier, and that the diff. amp. drive V_D is minimal.

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The bypass capacitor C_{BY} across R_C greatly improves spurious rejection by shorting all common mode signals injected into the mixer's LO inputs. Even though it degrades the balance in the differential signal across the collectors of transistors T1 and T2, corresponding to a small loss in sensitivity (less than $1/2$ dB at 470 MHz), the improvement in spurious rejection is quite substantial.

Buffer Amplifier

If the differential amplifier is used as a buffer amplifier ($m_2 = 1$), then the fundamental collector current I_1 will have a high frequency roll-off as shown in Fig. 3.5. The envelope of the peaks in the graph give the value of I_1 , normalised to its value at low frequencies. This simulation has been done with R_E of 1.2 k Ω , along with an infinite quality factor for both L_p and L_n . The 3 dB point is at a much lower frequency than when m_2 is 3 or 5, and is due to the Miller effect.

The voltage gain, $A_v = V_m/V_D$, at low frequencies is

$$A_v = g_m R_{mul}, \text{ where } g_m = I/V_T \text{ [A/V]} \quad (3.10)$$

For example, when the DC current I is 360 μ A, g_m is 13.8 mhos, and the voltage gain for a 1 k Ω R_{mul} is 13.8. To get a mixer LO drive, V_m of 150 mV, the required V_D from the oscillator cascode output is 150 mV/13.8 i.e. about 11 mV only. To get such small values of V_D , the cascode output tank must be damped by a small parallel resistance. Usually, it turns out that this resistance is much smaller than R_{mul} (between 10 and 100 Ω only), and so one may tend to dispense with the tank circuit altogether. However, when $m_1 > 1$, the levels of unwanted and stronger sub-harmonic frequency components at the cascode output, should be kept less than V_D , and because of this, the tank circuit is essential, although it is no longer necessary to tune it (due to the large damping, there is negligible change in amplitude with tuning).

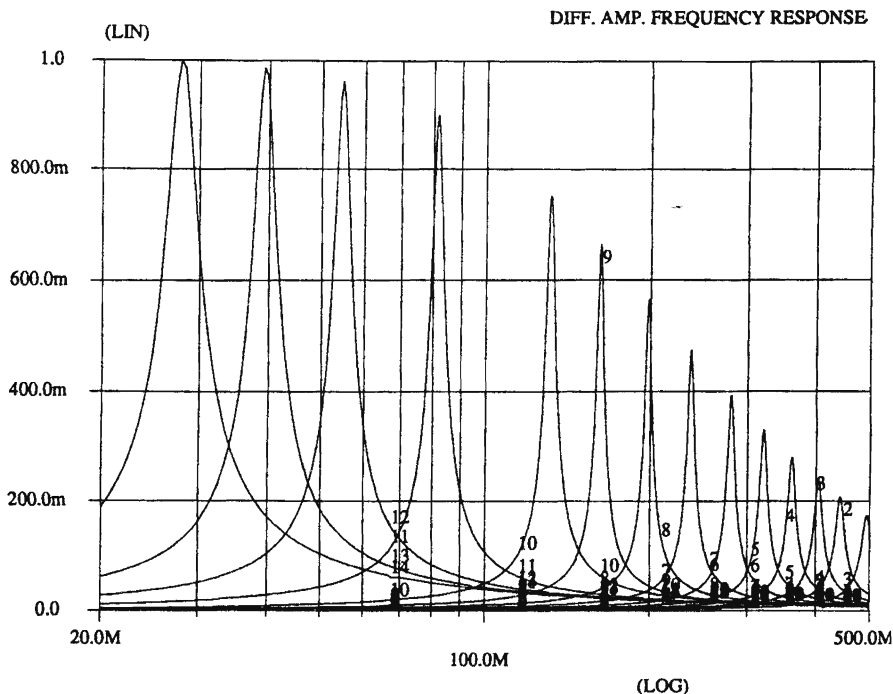


Figure 3.5 High Frequency Attenuation of I_1

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3.2 DESIGN OF OSCILLATOR TANK

The tank circuit at the cascode output of the oscillator, can be resonant at the crystal oscillation frequency, or its second harmonic, thus providing a multiplication factor m_1 of 1 or 2. As can be seen in Fig. 2.6 of the previous chapter, the 2nd harmonic of the collector current, varies more than the fundamental, as g_m/g_{m0} changes with the tuning of the crystal. For this reason, the gain margin g_{m0}/g_m should be sufficiently large over the tuning range if the 2nd harmonic frequency is used. The 3rd harmonic component (for the case when $m_1 = 3$) should be used with extreme care, since it shows an even larger variation with the crystal tuning.

Theoretically, the tank components should be chosen to provide sufficient drive to the differential amplifier. The amplitude of this drive signal V_D is related to the frequency multiplication factor m_2 of the differential amplifier, and is given in Table 3.0. The upper limits of the drive levels given in this table, are targeted to attain the asymptotic value of the current amplitude curves shown in Fig. 3.3. However, these large drive levels degrade spurious rejection of the receiver (even though the receiver sensitivity is best), and thus a compromise must be made between obtaining optimal drive levels, and achieving good spurious rejection. The application circuit design should aim at maintaining the minimal drive level as given in table 3.0, over the tuning range of the crystal oscillator. The multiplication factor of 5 requires a large drive level, and hence the spurious rejection would be worse than if m_2 was 3, for the same receiver frequency.

Drive Signal Amplitude, V_D (mV)	m_2 , Frequency Multiplication Factor of Diff. Amp.
150 to 250 *	1
250 to 400	3
350 to 550	5

* actual range is much smaller, as described below.

Table 3.0 Diff. Amp. Drive Level for optimal sensitivity

When $m_2 = 1$, then it is not necessary to fully switch the diff. amp. because its fundamental current I_1 is quite large, and more than sufficient to produce a V_M of

150 mV. The drive level V_D should be 10-50 mV only, and not 150-250 mV as given in the table above.

Component Values for Tank Circuit

The following are required in order to determine the tank circuit components.

- Oscillator large signal bias current, I_{dc} , and multiplication factor m_1
- Drive amplitude, V_D , for the diff. amp.
- Tail resistor, R_{E1} , of the diff. amp.

Denote I_{tank} as the harmonic component of the cascode collector current selected by the parallel resonant tank. Over the oscillator tuning range, the fundamental current component varies from $2I_{dc}$ to about $1.5I_{dc}$ (at extremes). The second harmonic component varies from $1.6I_{dc}$ to I_{dc} approximately. To be on the safe side, take

$$I_{\text{tank}} = 1.5I_{dc} \text{ for } m_1 = 1, \text{ and} \\ I_{\text{tank}} = I_{dc} \text{ for } m_1 = 2$$

The required tank parallel resistance resistance, R_{cas} , is given by

$$R_{\text{cas}} = V_D / I_{\text{tank}} \quad (3.11a)$$

$$R_{\text{cas}} = R_{\text{par_Lcas}} \text{ parallel } R_{\text{par_diff}} \text{ parallel } R_{B1}, \text{ where} \quad (3.11b)$$

$R_{\text{par_Lcas}}$ is the parallel resistance of the inductance L_{cas} , R_{B1} is the base bias resistor (9.6 k Ω) of the diff. amp., and $R_{\text{par_diff}}$ is the parallel resistance of the diff. amp. input. The large parallel resistance of the oscillator cascode output, may be neglected in determining R_{cas} .

$$R_{\text{par_Lcas}} = Q_{L_{\text{cas}}} (2\pi f_{\text{cas}} L_{\text{cas}}), \text{ with } f_{\text{cas}} = m_1 f_{L0} \text{ and } Q_{L_{\text{cas}}} \text{ the} \\ \text{quality factor of } L_{\text{cas}} \text{ at frequency } f_{\text{cas}} \quad (3.12)$$

$R_{\text{par_diff}}$ is difficult to calculate or simulate, since the input impedance of the diff. amp. varies with the instantaneous level of the drive signal $V_D \cos(\omega t)$. However, its value lies approximately within these limits:

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$3V_T/I$ (small-signal input impedance) $< R_{\text{par_diff}} < 3R_E$ (voltage follower input impedance). A value of $2BV_T/I$ may be assumed for practical purposes. (3.13)

The cascode output frequency, f_{cas} , is

$$f_{\text{cas}} = m_1 f_{L0} = f_{RX}/m_2 = 1/2\pi\sqrt{(L_{\text{cas}} C_{\text{cas}})}, \text{ where} \quad (3.14)$$

$$C_{\text{cas}} = C_{\text{tune_cas}} \text{ (tuning capacitor)} + C_{\text{par_diff}} \text{ (diff. amp. input \& cascode output)} + C_{\text{p_cas}} \text{ (parasitics \& board capacitance)} \quad (3.15)$$

If $m_2 = 1$, then $C_{\text{par_diff}}$ increases by a factor $(1/V_T)R_{\text{mul}}C_{\text{bc_T1}}$, which is the Miller Capacitance. $C_{\text{bc_T1}}$ is the base-collector capacitance of T1. For m_2 not equal to one, the Miller Capacitance may be ignored, and $C_{\text{par_diff}}$ may be taken as 3 pF.

Spurious Rejection

As discussed in the section on spurious rejection of the diff. amp. frequency multiplier, the value of L_{cas} may be taken as low as possible to obtain a high Q. This will improve spurious rejection by suppressing the amplitudes at harmonics (and subharmonic if $m_1 > 1$) of the oscillator cascode output frequency. However, the spurious rejection is more strongly influenced by the drive level V_D , which should be kept minimal.

With crystal frequencies more than about 60 MHz, and along with $m_1 = 2$, there is a large (about 50%) variation in I_{tank} with crystal tuning, so a variable damping resistor (with a maximum value about 4 times the parallel tank resistance R_{cas}) may be used in parallel with the tank, to adjust the amplitude V_D . After initial tuning of the receiver, the damping resistor is reduced from its maximum value, till the IF level drops to 50%. This reduces V_D so that the differential amplifier is not overdriven. C15 is now tuned maximum IF level (on pins TPI and TPQ). The damping resistor is then increased to maximum, and the IF level noted. The damping resistor is then decreased so that the IF level is reduced by about 10%. This ensures that V_D is just at the optimum level.

When $m_1 = 1$, there is smaller variation in I_{tank} with crystal tuning. For the case $m_1 = 1$ and $m_2 > 1$, the damping

resistor is not really required, and the tank may instead be detuned by the tuning capacitor, $C_{\text{tune_cas}}$, to reduce the IF level by about 10%.

If the oscillator is designed to provide a large gain margin over the entire tuning range (by providing sufficient bias current or by having smaller tuning range for the crystal), then the variation in I_{tank} would be very small, and the damping resistor may be dispensed with, and instead the value of L_{cas} and its Q may be appropriately taken to obtain the minimum required drive level V_D .

3.3 EXAMPLES

1) RECEIVER FREQUENCY OF 469.95 MHZ

From Table 2.0 of the previous chapter, $m_1 = 2$ and $m_2 = 3$ at 469.95 MHz. The oscillator frequency is thus $469.95/(2 \times 3) = 78.325$ MHz. The design of this oscillator has been covered in the previous chapter.

Design of the Diff. Amp. Tank Circuit

The first step is to fix the bias current of the diff. amp. at a reasonably low level, say below 500 μA . Choosing a 1.2 k tail resistor, Fig. 3.1 indicates about 360 μA quiescent current. The other way round, a 360 μA tail current gives a value of 1.2 k for R_E , using equation (3.0). The amplitude of the third harmonic collector current is, from (3.1b)

$$I_3 = 360 \times 4/(3\pi) \times 85\% = 130 \mu\text{A}$$

From (3.3), for mixer drive voltage $V_m = 150$ mV, the effective parallel resistance required is

$$R_{\text{mul}} = 0.15 \text{ v}/130 \mu\text{A} = 1.15 \text{ k}\Omega.$$

The parallel resistance of the mixer LO_input and diff. amp. output, $R_{\text{par_mix}}$, is about 3 k Ω at 470 MHz, as given in Fig. 3.4. From (3.4), the required parallel resistance of the tank inductors, is then

$$2R_{\text{par_Lp}} = 1.15 \times 3.4/(3.4-1.15) = 1.74 \text{ k}, \text{ or } R_{\text{par_Lp}} = 869 \Omega$$

If Q_{Lp} is 50, then $L_p \geq 5.9$ nH from (3.5).

This implies $L_{\text{mul}} = 2L_p \geq 12$ nH

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Using equation (3.6) we get $C_{mul} \leq 9.5$ pF.

With a 1 pF board and parasitic capacitance C_{p_mul} , and C_{par_mix} of 2 pF, the tuning capacitance is,

$$C_{tune_mul} \leq 6.5 \text{ pF}$$

The closest inductance values are $L_p = L_n = 8$ nH, and the corresponding $C_{Tune_mul} = 2.5\text{-}6$ pF

From Table 3.0, the minimal drive level $V_D = 250$ mV for $m_2 = 3$. The large signal DC current is thus, from (3.9a)

$$I_{act} = 360 \times 10^{-6} + 0.25/(\pi 1200) = \text{about } 425 \text{ } \mu\text{A}$$

The collector resistor R_C is, from (3.9),

$$R_C = 0.3 \text{ V}/425 \text{ } \mu\text{A} = 704 \text{ } \Omega. \text{ A standard value of } 680 \text{ } \Omega \text{ was used.}$$

Design of Cascode Output Tank

The design of a 78.325 MHz oscillator in the previous chapter gave a large signal oscillator DC current of 280 μ A. As $m_1 = 2$, the signal current to be amplified by the tank is $I_{tank} = I_{dc} = 280 \text{ } \mu\text{A}$.

To get a drive level of 400 mV peak (for $m_2 = 3$), the required parallel tank resistance is

$$R_{cas} = 0.4 \text{ V}/450 \text{ } \mu\text{A} = 1.43 \text{ k}\Omega$$

The value of the diff. amp. small signal DC current is 360 μ A, so from (3.13),

$$R_{par_diff} \approx (2 \times 70 \times 0.026)/360 \text{ } \mu\text{A} = 10.1 \text{ k}\Omega.$$

This in parallel with the bias resistor R_B of 9.6 k gives 4.9 k Ω

From (3.11b), the required parallel resistance of the tank inductance is

$$R_{par_Lcas} = 4.9 \times 1.43/(4.9 - 1.43) = 2 \text{ k}\Omega \text{ approximately.}$$

The tank resonance frequency is

$$f_{cas} = m_1 f_{L0} = 2 \times 78.325 = 156.65 \text{ MHz}$$

A wide range of available inductances and capacitances can be resonant at this frequency. If the quality factor of the inductance is too high, i.e. $R_{pas_Lcas} \gg 2 \text{ k}\Omega$, then a damping resistor may be required across the tank in order to limit the signal level to below 600 mV. The table below gives the range of C_{cas} , L_{cas} and Q_{Lcas} . It uses equations (3.12) and (3.14).

Ccas			
10 pF		50 pF	
Lcas	QLcas	Lcas	QLcas
100 nH	20	20 nH	100

An inductance of 100 nH (with a quality factor of 50 at 156 MHz) was used. The required tuning capacitor is given as follows, using equation (3.15).

The board capacitance C_{p_cas} is taken as 1 pF, and C_{par_diff} as 3 pF.

$$C_{tune_cas} = C_{cas} - C_{par_diff} - C_{p_cas}$$

$= 10 - 1 - 3 = 6$ pF i.e. a tuning range of 3-10 pF would suffice.

The measured V_D was nearly 600 mV i.e. more than 400 mV because the Q of the inductance was more than 20. A smaller inductance (to reduce V_D) was not used, in order to allow a 50% reduction in V_D that occurred when the crystal was pulled by more than 10 ppm. To reduce V_D (to improve spurious rejection) at the nominal frequency, a 5 k Ω variable resistor was used for damping. The damping resistor was adjusted so that the IF level was reduced to about 90% of its peak value (that corresponding to the maximum value of the damping resistor).

If the crystal tuning is less than 10 ppm, then the damping resistor is not required, and instead a lower inductance value (68 nH) can be taken. The IF level can be reduced by simply detuning the tank.

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2) RECEIVER FREQUENCY OF 288.234 MHz

The appropriate multiplication factors are $m_1 = 2$ and $m_2 = 3$ for 288 MHz, as given in Table 2.0 of the previous chapter. The oscillator frequency is therefore 288.234 MHz/(2 x 3) = 48.039 MHz.

Design of the Diff. Amp. Tank Circuit

The mixer parallel resistance, $R_{\text{par_mix}}$, is about 5.8 k Ω at 288 MHz i.e. nearly double of its value at 470 MHz, as can be seen in Fig. 3.4. The component I_3 is 130 μA when R_E is 1.2 k Ω , as in the previous example.

From (3.3), for mixer drive voltage $V_m = 150$ mV peak, the effective parallel resistance required is

$$R_{\text{mul}} = 0.15 \text{ V}/130 \mu\text{A} = 1.15 \text{ k}\Omega.$$

From (3.4), the required parallel resistance of the tank inductors, is then

$$2R_{\text{par_Lp}} = 5.8 \times 1.15/(5.8-1.15) = 1.43 \text{ k}, \text{ or } R_{\text{par_Lp}} = 717 \Omega$$

If Q_{Lp} is 50, then $L_p \geq 8$ nH from (3.5).

This implies $L_{\text{mul}} = 2L_p \geq 16$ nH

Using equation (3.6) we get $C_{\text{mul}} \leq 19$ pF.

However, to improve spurious rejection, the drive V_D had to be reduced, and as a result, the inductances L_p and L_n were increased to 18 nH each (Q of 50) in order to maintain 80-100 mV for V_m . $C_{\text{tune_mul}}$ of 3-10 pF was the closest to the required 8.5 pF capacitance to tune out 36 (i.e. 18+18) nH. Note that there is a 1 pF board and parasitic capacitance $C_{\text{p_mul}}$, and about 2 pF $C_{\text{par_mix}}$.

The collector resistor R_C from (3.9), remains the same as before, i.e. 680 Ω .

Design of Cascode Output Tank

The 48.039 MHz Colpitts oscillator gives a large signal oscillator DC current of 280 μA , when it is biased by a 1.8 k Ω resistor, as discussed in the previous chapter. As $m_2 = 2$, the signal current to be amplified by the tank is $I_{\text{tank}} = I_{\text{dc}} = 280 \mu\text{A}$, at 96.078 MHz.

L_{cas} of 33 nH (Q of 50) gave V_D of about 375 mV. It was tuned by a 9-40 pF tuning capacitor in parallel with a 56 pF fixed capacitor. Larger inductances though increased V_D , but made the spurious rejection worse. Damping resistor was not necessary because at 48 MHz, the oscillator has a large gain margin and the amplitude V_D was nearly constant over ± 15 ppm tuning range. Instead, the IF level was reduced by detuning the tank.

3) RECEIVER FREQUENCY OF 172.941 MHz

The appropriate multiplication factors are $m_1 = 1$ and $m_2 = 3$ for 173 MHz, as given in Table 2.0 of the previous chapter. The oscillator frequency is thus 172.941/(1 x 3) = 57.647 MHz. The design of this oscillator has been covered in the previous chapter.

Design of the Diff. Amp. Tank Circuit

The mixer parallel resistance is about 7.5 k Ω at 173 MHz and the component I_3 is larger than the I_5 of the previous example. Thus it would seem possible to reduce the tail current and still achieve sufficient mixer drive voltage. With an R_E of 2.2 k Ω , the tail current I is about 200 μA , as seen in Fig. 3.1. Taking this as the starting point, the circuit feasibility is studied next. The amplitude of the third harmonic collector current is, from (3.1b)

$$I_3 = 200 \times 4/(3\pi) \times 85\% = 72 \mu\text{A}$$

From (3.3), for mixer drive voltage $V_m = 150$ mV, the effective parallel resistance required is

$$R_{\text{mul}} = 0.15 \text{ V}/72 \mu\text{A} = 2.08 \text{ k}\Omega.$$

The parallel resistance of the mixer L_{O_input} and diff. amp. output, $R_{\text{par_mix}}$, is about 7.5 k Ω at 173 MHz, as given in Fig. 3.4. From (3.4), the required parallel resistance of the tank inductors, is then

$$2R_{\text{par_Lp}} = 7.5 \times 2.08/(7.5-2.08) = 2.8 \text{ k}\Omega, \text{ or } R_{\text{par_Lp}} = 1.4 \text{ k}\Omega$$

L_p and L_n of 33 nH each, were used. Each of them had a parallel resistance of 1.2 k Ω . The tuning capacitor was 5-20 pF.

From Table 3.0, the drive level $V_D = 400$ mV for $m_2 = 3$. The large signal DC current is thus

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$$I_{\text{act}} = 200 \times 10^{-6} + 0.4/(\pi 2200) = 258 \mu\text{A}$$

The collector resistor R_C from (3.9), is 1.16 k Ω , and the closest value of 1.2 k Ω was used.

Design of Cascode Output Tank

The design of a 57.647 MHz oscillator in the previous chapter gave a large signal oscillator DC current of 280 μA . As $m_1 = 1$, the signal current to be amplified by the tank is $I_{\text{tank}} = 1.5I_{\text{dc}} = 420 \mu\text{A}$.

To get a drive level of 400 mV (for $m_2 = 3$), the required parallel tank resistance is

$$R_{\text{cas}} = 0.4/420 \mu\text{A} = 952 \Omega$$

The value of the diff. amp. small signal DC current is 100 μA , so from (3.13),

$$R_{\text{par, diff}} \approx (2 \times 70 \times 0.026)/100 \mu\text{A} = 36 \text{ k}\Omega.$$

This is in parallel with the bias resistor R_B of 9.6 k gives 7.8 k Ω

From (3.11), the required parallel resistance of the tank inductance is

$$R_{\text{par, Lcas}} = 7800 \times 952/(7800-952) = 1.1 \text{ k}\Omega \text{ approximately.}$$

The tank resonance frequency is $f_{\text{cas}} = m_1 f_{\text{LO}} = 57.647 \text{ MHz}$, and the inductance L_{cas} from (3.12) is 61 nH, when its Q is 50.

An inductance of 68 nH (with $Q > 50$) for L_{cas} was used. C_{cas} of 112 pF is required for tuning. An 82 pF fixed capacitor in parallel with 13-50 pF tuning capacitor was used.

Improvements for Spurious Rejection

To improve spurious rejection, the cascode tank had to be detuned in order to reduce the amplitude V_D from 400 mV to about 250-300 mV. Because of this, the amplitude V_m decreased below 80 mV, and the sensitivity decreased by 0.3 dB. To restore the sensitivity without degrading the spurious rejection, V_m had to be increased without increasing V_D . Therefore, the DC current of the

diff. amp. was increased by biasing it with a 1.2 k Ω tail resistor R_E . The DC current of the diff. amp. is then about 430 μA , and the value of R_C is 700 Ω for a 300 mV drop. 680 Ω was taken as a suitable value.

An alternative solution is to make $m_1 = 3$ and $m_2 = 1$, thus tuning the oscillator output directly to the third harmonic of the crystal oscillation frequency. Since the diff. amp. now has a large gain, therefore V_D can be made very small (less than 50 mV). L_{cas} of 27 nH with a parallel fixed capacitance of 27 pF, was taken. A damping potentiometer of 100 Ω was used to reduce V_D sufficiently till the IF level dropped by 10%. Because of the large damping, it was not necessary to tune the capacitance. Note that the tank circuit is still required (instead of replacing it by the damping potentiometer) because the strong subharmonics signals ($x1$ and $x2$ of the crystal frequency) have to be suppressed. This solution gives a better spurious rejection because V_D and the subharmonics are very small. Even with a 100 Ω potentiometer, it was difficult to reduce the IF level by 10%, therefore the DC current of the diff. amp. had to be reduced by increasing R_E from 1.2 k Ω to 2.2 k Ω . The value of R_C is then 1.5 k Ω for a 300 mV drop (I is about 200 μA). Note that even when the potentiometer is set to 0 Ω , V_D is still quite large due to the drop across the package lead and track inductance.

PHASE SHIFTER

The phase shifter is intended to split the received RF signal into two paths, the I and the Q channels, that are in phase quadrature (90° relative phase), but have equal amplitudes. The I and the Q RF signals are mixed with the LO (local oscillator) signal to produce I and Q audio signals that maintain the same relative phase and amplitude as their RF counterpart. In order to have optimal performance of the demodulator, these audio signals, and hence the I and the Q RF signals, must be in phase quadrature, and should have equal amplitudes.

The impedance of the RF input of each mixer together with reactances connected in series, form the phase shift circuit, as shown in Fig. 4.0. In that figure, Z_m is the differential impedance of the mixer RF input. Z_1 and Z_2 are reactances connected in series with the mixers so that the current in one branch is lagging by 45°, while in the other it is leading by 45°, relative to the common input

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RF signal that is fed to the phase shifter from the LNA output through a power matching circuit. The two parallel branches of the phase shift circuit, produce a resultant real impedance, R_{phase} , which is power matched to the LNA output.

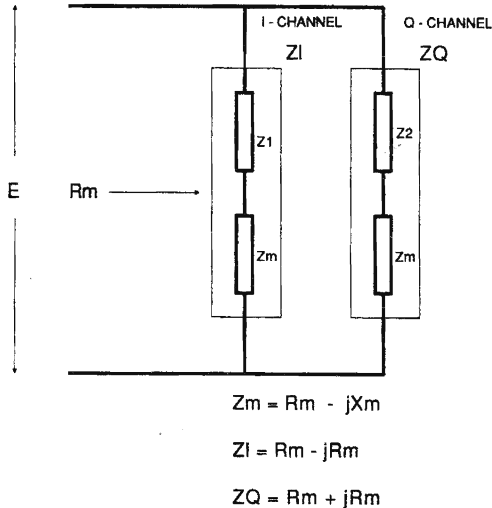


Figure 4.0 Phase Shifter

4.1 Detailed Analysis

To get phase quadrature and equal amplitudes for the I and the Q audio signals, the RF signal voltage at each mixer input must be equal in magnitude, but with the required 90° relative phase. This implies that the RF current through each mixer input impedance Z_m , be equal in magnitude, but with a 90° relative phase difference.

The mixer RF input impedance is represented as $Z_m = R_m - jX_m$. The negative sign is due to its parallel input capacitance, including parasitics.

The resultant impedances in the I and the Q phase shift branches are respectively

$$Z_I = Z_m + Z_1 \quad \text{and} \quad Z_Q = Z_m + Z_2 \quad (4.0)$$

If Z_1 and Z_2 are purely reactive, then the Z_I and Z_Q vectors lie on the vertical line passing through R_m , as shown in

Fig. 4.1. As it is required that the RF current amplitude in each branch be equal, therefore the magnitudes of Z_I and Z_Q must also be equal. These two conditions together imply that Z_I and Z_Q have absolute phases of -45° and $+45^\circ$ degrees respectively.

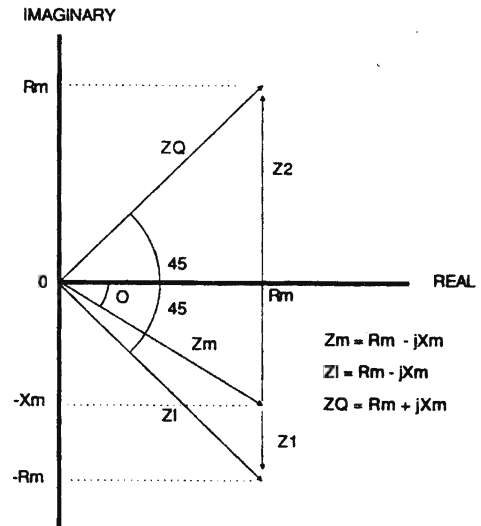


Figure 4.1 Impedance Diagram

The resultant impedance of the phase shift network is,

$$Z_{\text{phase}} = Z_I \text{ parallel } Z_Q \quad (4.1)$$

$$\text{From Fig. 4.1 it is apparent that } Z_I = R_m - jR_m \text{ and } Z_Q = R_m + jR_m \quad (4.2)$$

Substituting these values in the equation for Z_{phase} , we get

$$Z_{\text{phase}} = R_m + j0 \quad (4.3)$$

Hence the resultant impedance is real, given by $R_{\text{phase}} = R_m$

Denote Θ_m as the phase magnitude of Z_m i.e. $\Theta_m = \arctan(X_m/R_m)$. Figure 4.1 is for the case $R_m \geq X_m$, i.e. the angle $\Theta_m \leq 45^\circ$. The reactance Z_1 is capacitive. However,

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if $R_m < X_m$, i.e. $\Theta_m > 45^\circ$, then Z_1 is inductive. The reactance Z_2 is always inductive.

The reactances Z_1 and Z_2 are influenced by parasitic capacitance and inductance at the mixer RF inputs. If R and C are the effective parallel resistance and capacitance respectively, measured differentially across the mixer RF inputs with the parasitics included, then

$$Z_m = R_m - jX_m = R \text{ parallel } -j/\omega C, \text{ where } \omega \text{ is the angular frequency.} \quad (4.4)$$

This gives

$$R_m = R/(1 + \omega^2 R^2 C^2) \quad \text{and} \quad X_m = \omega R^2 C/(1 + \omega^2 R^2 C^2) \quad (4.5)$$

The capacitance of Z_1 is given as

$$C_1 = (1 + \omega^2 R^2 C^2)/[\omega(R - \omega R^2 C)] \quad (4.6)$$

The inductance of Z_2 is given as

$$R(1 + \omega RC)/[\omega(1 + \omega^2 R^2 C^2)] \quad (4.7)$$

For the case when Z_1 is inductive, its inductance is given by

$$L_1 = R(\omega RC - 1)/[\omega(1 + \omega^2 R^2 C^2)] \quad (4.8)$$

In order to balance the mixer RF inputs to ground, the reactances C_1 (or L_1) and L_2 must be split into two equal components as shown in Fig. 4.2.

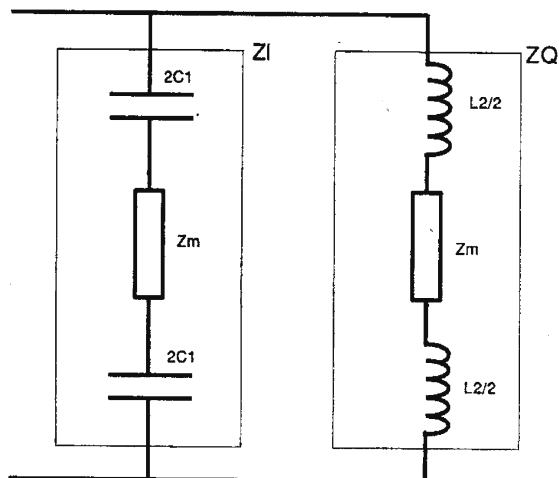


Figure 4.2 Balanced Phase Shift Circuit

Figure 4.3 shows the simulated value of R_m for various parasitic capacitances that are in parallel to the mixer differential inputs of the I and the Q channel. R_m is also the total impedance of the phase shifter, and has to be power matched to the LNA output.

Figures 4.4a and 4.4b show the simulated capacitance C_1 , while Fig. 4.5 shows the simulated inductance L_2 , for the same parasitic capacitances.

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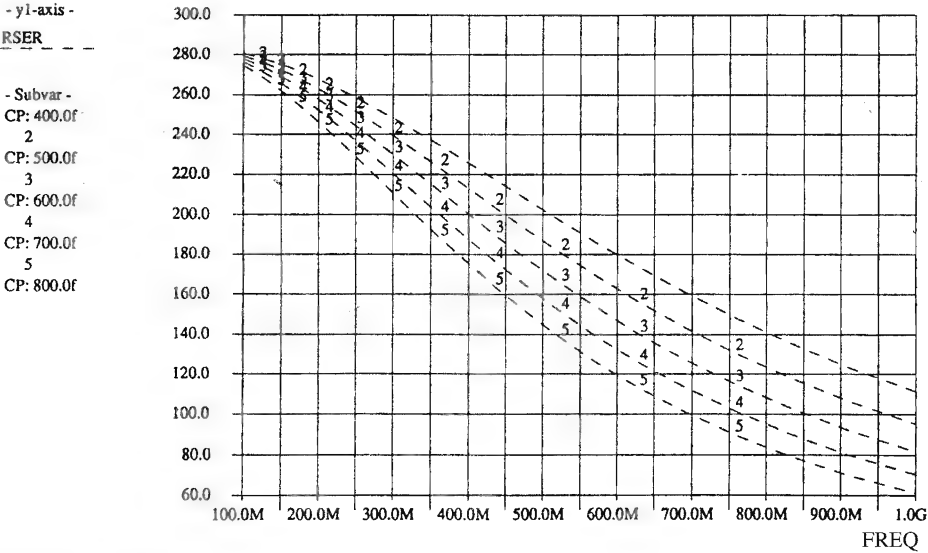


Figure 4.3 Simulation for R_m

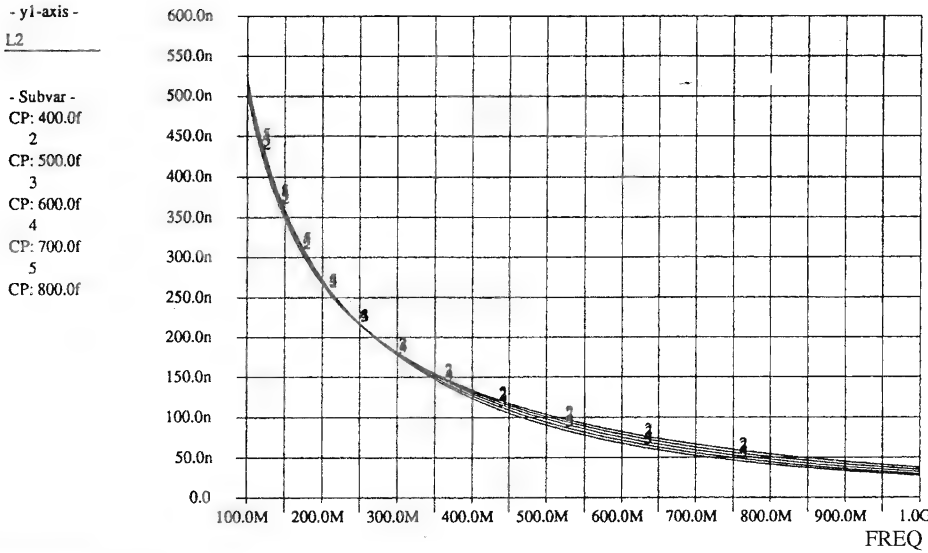
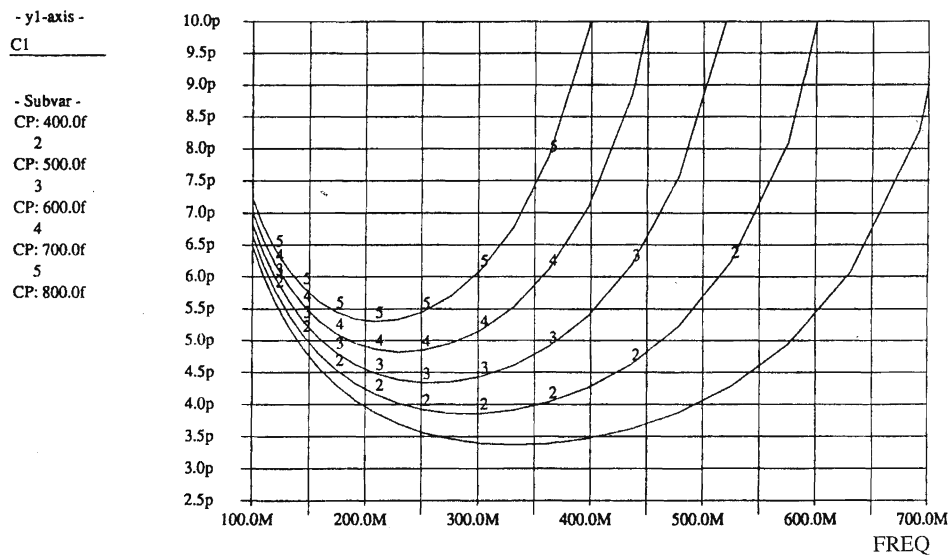
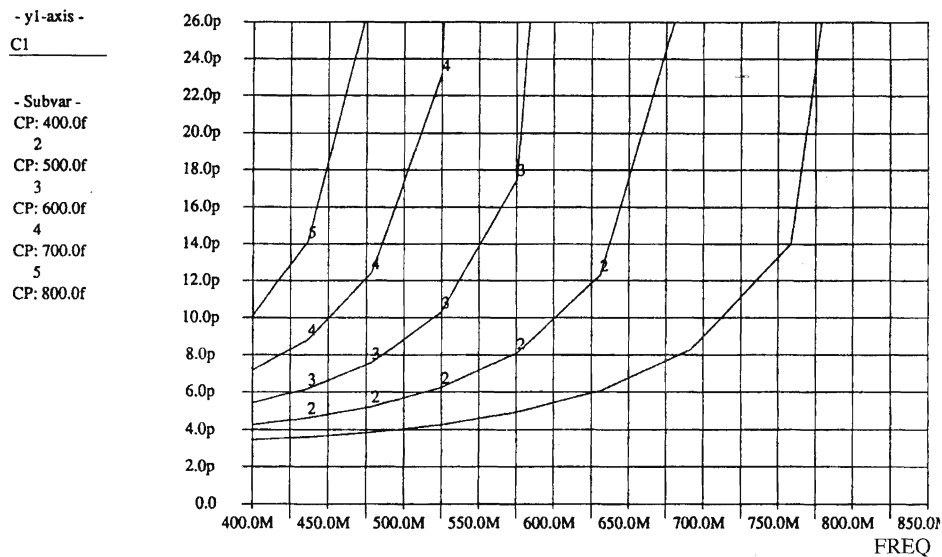


Figure 4.5 Simulation for L_2

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Figure 4.4a Simulation for C₁Figure 4.4b Simulation for C₁

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4.2 EXAMPLES

1) RECEIVER FREQUENCY OF 469.95 MHz

For a parasitic capacitance between 400 fF and 800 fF, C_1 varies from 3.7 pF to 22 pF, as shown in Figures 4.4a and 4.4b. L_2 varies between 100 nH and 125 nH, as shown in Fig. 4.5. By trial, $2C_1$ of 22 pF and $L_2/2$ of 40 nH (nominal) were the closest in the range of components that gave the best result. From the graph in Fig. 4.4b, 11 pF for C_1 implies a board capacitance of about 600 fF, which was also the measured value. The measured value of $L_2/2$ component was little larger than 40 nH at 470 MHz, and with an additional total inductance of about 20 nH due to board wiring, the effective value of L_2 was close to the simulated result.

2) RECEIVER FREQUENCY OF 288.234 MHz

The simulated values are 4.5 pF to 5 pF for C_1 (when the parasitic capacitance is between 600 fF and 700 fF) and about 190 nH for L_2 . The actual components had the values of 10 pF for $2C_1$, and 68 nH series 82 nH for L_2 .

3) RECEIVER FREQUENCY OF 172.941 MHz

The simulated values are 4.75 pF to 5.25 pF for C_1 , (when the parasitic capacitance is between 600 fF and 700 fF) and about 305 nH for L_2 . The components that gave the best results, were 10 pF for $2C_1$ and 150 nH for $L_2/2$.

4.3 CONCLUDING REMARKS

The simulated values of C_1 and L_2 give reasonably good results for the corresponding parasitic capacitance at the mixer input. Better results are obtained if the measured inductance value of L_2 at the receiver frequency, is used, instead of its nominal value at a different test frequency. An inductance of 1 nH per millimeter of board wiring should also be considered for an accurate determination of L_2 . The simulation was done assuming identical parasitic capacitance at the mixer RF inputs, and the effect of board wiring inductance was ignored.

The relative phase and difference in amplitudes between the I and Q audio signals at pins 1 and 2 (TPI and TPQ),

should be measured, keeping their amplitudes less than about 25 mV, to prevent inaccuracies due to differences in the gain compression in the two channels. It is recommended to measure the phase difference at the limiter outputs which have a hard limited waveform, with only the phase information. The limiter output is available at pins 26 and 27 when pin 25 (TS) is pulled to a voltage level higher than 0.9 V (e.g. to Vp).

LOW NOISE FRONT-END RF AMPLIFIER

The UAA2080T has a low noise front-end RF amplifier (called the LNA) to attain high sensitivity. Figure 5.0 shows a typical application circuit at a receiver frequency of about 470 MHz, for an unbalanced 50 Ω signal source. As shown in that figure, the circuit internal to the UAA2080T is an emitter-coupled differential amplifier that has a cascode differential output. The application circuit design for the LNA consists of a) Biasing, b) Input Noise Matching, and c) Output Power Matching. The circuit for the LNA should be optimised to attain the required spurious rejection for the receiver, and this requires a small trade-off with sensitivity.

5.1 BIASING

The biasing of the LNA influences its gain, input impedance, noise figure, IP3, and the DC current. As shown in Fig.5.0, the bases of the transistors T1 and T2 are internally biased by a 1.22 volts DC band-gap reference. The actual DC bias current is determined by the external tail resistor R_E which is in series with an internal 150 Ω resistor.

If the total tail resistance is $R_E = 150 + R_E$, and I is the DC tail current of the LNA, then with reference to Fig. 5.0,

$$R_E = \frac{V_B - V_T \cdot \ln(I/2I_S)}{I} - \frac{R_B}{2\beta} \quad (5.0)$$

I is the small signal DC tail current

β is the current gain, taken as minimum 70

$I_S = 2.7973 \times 10^{-14}$ mA, the reverse saturation current

$R_B = 9.6$ k Ω

$V_B = 1.22$ V

$V_T = 0.026$ mV

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The above equation is the same as the one for the biasing of the differential amplifier frequency multiplier which was described in chapter 3 (see equation (3.0)), hence Fig 3.1 of that chapter shows the simulated values of R_E versus I for the LNA too.

Figure 5.1 shows simulated differential input impedance (parallel R and C) of the LNA as a function of frequency, with the external tail resistor R_E as a parameter. Figures 5.3 to 5.5 show the gain and noise figures, while Figures 5.6 to 5.8 show the IP3 (referred to input, in dBm) and the gain. Each of these simulations are for a particular frequency only (around 173, 288 or 470 MHz). In these simulations, the total parallel resistance of inductances L_p and L_N was kept as 2 k Ω , and the load was also a 2 k Ω resistor (matched load). The values of L_N and L_p were chosen to tune out the capacitive reactance of the LNA output.

In Figures 5.3 to 5.5, it can be seen that the minimum noise figure occurs at a particular value of the source resistance, for a given R_E . The variation in the minimum noise figure with biasing (value of R_E), is very small. The minimum noise figure has the lowest value when R_E is 330 Ω . It may also be seen that the minimum noise figure does not correspond with the maximum power gain.

Equation 5.0 gives a value of 330 Ω for R_E when I is 770 μ A. At the frequencies of 173, 288 and 470 MHz, the minimum noise figures are 1.3, 1.5 and 1.8 dB respectively, when biased by an R_E of 330 Ω . The corresponding source resistances at the minimum noise figures, are 1.3, 1.1 and 1.0 k Ω respectively. For these source resistances, the power gains are 20, 19 and 17.7 dB, and the input IP3s are -27, -26.5 and -25.5 dBm respectively.

Conclusion

In pager applications where battery power has to be kept minimal, R_E may be kept at 330 Ω or more. In applications where battery drain is not a major constraint, a lower value of R_E could be used. This would increase the DC current, but would also increase power gain, and reduce the input parallel resistance, thus reducing input losses in the noise matching with a low impedance antenna. Also the input IP3 would improve.

5.2 INPUT NOISE MATCHING

To achieve a minimum system noise figure, the source resistance seen by the LNA should be somewhere between the one that gives the minimum noise figure for the LNA, and the one that gives maximum power gain for the LNA. Since the LNA is the receiver's front-end and has a large power gain, the source resistance that gives the lowest system noise figure, will also be close to the one that gives the lowest LNA noise figure. Denote $F_{LNA}(R_S)$ as the noise figure and $G_{LNA}(R_S)$ as the available power gain of the LNA, both of them being a function of the source resistance R_S as shown in the simulations (Figures 5.3 to 5.8). Let F_{post_LNA} be the equivalent noise figure of the rest of the stages following the LNA, and F_{system} the total noise figure of the cascade of the LNA and the rest of the stages. Then,

$$F_{system} = F_{LNA}(R_S) + \frac{F_{post_LNA} - 1}{G_{LNA}(R_S)} \quad (5.1)$$

The post LNA noise figure, F_{post_LNA} is about 14 dB i.e. about 25, and with the gain G_{LNA} a little greater than this, the second term in the above equation would be about one, with a small variation as G_{LNA} changes with R_S . The first term varies much more with R_S , and thus the optimal R_S that gives lowest F_{system} , is very close to the value that gives the lowest F_{LNA} . Due to the loss in the input matching, R_S is lower than the optimal simulated value.

The circuit in Fig. 5.0 has an unbalanced source in which one of the input terminals is grounded. By having a balanced input as shown in Fig. 5.2, the LNA noise figure could be decreased slightly, with similar improvement in receiver sensitivity. In Figure 5.0, the source resistance R_{in} has been transformed to a larger parallel input resistance R_{T_in} , given by

$$R_{T_in} = R_{in}(1 + Q^2), \text{ with } Q = 1/(2\pi f_{RX} C_{in} R_{in}) \quad (5.2)$$

Capacitance C_{in} is transformed into a parallel input capacitance C_{par_in} , given by

$$C_{par_in} = C_{in} Q^2 / (1 + Q^2) \approx C_{in} \text{ if } Q \text{ is large.} \quad (5.3)$$

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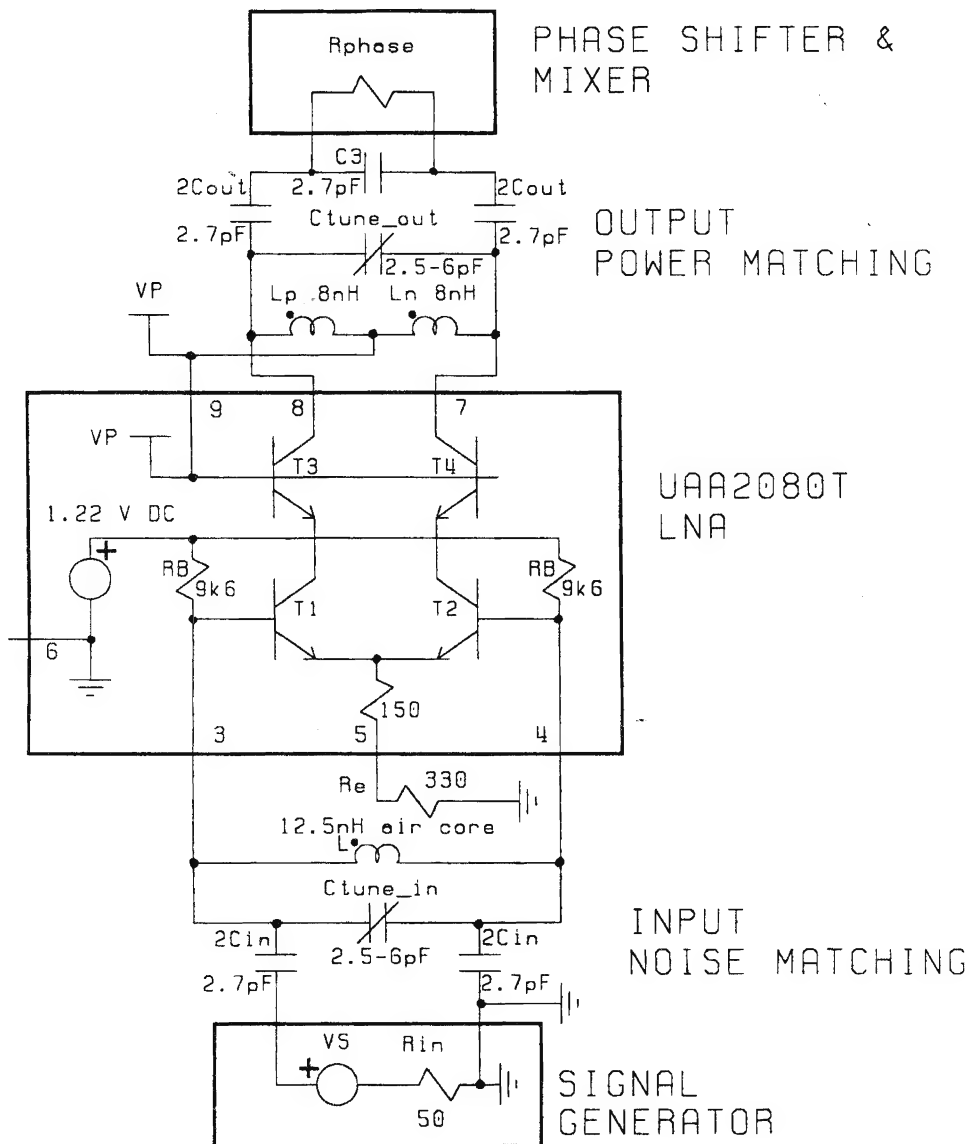


Figure 5.0 470 MHz LNA Application

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The LNA parallel input capacitance, C_{LNA_IN} , board parasitic capacitance, transformed capacitance C_{par_in} , and a small tuning capacitance, C_{tune_in} , all of which add up in parallel, are tuned out by the inductance L . The range of C_{tune_in} should be large enough to compensate the spreads in L and other capacitances. The value of C_{LNA_IN} may be taken as 1.5 pF.

Spurious rejection and Noise Figure

With reference to Fig. 5.0, the noise figure, F of the LNA with the input matching, is given as

$$F = [1 + R_{T_in}/R_p] \cdot F_{LNA}(R_S), \quad \text{where} \quad (5.4)$$

$R_p (= Q_L L \omega)$, Q_L is the quality factor of L is the parallel resistance of L . $R_S (= R_{T_in}$ parallel R_p) is the source resistance as seen by the LNA.

The term in brackets, is due to the insertion loss of R_p .

It may be noted that the input parallel resistance, R_{LNA_IN} of the LNA does not influence F . In order to optimise F ,

R_p needs to be large, which means that both the inductance L and its quality factor, should be large at the receiver frequency f_{RX} . However, the spurious rejection due to this tuned circuit, is proportional to the loaded quality factor, Q_{loaded} .

$$Q_{loaded} = R(C/L)^{1/2} = R/L\omega, \quad \text{where} \quad (5.5)$$

$R (= R_{T_in}$ parallel R_p parallel R_{LNA_IN}) is the total parallel resistance across the LNA inputs.

$C (= C_{par_in} + C_{tune_in} + C_{LNA_IN} + \text{parasitic capacitance})$ is the total capacitance across the LNA inputs.

Therefore, to have large Q_{loaded} and simultaneously small F , R should be large and L small. The use of air core inductance is therefore imperative.

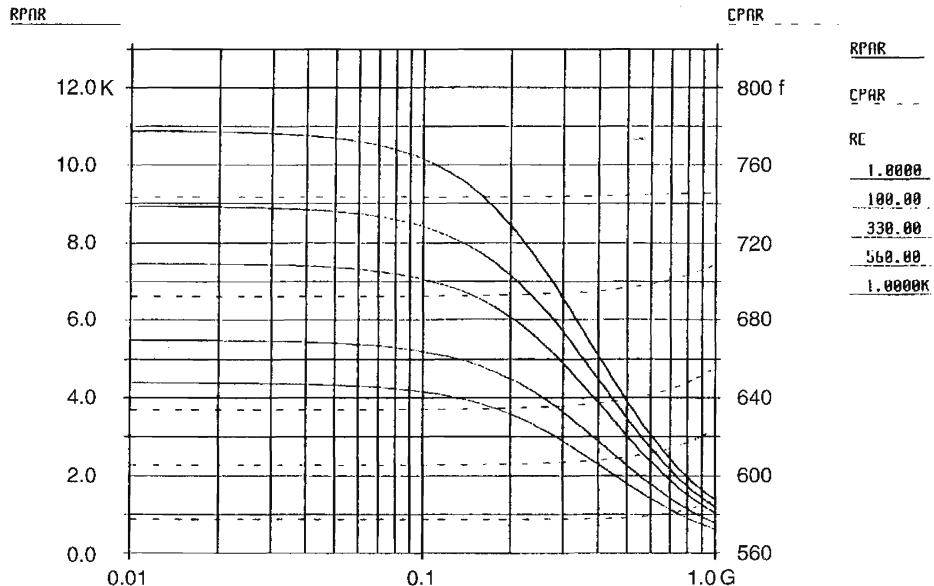


Figure 5.1 LNA Input parallel R and C (X-axis is frequency)

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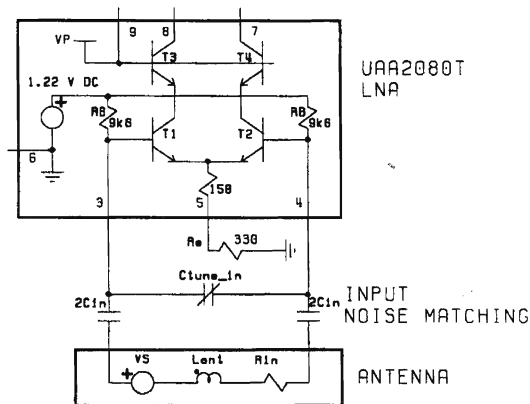


Figure 5.2 Antenna Matching

Antenna Noise Figure

A typical noise matching with a loop antenna is shown in Fig. 5.2. If F_{ant} is the antenna noise figure, then the total system noise figure, F_{system} , becomes

$$F_{\text{system}} = F_{\text{ant}} - 1 + \left[1 + R_{T_{\text{in}}} / R_p \right] \cdot F_{\text{LNA}} (R_{p \text{ parallel}} R_T) + \frac{F_{\text{post-LNA}} - 1}{G_{\text{LNA}} (R_S)} \quad (5.6)$$

Note that the source resistance, R_{in} , of the antenna, is the sum of its radiation resistance (R_R), and its loss resistance (R_L). The source resistance, R_{in} , is transformed to $R_{T_{in}}$ by the matching circuit. The antenna noise figure is given by

$$F_{ant} = F_B + R_l/R_B \text{ where} \quad (5.7)$$

F_R is the equivalent noise factor of the received noise field

For a loop antenna, R_p (ohms) = $320\pi^2 A^2 N^2 / \lambda^4$ (5.8)

A is the loop area, and λ is the wavelength. N is the number of turns in the loop.

At frequencies below 50 MHz, the noise figure of the received field, F_R is large, and there is not much

improvement in F_{ant} by keeping the antenna loss resistance R_L small. At higher frequencies however, F_R is small, and thus it is very important to keep R_L small. This can be achieved by reducing the resistivity of the antenna surface. Since the loop antenna resistance (given by $R_{\text{in}} = R_R + R_L$) is small, there would be considerable loss in the transformation network when transforming to the large optimal source resistance of the LNA, for a noise match. To keep system noise figure low, F as given in equation (5.4), has to be minimised. This would usually mean a $R_{T,\text{in}}$ which is smaller than the value obtained from simulations.

If E is the incident electric field (in volt/meter), then the voltage developed by the loop antenna is

$$V = h_{eff} E, \text{ where} \quad (5.11)$$

h_{eff} [meter] = $2\pi AN/\lambda$, is the effective height of the loop antenna, (5.12)
with A in [meter²] and λ in [meter].

Antenna Noise Matching

For maximum receiver sensitivity, the value of $R_{T,in}$ should be close to the simulated value of the optimal source resistance. The proper way to transform the antenna source resistance, is shown in Fig 5.2, with the necessary equations described below.

With 'D' the loop diameter, d the diameter of the wire, both in centimeters, and N the number of turns, the loop antenna's inductance, L_{ant} , is given as

$$L_{ant} (\mu H) = 2\pi 10^{-3} DN^2 [\ln(8D/d) - 2] \quad (5.9)$$

This inductance along with the two series capacitances ($2C_{in}$ connected at each end of the loop antenna), have a resultant reactance, X , given by

$$X = L_{ant} \omega - 1/(C_{in} \omega) \quad (5.10a)$$

This resultant reactance X is in series with R_{in} . The series combination of R_{in} and X is equivalent to a parallel combination of $R_{T_{in}}$ and $X_{T_{in}}$. The transformed resistance and reactance are

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$$R_{T_in} = R_{in}(1+Q^2), \quad X_{T_in} = X(1+Q^2), \quad \text{with } Q = X/R_{in} \quad (5.10b)$$

If Q is large, then $X_{T_in} \approx X$

Inductive Transformation

Usually it is preferred to keep the reactance X positive (i.e. inductive). Then X_{T_in} is the reactance of a parallel inductance (across pins 3 and 4 of the UAA2080T), and can therefore be tuned out by a tuning capacitor C_{tune_in} whose value is given by

$$C_{tune_in} = X_{T_in}/\omega \quad (5.10c)$$

The circuit in Fig 5.2 uses inductive transformation.

Capacitive Transformation

On the other hand, if X is taken negative (capacitive), then X_{T_in} represents the reactance of a capacitance, C_{par_in} (across pins 3 and 4 of the UAA2080T), given by

$$C_{par_in} = [\omega X_{T_in}]^{-1} \quad (5.10d)$$

This requires a tunable inductor across pins 3 and 4, for tuning. Instead, a fixed inductor, L_{par_in} , can be used along with a parallel tuning capacitor C_{tune_in} (which is taken as a fraction a of C_{par_in}), across pins 3 and 4. They are given by

$$L_{par_in} = [(1+a)C_{par_in}\omega^2]^{-1} \quad \text{and} \quad C_{tune_in} = aC_{par_in} \quad (5.10e)$$

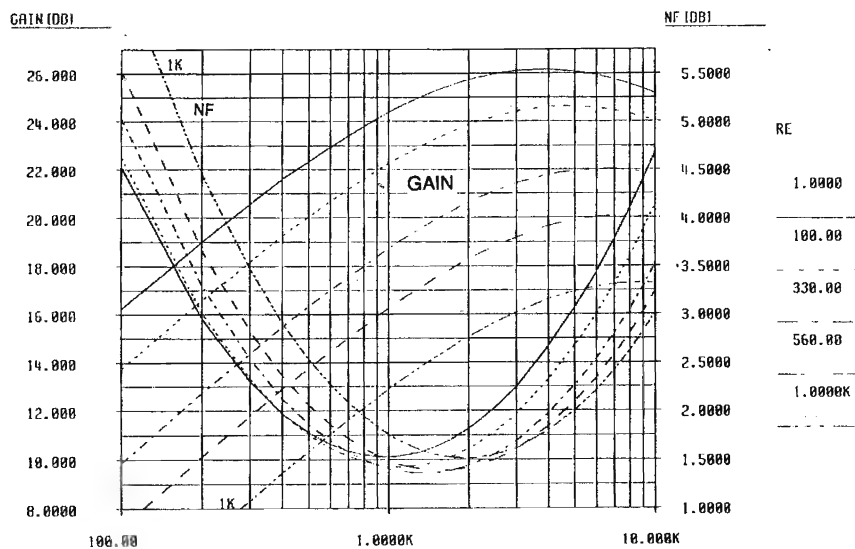
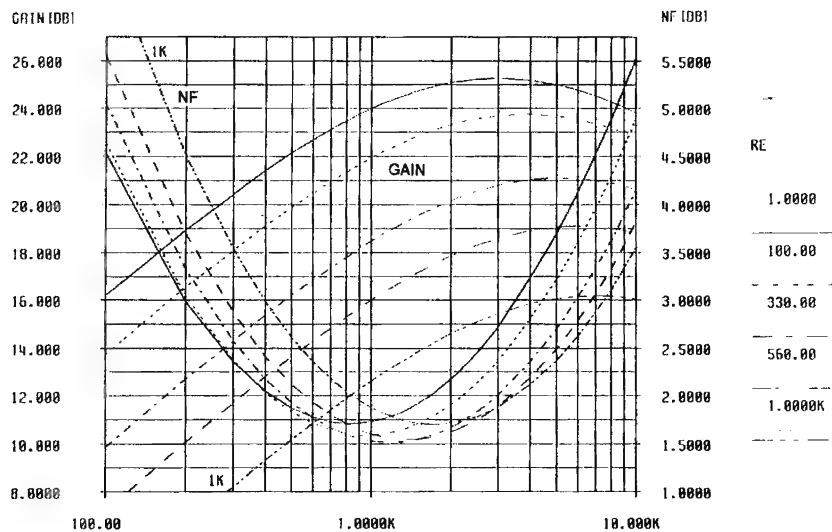
Taking negative X is not desirable as it requires an additional inductance at the input matching. The finite Q of this inductance increases the input noise figure.

Reducing antenna Inductance

The loop antenna gain and radiation resistance R_R increase with the square of N (number of turns in the loop), but unfortunately, so does L_{ant} . A very large L_{ant} could require a very small and impractical value of $2C_{in}$. To avoid using very small capacitances, many larger capacitors can be put in series to give an effectively small value of the required C_{in} . Instead of lumping the series capacitors at the two ends of the antenna, it is better to distribute them between the turns (i.e. break connection between adjacent loops and insert the capacitors in series).

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Figure 5.3 Noise Figure and Gain at 173 MHz (X-axis is R_s)Figure 5.4 Noise Figure and Gain at 280 MHz (X-axis is R_s)

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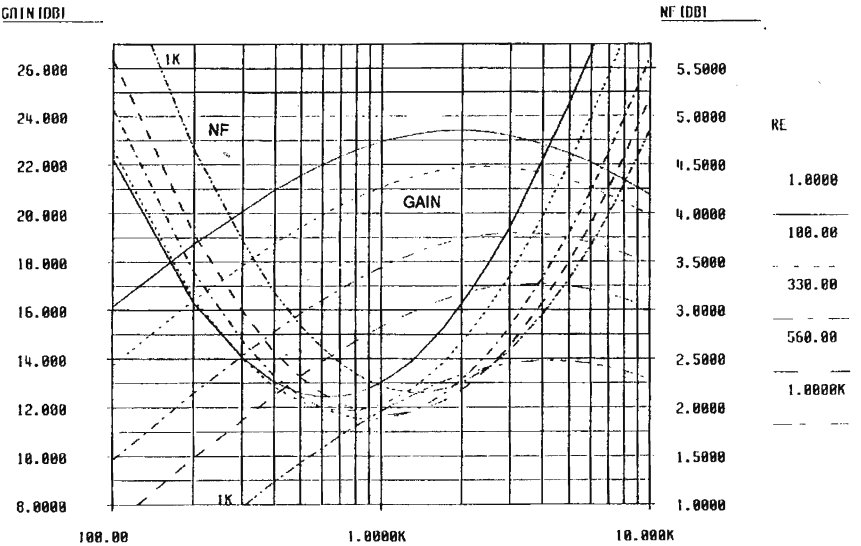


Figure 5.5 Noise Figure and Gain at 470 MHz (X-axis is R_s)

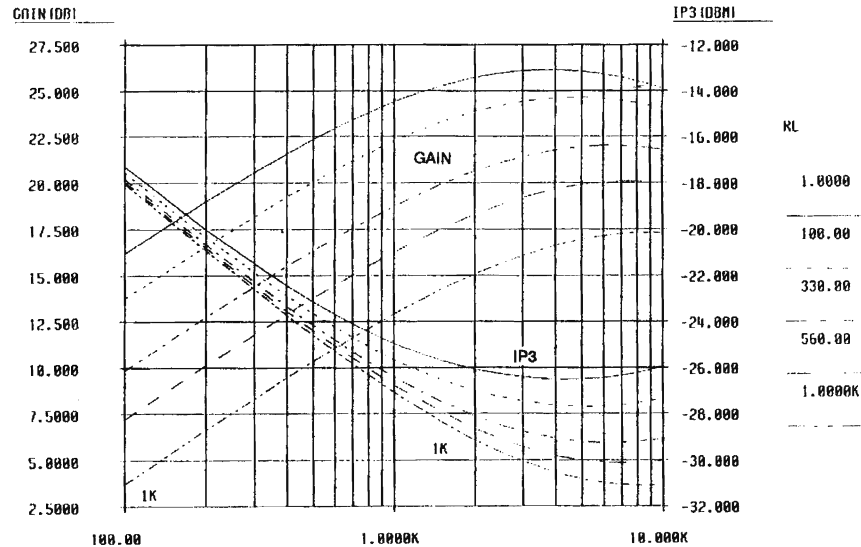


Figure 5.6 IP3 and Gain at 173 MHz (X-axis is R_s)

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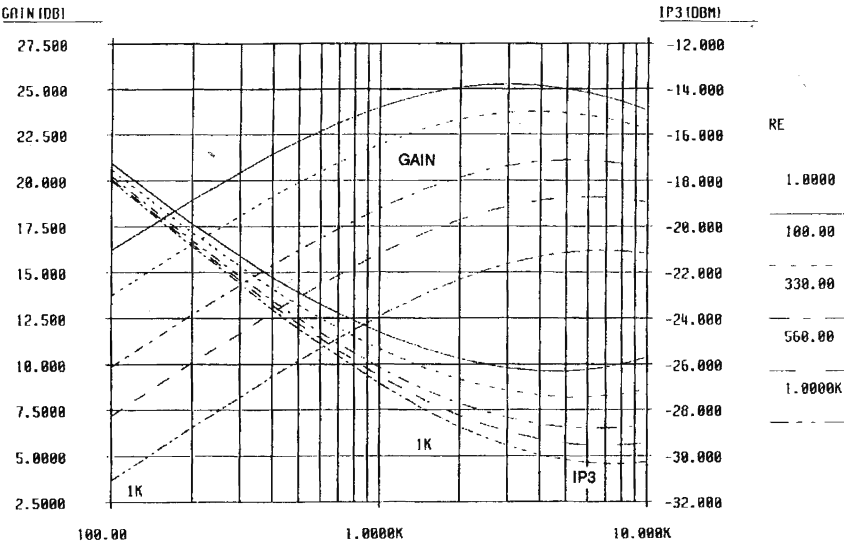


Figure 5.7 IP3 and Gain at 280 MHz (X-axis is R_S)

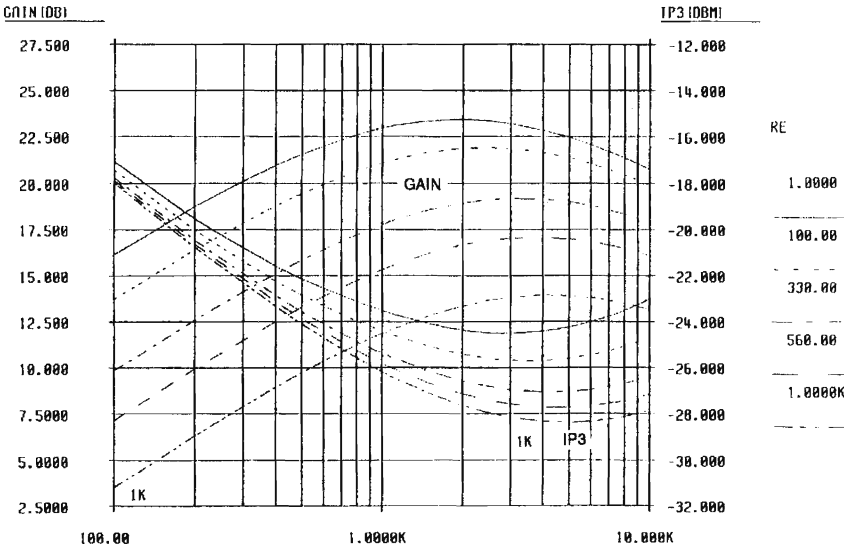


Figure 5.8 IP3 and Gain at 470 MHz (X-axis is R_S)

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5.3 OUTPUT POWER MATCHING

The LNA output is a cascode stage that has a high output impedance, and may be considered as a differential current source. To maximise the power gain of the LNA, the load resistance should be made as large as possible. This means that the resistive load, R_{phase} , of the phase shift network, has to be transformed to a large resistance by the output matching. The maximum value of the transformed resistance is limited by losses in the matching and tuning networks, and losses due to the board (dielectric and copper losses).

Figure 5.9 shows the output circuit. Capacitances C_{out} and C_3 transform the phase shift resistive load, R_{phase} , to a large value R_{load} . For power matching, R_{load} must be equal to $2R_p$, where R_p is the parallel resistance of inductances L_p or L_N . These inductances along with the tuning capacitor $C_{\text{tune_out}}$ tune out the reactance at the LNA output. The transformation formula is given as

$$R_{\text{load}} = \frac{1 + \omega^2 R_{\text{phase}}^2 (C_{\text{out}} + C_3)^2}{\omega^2 R_{\text{phase}} C_{\text{out}}^2} \quad (5.13a)$$

If $C_3 = NC_{\text{out}}$ then

$$R_{\text{load}} = R_{\text{phase}} (1+N)^2 + X_{C_{\text{out}}}^2 / R_{\text{phase}} \quad \text{with} \quad (5.13b)$$

$$X_{C_{\text{out}}} = 1/\omega C_{\text{out}} \quad (\text{the reactance of } C_{\text{out}})$$

The equivalent parallel capacitance, $C_{\text{par_out}}$ of the transformation network, is given as

$$C_{\text{par_out}} = \frac{C_{\text{out}} + \omega^2 R_{\text{phase}}^2 C_3 C_{\text{out}} (C_3 + C_{\text{out}})}{1 + \omega^2 R_{\text{phase}}^2 (C_3 + C_{\text{out}})^2} \quad (5.13c)$$

It may be taken as C_{out} approximately, when the transformation ratio is large, with $C_3 \geq C_{\text{out}}$.

The parallel combination of C_3 and R_{phase} is equivalent to a series combination of a smaller resistance R_{series} and a capacitance (transformed capacitance of C_3). This series resistance is then again transformed to a very large parallel resistance R_{load} , by the capacitance C_{out} in series with the transformed capacitance of C_3 . Larger the value of C_3 , the smaller R_{series} is, and also the greater R_{load} , but

so are the losses due to the ESR (equivalent series resistance) of C_3 and C_{out} . To minimise ESR losses, the ratio of R_{series} to the total ESR should be maximised. Assuming that the quality factors of C_{out} and C_3 are large and equal, and do not change as their capacitances are varied, the ratio of R_{series} to the total ESR of C_{out} and C_3 is maximised when the capacitive reactance of C_3 equals R_{phase} i.e.

$$X_{C_3} = R_{\text{phase}}$$

Under this condition, the transformed resistance is

$$R_{\text{load}} = R_{\text{phase}} [(1+N)^2 + N^2] \quad (5.14a)$$

and the ratio, A , of R_{series} to the loss resistance (total ESR) is,

$$A = Q' / [2(N+1)], \quad \text{with } Q' \text{ the quality factor of } C_{\text{out}} \text{ or } C_3 \quad (5.14b)$$

When the above condition holds, the insertion loss, IL_{out} , of the transformation network is minimum, and is given by

$$IL_{\text{out}} = 1 - 1/A \quad (5.14c)$$

If the capacitance C_3 is not used in the circuit, then the transformation is given as

$$R_{\text{load}} = R_{\text{phase}} (1 + Q^2), \quad \text{with } Q = 1/(2\pi f_{\text{RX}} C_{\text{out}} R_{\text{phase}}) \quad (5.15a)$$

Capacitance C_{out} is transformed into a parallel capacitance $C_{\text{par_out}}$, given by

$$C_{\text{par_out}} = C_{\text{out}} Q^2 / (1+Q^2) \approx C_{\text{out}} \quad \text{if } Q \text{ is large.} \quad (5.15b)$$

The ratio of R_{phase} to the loss resistance (ESR of C_{out}) is

$$A = Q' R_{\text{phase}} / X_{C_{\text{out}}} \quad (5.15c)$$

To maximise power gain, L_p and L_N should have as large a value possible, along with a large quality factor.

However, if their total parallel resistance $2R_p$ is too large, then other losses become dominant, and the optimal level of R_{load} is smaller than $2R_p$, and increasing R_p much further (by using larger inductance) may not significantly improve the gain. It usually turns out that the largest

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value for L_p and L_N is limited by the minimum practical capacitance value of $C_{\text{tune_out}}$, which should at least be of the tuning range of 2.5-6 pF.

Spurious Rejection

The spurious rejection of the receiver can be substantially improved by increasing the loaded Q of the tuned circuit at the LNA output. This can best be achieved by lowering the inductance of L_p and L_N . The LNA gain reduces because the parallel resistance of the inductance also becomes smaller. However, the loss in receiver sensitivity is only marginal because the LNA gain is still quite large. Thus, air core inductances are not needed for L_p and L_N , and they may be used only if the sensitivity has to be really maximised (the improvement would be marginal, say within 1 dB). It is important to keep $2R_p$ much smaller than the parallel loss resistance of the board, which could be about 10 k Ω at UHF, and a little higher at VHF. With insertion loss due to the board losses and losses in $C_{\text{tune_out}}$, C_{out} and C_3 , much less than 3 dB, the loaded Q with power matching is a little less than half the Q of the inductances. The value of $2R_p$ should be between 2 and 3 k Ω in order to have maximal gain, while attaining a loaded Q of about half that of the inductances. By reducing $2R_p$ below 2 k Ω , the power gain (with matched load) decreases, while the loaded Q approaches half that of the inductances. This may be done to improve spurious rejection further, at the expense of reduced sensitivity.

5.4 POWER GAIN

The simulated power gain, G_{sim} [dB], corresponding to the transformed source resistance $R_{r,\text{in}}$, is shown in Figs. 5.4 to 5.6, for particular frequencies. Since the simulated LNA gain has been done for a matched load of 2 k Ω , it would differ for other loads. The correction in gain, G_{cor} [dB], due to the matched output load resistance differing from 2 k Ω , is

$$G_{\text{cor}}[\text{dB}] = 10 \cdot \log(R_{\text{load}}/2), \quad (5.16a)$$

with R_{load} in $k\Omega$. This assumes that the value of R_{load} is equal to $2R_{p1}$, and that the equivalent parallel loss resistance due to board and matching losses, is much higher.

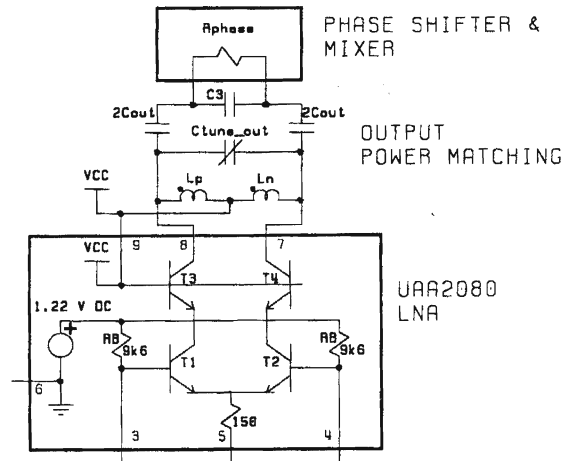


Figure 5.9 Output Power Matching

The insertion loss, IL_{in} , of the input matching circuit is

$$IL_{in} = [1 + (R_{T_{in}} \text{ parallel } R_{LNA_{in}})/R_P]^2, \quad (5.16b)$$

and the insertion loss in dB is $IL_{in}[\text{dB}] = 10.\log(IL_{in})$

R_p is the parallel resistance of the inductance L . However, if the quality factor Q_C of the total parallel input capacitance is not very much larger than the quality factor Q_L of L , then effective parallel resistance R_p is calculated by the following formula.

$$R_p = QL\omega, \text{ with } Q = [1/Q_c + 1/Q_l]^{-1} \quad (5.16c)$$

The total gain, $GAIN_{INA}$, is given as

$$\text{GAIN}_{\text{LNA}}[\text{dB}] = G_{\text{sim}}[\text{dB}] + G_{\text{cor}}[\text{dB}] - \text{IL}_{\text{in}}[\text{dB}] - \text{IL}_{\text{out}}[\text{dB}] \quad (5.16\text{d})$$

5.5 INPUT THIRD ORDER INTERCEPT POINT

The input IP3 of the receiver is dependent largely on the input IP3 of the LNA. The IP3 at the input terminals of an emitter coupled differential amplifier is 100 mV peak. For frequencies close to the received frequency, the system input IP3 is given by the following equation.

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$$IP3_{\text{system}} = IP3_{\text{LNA}} - 10 \cdot \log[1 + 10(IP3_{\text{LNA}} + GAIN_{\text{LNA}} - IP3_{\text{PHASE}})/10] \quad (5.17)$$

All the IP3's are referred to inputs, and are in dBm. $GAIN_{\text{LNA}}$ and IL_{in} are in dB.

$IP3_{\text{PHASE}}$ is the IP3 of the phase shifter the mixer taken together. The simulated values for the mixer IP3 are given in table 6.0 (chapter 6). $IP3_{\text{PHASE}}$ is approximately 3dB more than that of the mixers.

The $IP3_{\text{LNA}}$ improves over the simulated value due to the insertion loss at the input. But this occurs at the expense of increased noise figure.

$$IP3_{\text{LNA}} = IP3_{\text{LNA}}(\text{simulated}) + IL_{\text{input}}[\text{dB}] \quad (5.18a)$$

The intermodulation rejection of the receiver, IM3 is given by

$$IM3[\text{dB}] = 2[IP3_{\text{system}} - A - 3 - CCR/2]/3 \quad (5.18b)$$

'A' is the receiver sensitivity (at say 3% bit error rate) in dBm. CCR is the co-channel rejection in dB, when the signal power level is A+3 dBm.

5.6 EXAMPLES

In the following examples, the LNA has been biased by a 330 Ω external tail resistor.

1) RECEIVER FREQUENCY OF 469.95 MHz

Input Noise Matching for 50 Ω unbalanced source

For a balanced input, the simulation in Fig. 5.6 shows an optimal source resistance of 1 k Ω , at which the noise figure is 1.8 dB. C_{in} of 1.35 pF (2.7 pF/2) transforms a 50 Ω source into $R_{\text{T,in}}$ of 1.3 k Ω . The 12.5 nH L is an air core type with a Q of about 145 at 470 MHz. With a Q of about 200 for the parallel capacitance, the Q of the tank alone is about 84. Its parallel resistance R_p is thus about 3.1 k Ω , bringing the value of R_s to about 916 Ω (1.3 K parallel 3.1 K), which is the source resistance seen by the LNA. The degradation in noise figure is a factor $1 + R_{\text{T,in}}/R_p = 1.42$, which is about 1.5 dB, thus making the

LNA noise figure 3.3 dB, for a balanced input, and a little worse for the unbalanced case.

The parallel input resistance of the LNA is about 3.2 k Ω , so the insertion loss of the noise matching circuit is 2.3 dB, using equation (5.16b). This increases the input IP3 of the LNA by 2.3 dB.

The inductance L of 12.5 nH, requires a capacitance $1/L\omega^2$ i.e. about 9 pF for parallel resonance. With 1.35 pF C_{in} , 1.5 pF $C_{\text{LNA,IN}}$, and 1.5 pF board capacitance, a remaining 4.5 pF is required for tuning. Due to board wiring, the effective value of L increases by about 1 nH per cm of PCB track, so $C_{\text{tune,in}}$ would be less than 4.5 pF. A value of 2.5-6 pF tuning range was found appropriate.

The loaded Q at the input is $(R_s \text{ parallel } R_{\text{LNA,IN}})/\omega L$. From Fig. 5.3, $R_{\text{LNA,IN}}$ is 3.5 k Ω , so the loaded Q is $725/37 = 20$.

Output Power Matching

R_{phase} is about 190 Ω , from the simulations in Fig. 4.3 of the previous chapter. In practice, R_{phase} will be less than the simulated value due to losses in the phase shift components. With the choice of 2.7 pF for C_3 and $2C_{\text{out}}$, X_{C2} is a little less than R_{phase} , and $N = 2$. The transformed load, R_{load} , is about $13R_{\text{phase}} \approx 2.5\text{k}\Omega$, using equation (5.14a). Inductances of 8 nH for L_p and L_N , with a Q greater than 50 at 470 MHz, provide a total parallel resistance close to 2.5 k Ω for power matching.

The 16 nH total inductance requires a capacitance of $1/L\omega^2 \approx 7.2$ pF. The transformed parallel capacitance is a little less than 2.7/2 pF i.e. less than 1.3 pF. With the LNA parallel output capacitance along with board parasitics taken as 2 pF, the tuning capacitance required is $7.2 - (1.3 + 2) = 3.9$ pF. The range of 2.5-6pF was found suitable for $C_{\text{tune,out}}$.

The loaded Q of the output is a little less than half the Q of L_p or L_N , due to losses in the board and impedance transformation.

From Fig. 5.6, the simulated gain is 17.7 dB. The correction due to the load differing from 2 k Ω is 0.97 dB. The input insertion loss is 2.3 dB. The total power gain is about 16.4 dB, without considering losses at the output.

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The system IP3 is about -28.3 dBm, using equation (5.17). The receiver sensitivity was measured around -125.5 dBm (for 80% call success rate) with the PCF5001T decoder, and the CCR measured about 6 dB. The intermodulation rejection, IM3 measured about 60 dB, and its value computed from equation (5.18b) is 60.8 dB.

2) RECEIVER FREQUENCY OF 288.234 MHz

Input Noise Matching for 50 Ω unbalanced source

Optimal sensitivity was achieved with a value of 4.7 pF for $2C_{in}$, for an unbalanced 50 Ω source. The transformed resistance is 1.15 k Ω , and the optimal simulated source resistance is around 1.1 k Ω . In order to use a tuning capacitor in the range of 2.5-6 pF, the value of L was 35.5 nH. For an air core type with a Q of around 120, a 22 nH inductance improved spurious rejection by 4 dB (at the expense of 0.4 dB loss in sensitivity) when compared with the air core inductance of 35.5 nH. For the 22 nH inductance, a 13.9 pF is required for resonance. A 5-20 pF tuning capacitor was found suitable.

Output Power Matching

For maximum power gain, the largest inductance for L_N and L_p was 27 nH each. The total of 54 nH was tuned by a 2.5-6 pF tuning capacitor, along with the additional parallel capacitance (about 2 pF for LNA output and board capacitance, and 1 pF transformed capacitance). Maximum gain was attained when C_3 and $2C_{out}$ were 2.2 pF.

With 15 nH inductance for L_N and L_p , the spurious rejection improved by about 3 dB, and the sensitivity reduced by about 0.3 dB. A 3-10 pF tuning capacitor was appropriate for this choice of inductance.

3) RECEIVER FREQUENCY OF 172.941 MHz

Input Noise Matching for 50 Ω unbalanced source

The optimal source resistance is between 1 k Ω and 1.3 k Ω for a noise match, as shown in the simulations. C_{in} of 4.1 pF transforms the 50 Ω source resistance to 1.05 k Ω . This value of C_{in} (choice of $2C_{in}$ fell among

practical values of 5.6, 6.8, 8.2 and 10 pF) gave the best receiver sensitivity when L was taken as 82 nH, with a Q of 65 at 173 MHz.

This value of 82 nH was the largest that could be tuned out by a 2.5-6 pF C_{tune_in} in the circuit. 82 nH is tuned out by 10.3 pF. With about 4 pF for C_{in} , and 3 pF for board and LNA input capacitance, a remaining of about 3.3 pF is provided by C_{tune_in} .

An air core coil of 43 nH, with a Q of 115 at 173 MHz, improved the spurious rejection by about 2.3 dB, while the sensitivity reduced by about 0.2 dB. The tuning capacitor was 5-20 pF, and had a Q that was less than the 2.5-6 pF capacitor. Also, when $2C_{in}$ of 6.8 or 10 pF were used, the sensitivity reduced by about 0.3 dB.

Output Power Matching

R_{phase} is about 270 Ω from the simulations. A value of 3.9 pF for C_3 and $2C_{out}$ gave an optimal transformation, when L_p and L_N 68 nH, with a Q of 65, were used. The tuning capacitance required was 2.5-6 pF.

The spurious rejection improved by about 4 dB (at the expense of 0.5 dB reduction in sensitivity) when L_p and L_N were taken as 22 nH each (with Q of about 70). The value of 8.2 pF for C_3 and $2C_{out}$ gave optimal gain.

MIXER & POST MIXER STAGES

One of the outstanding features of the UAA2080 single-chip paging receiver is that the mixer and post mixer stages (i.e. IF filters, limiters and demodulator) are fully integrated, obviating the need for any external components or application circuits. Only a single resistor is required to set the upper cut-off frequency of the IF filter. This chapter therefore serves only to describe these sections in more detail, without going into any application circuit design.

6.1 MIXER

The mixer in each of the I and the Q channels, is a double-balanced Gilbert Multiplier, as shown in Fig. 6.0. The emitters of the lower stage (grounded base) transistors comprise the differential RF input. Because of the common-base configuration of the RF input, the IP3

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of the mixer is rather large. The Table 6.0 below gives the simulated noise figure, IP3 and power gain of the mixer (when it is fully switched). The output differential impedance of the mixer is 6.4 kΩ, while the loading of the following IF filter is negligible. The conversion gain of the mixer is dependent on the LO drive level, as shown in Fig. 3.3. The phase-shifter in front of the mixer's RF inputs, have a 3 dB attenuation. The combined mixer and phase shifter characteristics therefore differ by about 3 dB from the values in Table 6.0.

Frequency [MHz]	IP3 [dBm]	Noise Figure [dB]	Gain [dB]
173	-13.4	4.2	2.8
288	-13.2	4.4	2.7
470	-13.3	4.8	2.4

Table 6.0 Simulated Mixer Characteristics

The bases of the upper stage switching transistors must be biased at a DC voltage that would provide equal collector-emitter voltage for the upper and lower stages of the mixer, at the lowest supply voltage. This has been covered in Chapter 3, on the frequency multiplier.

6.2 IF FILTER

The collector load of the the mixer upper stage switching transistors, is a low pass RC filter that removes the RF signal. The differential output signal (in the audio band) of the mixer is amplified by a low noise audio amplifier to ensure that the noise of the following stages do not affect the overall noise figure. It is followed by an active low pass filter that reduces the levels of strong signals in the adjacent channel. This filter has a notch at 15 kHz. For channel spacing of 20 kHz or more, receiver's adjacent channel performance is actually

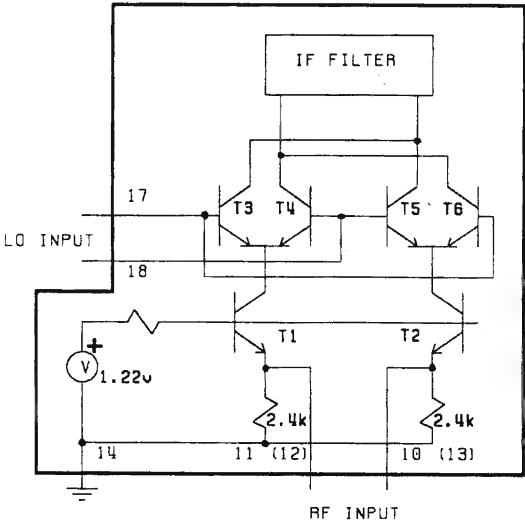


Figure 6.0 UAA2080T Mixer (shown with pin numbers)

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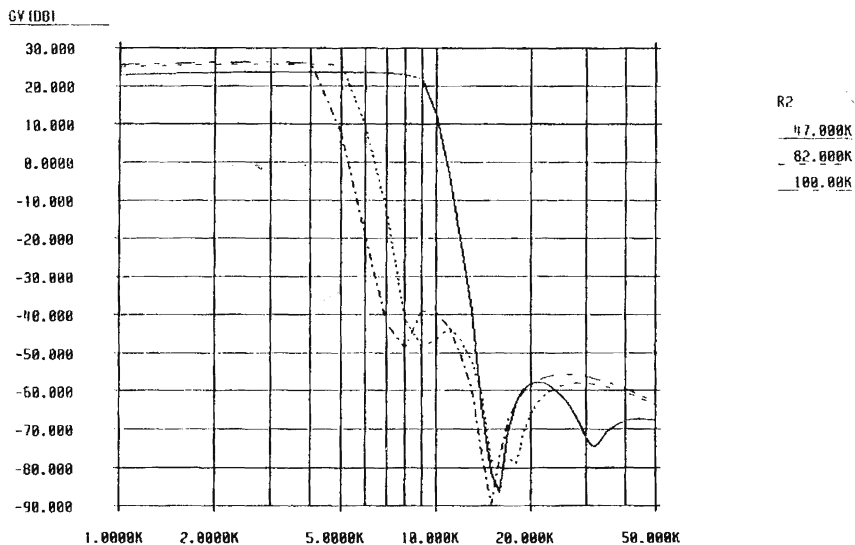


Figure 6.1 IF Filter Transfer Function (X-axis is frequency)

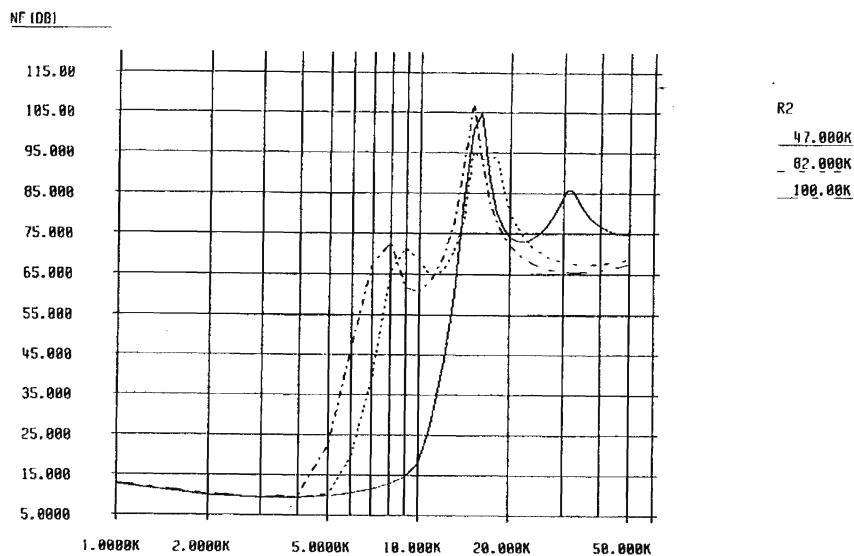


Figure 6.2 IF Filter Noise Figure (X-axis is frequency)

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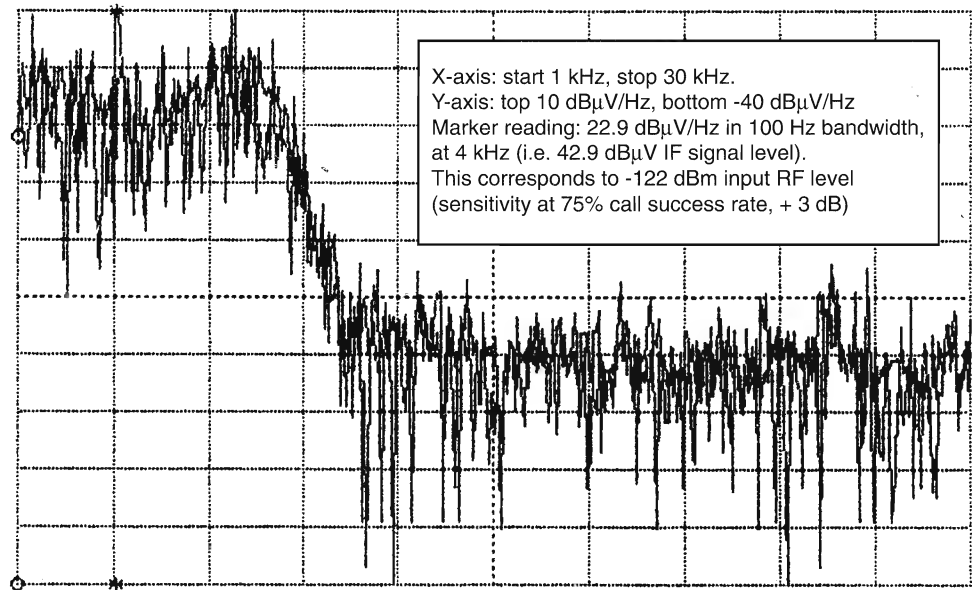


Figure 6.3 Measured Noise Floor at TPI and TPQ, for 470 MHz application determined by the onset of blocking and non linear effects in this high pass filter which precedes a gyrator filter. AC coupling between the active filter and the gyrator filter keeps DC-offsets away from the gyrator filter.

The programmable gyrator low pass filter serves to limit the noise bandwidth of the receiver, and thus to optimise receiver sensitivity. It implements the transfer function of a 7th order elliptic filter, with the upper (3 dB) cutoff frequency controlled by an off-chip resistor across pins 15 and 16 of the UAA2080. Note that this single gyrator resistor, R2, controls the upper cutoff frequency for both the channels. The gyrator filter outputs are available through buffer amplifiers, at pins TPI and TPQ. The upper cutoff frequency of the gyrator filter varies linearly with the off-chip resistance, R2, as shown in Fig. 6.1. Note that the transfer function in Fig. 6.1 is for the entire IF filter. The larger the resistance R2, the smaller is the upper cutoff frequency. The notch at 15 kHz is independent of R2, as it is determined only by the active filter. There is negligible variation in the IF filter transfer function, in the temperature range -10 °C to +55 °C and supply range 2.05 V to 3.5 V. Table 6.1 shows some measurements of the 3 dB upper cutoff frequency. It is

not advisable to use R2 less than 39 k Ω , because the pass band gain of the filter decreases, and the relative 3 dB roll-off point remains nearly constant at 10 kHz.

R2 k Ω	f (-3dB) kHz
120	3.25
100	4.0
82	5.25
68	6.25
56	7.5
47	9.0
39	10.0

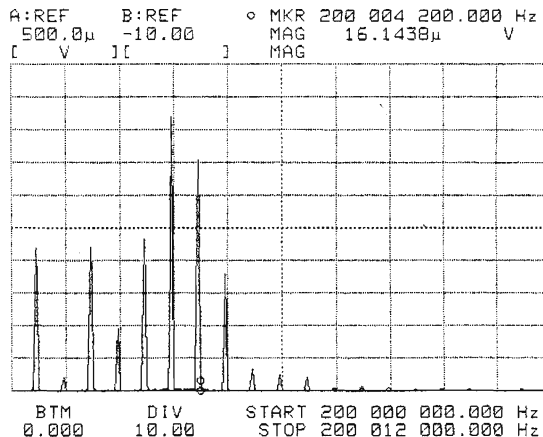
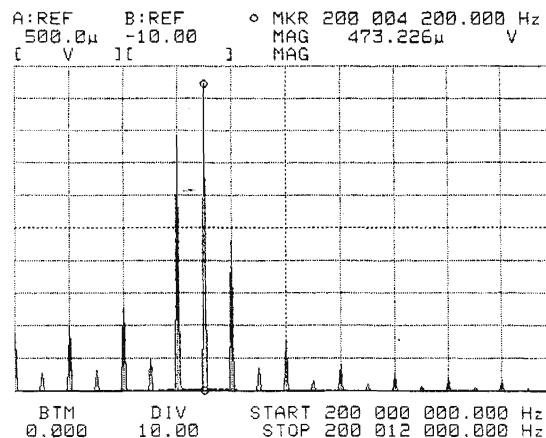
Table 6.1

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S/N Ratio

The measured noise floor at the IF output (pins 1 and 2) is shown in Fig. 6.3 for a 470 MHz receiver, when R2 is 47 k Ω . The passband noise level is about 20 dB more than in the stopband, therefore the noise bandwidth of the receiver is solely determined by the IF passband. Knowledge of the noise bandwidth allows an approximate calculation of the receiver sensitivity. For example, the upper cutoff is about 9 kHz when R2 is 47 k Ω . The RF input noise bandwidth is then approximately 18 kHz. The measured sensitivity at 470 MHz was -125.5 dBm (50 Ω source at room temperature) i.e. -12.5 dB μ V (EMF), for 80% CSR (call success rate) using a PCF5001T decoder. At room temperature (300 °K), the input noise floor is -60.82 dB μ V/Hz (50 Ω source), thus producing a -18.3 dB μ V noise source voltage in the 18 kHz passband. The S/N ratio at the RF input is therefore 5.8 dB (18.3-12.5). The measured noise floor at the IF output was 0.3 dB μ V/Hz giving 39.8 dB μ V noise voltage in the 9 kHz band. The IF signal voltage measured 40.8 dB μ V for -125.5 dBm RF input level (thus giving a voltage gain V_{IF}/V_{RF} of 53.3 dB). The S/N ratio at the IF output is therefore 1dB (40.8-39.8), which gives a 4.8 dB (5.8-1) receiver noise figure. The limiter/demodulator combination is driven by the same IF signal that is available at pins 1 and 2. Therefore it may be concluded that the UAA2080T demodulator requires a signal quality of only 1dB S/N ratio at 1200 baud to give a 80% CSR, using the Philips PCF5001T decoder. Since the noise figures of the IF filter (shown in Fig. 6.2), mixer and phase-shifter, and the RF LNA, are known, the input signal level (receiver sensitivity) corresponding to 1 dB S/N ratio at the demodulator, can be calculated.

Figure 6.4 Signal Spectrum (250 μ s rise/fall time)Figure 6.5 Signal Spectrum (50 μ s rise/fall time)

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Signal Spectrum and Filter Cutoff Frequency

The required upper cutoff frequency of the IF filter depends on the frequency drift (due to aging, and temperature changes) of the local oscillator, on the transmitter frequency offsets, and on the power bandwidth of the received signal (determined by frequency deviation and data rate, that are limited by the channel spacing which is 20 or 25 kHz in this application).

Figure 6.4 shows the upper half power spectrum of the transmitted preamble signal (a mirror image of this spectrum lies below the carrier frequency). FM modulation (DC coupled) was used, with peak deviation of 4 kHz and carrier of 200 MHz. The edges of the modulating 1200 baud NRZ preamble data signal had a rise and fall time of 250 μ seconds. For the preamble (alternating 1 and 0 data sequence), the line spectra are at multiples of half the baud rate i.e. at multiples of 600 Hz, on either side of the carrier. If the data edges had zero rise/fall time, then the envelope of the line spectra follows the difference of two $\text{Sin}(x)/x$ curves, one centered at $f_{\text{carrier}} - 4 \text{ kHz}$ and the other at $f_{\text{carrier}} + 4 \text{ kHz}$. The variable 'x' is πfT , with $T = 1/\text{baud}$, and f the relative frequency (from $f_{\text{carrier}} - 4 \text{ kHz}$ or $f_{\text{carrier}} + 4 \text{ kHz}$). Since $\text{Sin}(x)/x$ is maximum at $x = 0$, therefore the line spectra peak at $\pm 4 \text{ kHz}$ from the carrier. Fig. 6.5 shows such a power spectrum (the rise/fall time was 50 μ s instead of zero, due to practical limitations).

With 250 μ second rise/fall time, the power at frequencies outside $[f_{\text{carrier}} - 4 \text{ kHz}, f_{\text{carrier}} + 4 \text{ kHz}]$ is reduced, while the power within this interval is increased. If a sinusoidal signal of frequency f_m , is used to frequency modulate the carrier with a peak deviation of Δf , then the 99% power bandwidth is $2 \cdot (\Delta f + f_m)$. For the ramped waveform of the above mentioned preamble, the power bandwidth is therefore more than $2 \cdot (4 \text{ kHz} + 1200/2)$ i.e. more than 9.2 kHz. This means that the IF cutoff frequency should be more than 4.6 kHz.

The modulation index 'm' of the transmitted signal is defined as the total number of points at intervals of half bit rate (i.e. 600 Hz for 1200 baud), that are present in the power bandwidth. The IF filter upper cutoff should ideally be set to $0.5 \text{ m} \cdot [\text{bit rate}/2]$. However, due to the difference, f_{offset} , between the transmitted carrier frequency and the local oscillator frequency, the upper cutoff

frequency should be increased. The maximum value of f_{offset} is of course limited to Δf , which is the peak frequency deviation. If f_{offset} exceeds Δf , then the demodulator will not be able to decode the data, since the transmitted frequency will not cross the receiver frequency during data transitions (1 to 0 or 0 to 1). Therefore, the upper cutoff frequency should not exceed $0.5 \text{ m} \cdot [\text{bit rate}/2] + \Delta f$ under any circumstance. At a given f_{offset} , the peak IF frequency deviations are $\Delta f - f_{\text{offset}}$ and $\Delta f + f_{\text{offset}}$. For the demodulator to detect a change in data, there must be at least a quarter cycle of the IF signal in the bit period. Equating $\Delta f - f_{\text{offset}} = [\text{bit rate}]/4$, the maximum offset is therefore $f_{\text{offset}} = \Delta f - [\text{bit rate}]/4$ which is 3.7 kHz for 1200 baud and 4 kHz deviations.

Offset performance depends on the data (preamble or PRBS) and the rise/fall time of the data edges. For the 1200 baud preamble with 250 μ s rise/fall time, the upper half power bandwidth extends till 6.85 kHz, as shown in Fig. 6.4. The best sensitivity was attained with R2 of 62 k Ω (i.e. the upper cutoff at about 6.9 kHz) when f_{offset} was zero. With R2 of 47 k Ω (i.e. cutoff at 9 kHz) the offset performance improved for f_{offset} greater than 2.5 kHz. However, for a 50 μ s rise/fall time (spectrum shown in Fig. 6.5), here is no improvement in offset performance when the IF cutoff frequency is more than the optimal cutoff frequency of 6.9 kHz.

Note that increasing the upper cutoff frequency beyond the nominal power bandwidth (to accommodate frequency offset f_{offset}) unfortunately increases the receiver's noise bandwidth, and thus decreases the receiver sensitivity, even though the offset performance may improve. The loss in sensitivity in dB varies as $10 \cdot \text{LOG}(B)$, where B is the factor by which the bandwidth increases beyond its optimal value. The loss in sensitivity with f_{offset} is given in table 6.2, for a 50 μ s rise/fall time. Note that in the absolute scale, the sensitivity with R2 of 47 k Ω , is $10 \cdot \text{LOG}(9/6.9) = 1.1 \text{ dB}$ worse than the optimal value (with R2 = 62 k Ω).

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UAA2080T VHF/UHF paging receiver

Loss in Sensitivity (dB)	Offset (kHz)	
	R2=62k Ω	R2=47k Ω
1	2.4	2.2
2	2.6	2.7
3	2.8	2.9
5	3.1	3.2
10	3.3	3.5

Table 6.2 Sensitivity versus Offset for 50 μ s rise/fall time, 1200 baud and 4 kHz Δf

With 250 μ s rise/fall time, the loss in sensitivity varies as given in table 6.3. In the absolute scale, the sensitivity, with R2 of 47 k Ω , is 0.5 dB worse (and not 1.1 dB as expected!).

Offset (kHz)	Loss in Sensitivity (dB)	
	R2=62k Ω	R2=47k Ω
2.0	0.2	0.2
2.5	2.0	1.5
2.75	4.1	2.9
3.0	9.0	6.0

Table 6.3 Sensitivity versus Offset for 250 μ s rise/fall time, 1200 baud and 4 kHz Δf

6.3 LIMITER

The limiter serves as a zero crossing detector, thus removing amplitude variations in the IF signal, while retaining only the phase information. It has 75 dB gain, an upper 3 dB roll-off at 17 kHz, and a lower 3 dB roll-in of 600 Hz. The limiter threshold level is -70 dB μ V peak-peak. The limiter outputs are available at pins 26 (channel Q) and 27 (channel I), when pin 25 (TS) is

pulled to Vcc. The limiter outputs are ideally suited to measure the I-Q phase difference, since its outputs are square waves with sharp edges.

6.4 DEMODULATOR

The demodulator of the UAA2080 is a phase detector that detects the relative (positive/negative) phase difference between the I and the Q channel signals that emerge from the limiters. Basically, for every edge (positive and negative) in the I channel limiter output, it samples the amplitude in the Q channel limiter output, and vice versa. The sampled amplitudes (polarity corrected) are fed to a schmitt trigger whose output is available at pin 27 (DO) as the data output. Therefore, the data output is updated 4 times per cycle of the IF signal. This also means that the maximum jitter duration in the data output is $1/(4 \cdot \Delta f)$. For 4 kHz deviation, the peak jitter is 62.5 μ s i.e. 0.075 unit interval at 1200 bauds. The mean jitter is half of this. These values are only valid for zero frequency offsets. With offsets, the peak jitter duration becomes $[4(\Delta f - f_{\text{offset}})]^{-1}$. The minimum pulse width possible at the demodulator output, is 5.5 μ s.

When the phase difference between the I and Q channel is precisely 90°, a zero crossing in one channel occurs simultaneously with the peak (positive or negative) in the other (before the limiter), thus allowing the best noise margin at the limiter inputs. If the phase difference differs by θ degrees from 90°, the instantaneous voltage level is the peak level multiplied by $\cos\theta$, when the zero crossing occurs in the other channel. The noise margin is therefore reduced, and it amounts to the same as reducing the level of the received signal while keeping θ at zero degrees. The relative sensitivity thus varies as $20 \cdot \text{LOG}(\cos\theta)$, being maximum when θ is zero i.e. the difference is precisely 90°.

Pager receivers

UAA2080T VHF/UHF paging receiver

6.5 DIGITAL INTERFACE

Output Select

Pin 25 (TS) controls an internal multiplexer that multiplexes pins 26 and 27 as follows.

Pin 25	Pin 26	Pin 27
LOW (GND) or open	Battery Low Indicator, BLI	Data Output, DO
HIGH (VP)	Q-Limiter Output	I-Limiter Output

Table 6.4 Multiplexed Outputs

Data / I-Limiter Output

The data output, pin 27 (DO), is driven by a 20 µA current source/sink, with a 5 kΩ resistor in series with the pin. The voltage swing at this pin is about Vcc - 1 Volt. The rise/fall time of the data signal is

Time (Rise or Fall) = (Vcc-1)*C_{load}/(20 x 10⁻⁶). (6.1)

C_{load} is the capacitive load at pin 27. When using the Philips PCF5001T Decoder, no external load capacitance or series resistance is required on pin 27, or other the interface pins 26 and 28. With ordinary Bit Error Rate meters that do not provide digital data filtering, it is recommended to use a C_{load} of 1 nF for 1200 baud. The rise/fall time is then about 75 µs for a supply of 2.05 volts. C_{load} should be placed close to pin 27 of the UAA2080T. With an ordinary BER meter (e.g. HP3764A), there is more than 1 dB sensitivity improvement when C_{load} is used. The data input to the BER meter was driven by a comparator whose threshold was set at half the UAA2080T supply voltage.

Battery Low Indication / Q-Limiter Output

The battery low indicator output, pin 26 (BLI), is also driven by a 20 µA current source/sink, with a 5 kΩ resistor in series with the pin. This pin is set HIGH when the battery voltage is less than 2.05 V.

Receiver Enable

The internal 1.22 V band-gap reference voltage source is switched on when the receiver enable, pin 28 (RE) is pulled to Vcc, thus enabling the biasing of the entire chip. The receiver turn-on time (time from RE going high till the first valid data bit emerging on DO) depends on the oscillator build-up time. With the onboard crystal oscillator (using circuit and crystals as described in Chapter 2), the receiver enable time was measured to be less than 4 ms.

Pager receivers

UAA2080T VHF/UHF paging receiver

APPENDIX

A) List of Components

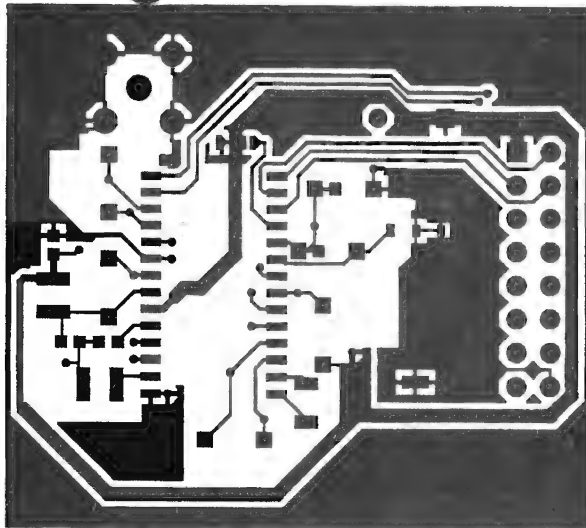
COMPONENT	VALUE		
	470MHz	288MHz	173MHz
R1	330 Ω	330 Ω	330 Ω
R2	47k Ω	56k Ω	56k Ω
R3	680 Ω	680 Ω	1.5k Ω (680 Ω)
R4	1.2k Ω	1.2k Ω	2.2k Ω (1.2k Ω)
R5	1.8k Ω	1.8k Ω	1.8k Ω
R6	5k Ω pot.	—	100 Ω pot.
C1	2.7pF	4.7pF	8.2pF
C2	2.7pF	4.7pF	8.2pF
C3	2.5–6pF	3–10pF	5–20pF
C4	1nF	1nF	1nF
C5	1nF	1nF	1nF
C6	2.5–6pF	3–10pF	5–20pF
C7	2.7pF	3.9pF	8.2pF
C8	2.7pF	3.9pF	8.2pF
C9	2.7pF	3.9pF	8.2pF
C10	22pF	10pF	10pF
C11	22pF	10pF	10pF
C12	2.5–6pF	3–10pF	5–20pF
C13	10 μ F tant.	10 μ F tant.	10 μ F tant.
C14	1nF	1nF	1nF
C15	3–10pF	9–40pF	— (13–50pF)
C16	13–50pF	13–50pF	13–50pF
C17	15pF	15pF	15pF
C18	1nF	1nF	1nF
C19	—	—	—
C20	1nF	1nF	1nF
C21	1nF	1nF	1nF
C22	—	56pF	27pF (82pF)
L1	12.5nH air core	35.5nH air core	43nH air core
L2	8nH	15nH	22nH
L3	8nH	15nH	22nH
L4	40nH	68nH	150nH
L5	40nH	82nH	150nH
L6	8nH	18nH	33nH
L7	8nH	18nH	33nH
L8	100nH	33nH	27nH (68nH)
L9	560nH	560nH	560nH
CRYSTAL	78.325 MHz	48.039 MHz	57.647 MHz

The values in brackets for the 173MHz circuit, are an alternative, that may give a slightly worse spurious rejection.

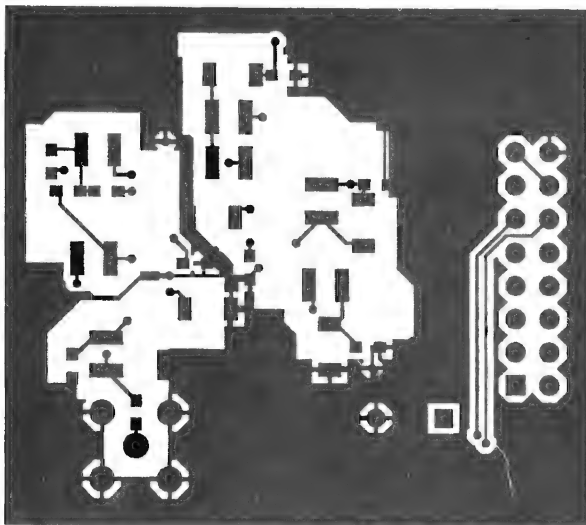
Pager receivers

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B) PRINTED CIRCUIT BOARD

**PHILIPS**

Top Side (scale 2:1)

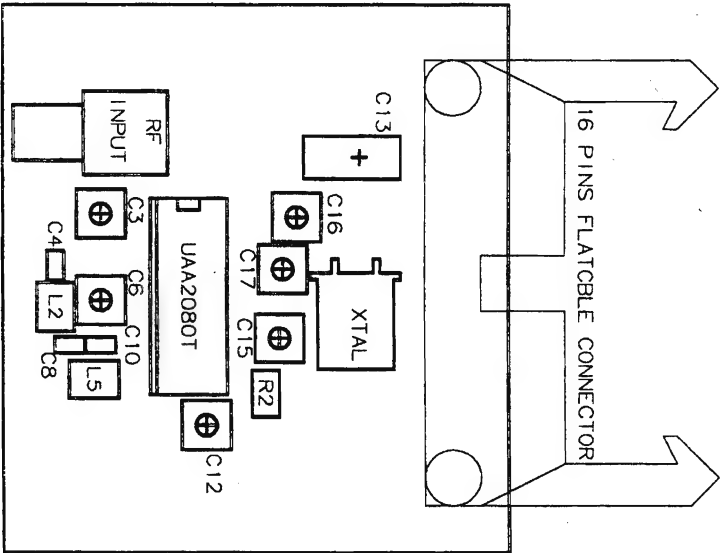


Bottom Side (scale 2:1)

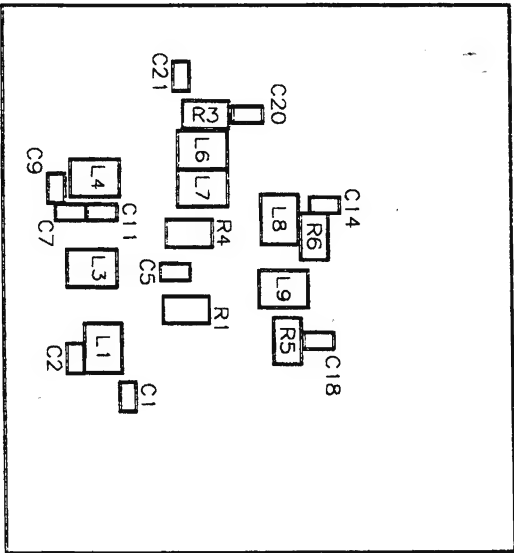
Pager receivers

UAA2080T VHF/UHF paging receiver

Top side



Bottom side
Component placement



CHAPTER 5

PAGER DECODERS

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PCA5000T and PCA5000AT Features and Applications

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PCF5001T versatile POCSAG decoder applications

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PCA5000T and PCA5000AT Features and Applications

SUMMARY:

The PCA5000T Paging Decoder has been designed to decode POCSAG-coded data and to organize and control pager operation for wide-area paging systems. It decodes the POCSAG data received from the paging receiver IC, synchronizes, error-corrects and formats the POCSAG data to provide audio tones and displayed messages.

The Paging Decoder's programmable internal RAM memory not only establishes the two user address codes for the individual pager but also determines the operating mode (alert-only or display pager) and the generation/storage of audio tones to alert the user. To minimize current drain from the main battery, the Paging Decoder switches on the paging receiver IC for the minimum time according to the state of the synchronisation algorithm. The PCA5000T also provides battery low-level alert tones/indication, out-of-range indication and an internal voltage doubler to interface the Paging Decoder directly to a CMOS microcontroller.

The PCA5000T is designed to operate in two configurations. Firstly, as an alert-only pager in combination with a paging receiver IC only. The alert-only pager uses pushbutton control and generates audio tone cadences with a 2 kHz bleeped. Secondly, in combination with a paging receiver IC and a microcontroller, to provide audio tone cadences plus message displays.

Pager decoders

PCA5000T and PCA5000AT Features and Applications

1. INTRODUCTION

The PCA5000T Paging Decoder is a low-power decoder and pager controller specifically designed for use in radiopagers operating at a data bit rate of 512 bits/s. The PCA5000T decodes the CCIR Radiopaging Code No. 1 (POCSAGcode), which is widely used as a transmission code for wide-area paging systems. Used in conjunction with the Philips UAA2033T/UAA2050T Low Power Digital Paging Receivers, the PCA5000T offers an attractive miniature solution for alert-only and display pager applications.

In the alert-only pager mode, the PCA5000T scans the three pushbutton switches, which are then used to switch the pager ON and OFF and to enable the SILENT state. When in the SILENT state, incoming calls are stored until the pager is switched to the ON state again.

In the display pager mode, received calls and messages are transferred to an external microcontroller via the ICs serial communication interface. A built in voltage converter can double the supply voltage to increase the voltage level of the interface signals and thereby enable direct signal transfer between the Paging Decoder and the microcontroller. A 16.384 kHz reference frequency is also generated in the display pager mode, it can be used to drive a real-time clock in the microcontroller.

Call alert cadences are generated when valid calls and messages are received, four different call alert cadences are possible. Status tone cadences are generated following a user status interrogation to indicate the present state of the Paging Decoder. Static on-chip RAM stores two Receiver Identification Codes (RICs) and six special function bits (SPF01-06). The built-in ACCESS synchronisation algorithm is used to synchronize the decoding process to the POCSAG code format.

The PCA5000T is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

The PCA5000T incorporates the following features:

- operates over a wide DC supply voltage range (from 1.7 to 6.0 V)
- requires low DC supply current (typically 15 μ A)
- decodes POCSAG-coded data at 512 bits/s and can be adapted to decode data also at other data bit rates
- incorporates powerful "ACCESS" synchronization algorithm
- supports two user addresses
- provides four different alert cadences
- silent call storage
- interfaces directly to UAA2033T or UAA2050T paging receiver ICs
- directly drives a 2 kHz bleeper
- controls paging receiver IC power consumption to minimize battery current
- contains a non-volatile static RAM memory with back-up battery
- internal voltage converter
- level shifted microcontroller interface signals in display pager mode
- battery low level alert
- out-of-range indication
- contained in a 28-lead mini-pack (S0-28).

Pager decoders

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2. PAGING DECODER OPERATION

This section describes the features and operation of the PCA5000T which are common to both alert-only and display pagers. Specific information relevant to one pager mode only is provided in Sections 3 and 4.

A simplified block diagram of the decoder is shown in fig. 1.

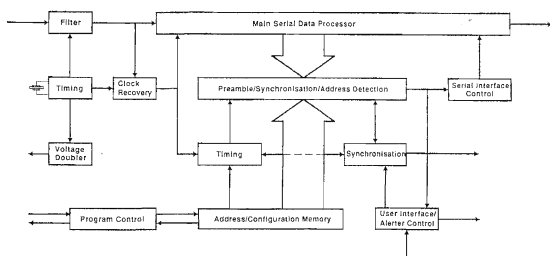


Fig. 1 Functional Blocks PCA5000T

2.1 Decoder Status

The PCA5000T has three internal states: ON, OFF and SILENT. A state is selected by pushbutton operation in the alert-only mode or by static input signals in the display mode.

The ON state is the normal operating state of the Paging Decoder. The PCA5000T controls the receiver enable output to switch the receiver on when needed and to receive POCSAG data, this serial data is subsequently processed by the PCA5000T. When a valid paging call is received, the PCA5000T generates the appropriate call alert cadences.

In the OFF state the Paging Decoder disables the paging receiver IC and no data is processed. However, the crystal oscillator remains operating to ensure that status interrogation is maintained to detect a status change. Also, the 16.384 kHz reference frequency output signal remains active.

In the SILENT state operation is the same as in the ON state except that only special silent override calls are

allowed to generate alert cadences. If, and only if, the Paging Decoder is programmed for the alert-only mode, up to four different calls are stored and alert cadences are generated when the ON state is re-selected.

2.2 Data Reception

2.2.1 Data Input

The data input is fully asynchronous. The data bit rate corresponds to 1/64 of the crystal frequency. The nominal data bit rate is 512 bits/s when a 32.768 kHz crystal oscillator is used. The PCA5000T has been designed to basically operate at a data bit rate of 512 bits/s.

The PCA5000T expects the input data to have positive logic polarity; a logic '1' corresponds to a HIGH level voltage input and a logic '0' corresponds to a LOW level voltage input. The input data may contain jitter and spikes, therefore, the data is first passed through a digital noise filter. The digital noise filter samples the input data at eight times the input data rate. The filtered input data is fed to the main serial data processor and is also used as a reference for the bit clock recovery circuit.

2.2.2 Bit Clock Recovery

An internal bit clock is recovered from the filtered input data, the bit clock is therefore synchronised to the input data and has a nominal frequency equal to the data bit rate, i.e. 512 Hz.

The bit clock tries to sample each data bit at the center of the bit period. The clock recovery algorithm evaluates logic transitions in the data and adds or omits internal clock cycles to shift the sampling instant in fractions of 1/8 of the bit period. Therefore, the time resolution is fixed to 1/8 of the bit duration (1/8 of 1/512 second) per data bit.

The internal sampling clock is derived from the 32.768 kHz crystal oscillator. The bit clock recovery mechanism compensates also for ageing and temperature drift of the crystal oscillator frequency within ± 50 ppm deviation and is also effective if an external clock is used.

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2.2.3 Data Input Format (POCSAG Code)

The PCA5000T decodes the received serial data according to the standards of the CCIR Radiopaging Code No.1 (POCSAG Code). The code format is independent of the data bit rate, however, with an oscillator frequency of 32.768 kHz the PCA5000T only decodes received data with a bit rate of 512 bits/s.

The POCSAG-coded data starts with a preamble, which consists of bit reversals, 10101010..... , for at least 576 bits, see fig. 2.

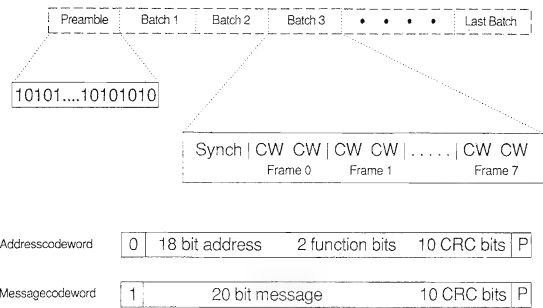


Fig. 2 CCIR Radiopaging Code No. 1 (POCSAG Code)

Normally, the preamble is used to enable the Paging Decoder to acquire bit synchronization and to prepare it for codeword synchronization. After the preamble, batches of codewords are transmitted according to the number of messages to be transmitted. Each batch consists of 17 codewords, each of 32 bit length. The first codeword of each batch is always a synchronization codeword, which synchronizes the Paging Decoder to the POCSAG code structure.

The following 16 codewords are arranged as eight frames, each containing two codewords. These codewords are either address, message or idle codewords. Idle codewords are used to fill empty batches or to separate successive calls.

The address codeword selects a specific pager and classifies a call as being tone only, numeric or alphanumeric. In the POCSAG system a pager user address (Receiver Identification Code, RIC) is defined by

a decimal number from 0 to 2,097,151 represented by a 21-bit binary number. Bit 1 of an address codeword is always a logic '0', bits 2 to 19 are the 18 most significant bits of the 21-bit RIC. The complete addressing is performed by coding the remaining three least significant address bits in the number of the frame, in which the address codeword is transmitted. Bits 20 and 21 of the address codeword are two function code bits which classify the call as tone only, numeric or alphanumeric. Bits 22 to 31 are the Cyclic Redundancy Check bits (CRC) based on (31,21) BCH-codes (Bose, Chaudhuri, Hoquenghem). The polynomial used to generate the BCH codes is:

$$x^{10} + x^9 + x^8 + x^6 + x^5 + x^3 + 1$$

Bit 32 is a parity check bit, to establish even parity for the address codewords. The redundancy introduced in the codewords can be used to increase the call success rate by error detection and correction in the Paging Decoder.

Message codewords contain the information to be displayed when numeric or alphanumeric calls are transmitted. The message codewords are transmitted directly following an address codeword. Messages, which are too long for one message codeword, continue in the codeword positions of subsequent frames and batches until the complete message has been transmitted, see fig. 3.

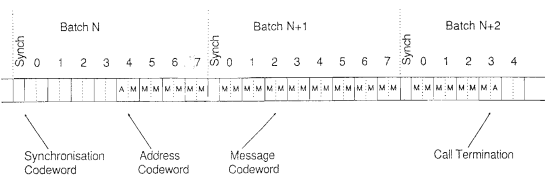


Fig. 3 Message call overflowing into subsequent batches

Bit 1 of a message codeword is always a logic '1' to distinguish it from an address codeword. Bits 2 to 21 contain the information to be displayed, the coding of which is determined by the system provider or the authorities. Bits 22 to 31 are the CRC check bits, which again, together with the parity check bit, improve the message reliability.

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2.2.4 Synchronization Strategy

In order to receive and detect incoming calls the Paging Decoder must achieve synchronization with the POCSAG code structure. In the PCA5000T this is achieved by the Philips ACCESS algorithm, which is a state machine with five internal states. The state machine is active only when the Paging Decoder is in the ON or SILENT states. The state of the algorithm also controls the paging receiver IC power switching algorithm to achieve fast synchronization with low power consumption both for good reception conditions as well as for fading RF signals.

- a) Power on, state 1. The power on state is entered when the pager is switched on or upon selection of either the ON or SILENT states. The paging receiver is enabled and, for up to three seconds, the PCA5000T scans the input data for a preamble or synchronization codeword. If a preamble is detected the algorithm enters the preamble receive state, if a synchronization codeword is detected the algorithm enters the data receive state. If neither is detected within the 3 second interval, the algorithm enters the carrier off state.
- b) Preamble receive, state 2. The paging receiver remains switched on. The PCA5000T checks the POCSAG data bit-by-bit for the preamble and synchronization codeword bit patterns. If neither preamble or synchronization codeword bit patterns are detected within 544 bits the algorithm enters the carrier off state. Preamble detection causes the Paging Decoder to remain in the preamble receive state, while synchronization codeword detection causes the Paging Decoder to enter the data receive state.
- c) Data receive, state 3. This is the normal data receive state, in which the Paging Decoder decodes received calls and messages. The Paging Decoder scans both the synchronization codeword position and the frame programmed by the user address in every batch. The codewords received in the frames are processed as described in Section 2.2.5.
If the Paging Decoder fails to recognize a synchronization codeword, the algorithm enters the fade recovery state. Otherwise, the algorithm remains in the data receive state. If however, a preamble is

detected the algorithm enters the preamble receive state.

- d) Fade recovery, state 4. The Paging Decoder attempts to compensate for bit shifting which can occur due to fading of the RF signal. It checks for the preamble and synchronization codewords where the synchronization codeword is normally expected from the previous data. These checks are performed exactly at the normal expected synchronization codeword position but also one bit before and after the expected position. This is equivalent to a synchronization codeword sampling window with a one-bit margin on both sides of the expected synchronization codeword.

When a preamble is detected the preamble receive state is entered. If a synchronization codeword is detected, the algorithm switches back to the data receive state. Otherwise the fade recovery state is maintained for 15 batches, after this, a timeout switches the Paging Decoder into the carrier off state.

- e) Carrier off, state 5. In the carrier off state, the PCA5000T scans the received data for a 32-bit block every 18 codewords, 18 codewords are equal to one complete batch plus one codeword. As each new bit is received, the algorithm checks for a preamble or a synchronization codeword on the most recently received 32 bits. Data processing is performed discontinuously, the most recent 32 bits of data consist of n bits taken from the current block and $(32 - n)$ bits taken from the previous block (using a gated shift register). Therefore, the algorithm shifts a 32-bit sampling window over every bit position to sample every bit position within the time of 17 batches. The carrier off state is maintained until either a preamble is detected, whereupon the preamble receive state is entered, or when a synchronization codeword is detected, whereupon the data receive state is entered.

2.2.5 Call Reception

2.2.5.1 Address Scanning and Detection

Address scanning is performed only when the Paging Decoder is in the data receive state, described in Section 2.2.4. Address scanning comprises the input of the two

Pager decoders

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codewords within the frame of each batch determined by the frame number programmed into the Paging Decoder RAM memory. Each of the received codewords is error-corrected and, if the result of error correction is a valid codeword and if it is an address codeword, then bits 2 to 19 of the address codeword are compared with each of the 18-bit user addresses stored in the Paging Decoder RAM memory (see Section 2.2.3). If the comparison gives a true result, the Paging Decoder has detected a call. This causes the Paging Decoder:

- to store the two function code bits (bits 20 and 21 of the address codeword) for correct cadence generation
- to wait for message codewords which may follow directly after the address codeword
- to initiate a message transfer via the microcontroller interface start command.

2.2.5.2 Call Termination

The PCA5000T is capable of handling message calls. The message codewords of a message call follow the address codeword directly and occupy codeword positions in the succeeding frames (i.e. $N + 1$, $N + 2, \dots$) and batches, see fig. 3. However, irrespective of the message call length, synchronization codewords are still received.

When the PCA5000T has received a valid address codeword it keeps the paging receiver enabled to receive subsequent codewords until one of the following call termination conditions is fulfilled:

- the last received codeword is an address codeword
- a synchronization codeword is not detected at the beginning of the current batch, i.e. the state mechanism has left the data receive state
- an idle codeword is received
- error correction is unable to regenerate the last received codeword.

Termination of a call is signalled by the Paging Decoder by sending a stop command via the microcontroller interface.

2.2.6 Error Correction Algorithms

As explained in Section 2.2.3, the POCSAG codewords contain CRC (redundancy) bits which can be used to increase the call success rate by performing error correction on the received codewords. In the PCA5000T four different error-correction algorithms are implemented:

- preamble: a four-bit random error correction is performed when inputting preamble
- synchronization codeword: the Paging Decoder can correct two randomly distributed bit errors within the 32-bit synchronization codeword
- address codeword: a four-bit burst error correction algorithm is applied to the address codewords. (Burst error means that the errors lay all within a field of the burst length, i.e. four bits in this case)
- message codewords: a single bit error within one message codeword can be corrected by the Paging Decoder. If Special Programmed Function Bit SPF03 is a logic '1', the four-bit burst error correction algorithm is applied to the message codewords associated with RIC B. Function Codes (FC) 00 and 11 (see Section 2.8.2).

When the error correction facilities are considered it must be taken into account that increasing the number of bit errors that can be corrected also increases the false call rate. The false call rate has to do with calls that you recede but which were not originally addressed to you. This is a general problem of error correction using forward error correction codes and methods.

2.2.7 Paging Receiver Power Control

The bipolar paging receiver IC consumes the most power in a pager. Therefore, the paging receiver IC has to be switched off as often as possible to maximize battery economy, see fig. 4. The PCA5000T provides a paging receiver power control facility activated by the receiver enable output signal RE (pin 10) which is used to achieve a very low average paging receiver power consumption.

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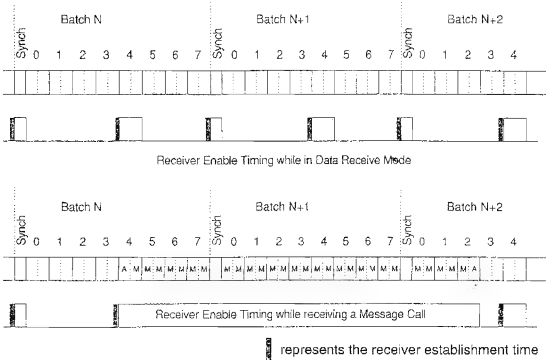


Fig. 3 Receiver power control

The receiver enable output signal (RE) is set to a logic HIGH when the Paging Decoder requires data from the paging receiver. Since most of the paging receivers require some time to settle and to come into a stable operating state, the RE signal activates the paging receiver for a time equivalent to 16 bits before the data is actually required (31.25 ms at 512 bits/s). Paging receiver switching depends on the current state of the synchronization mechanism (refer to Section 2.2.4):

- power on, state 1: the paging receiver is always enabled
- preamble receive, state 2: the paging receiver is always enabled
- data receive, state 3: the paging receiver is enabled for the synchronization codeword and for the frame defined by the pager's user address. The resulting duty cycle depends on the programmed frame number:
 - $d = 4/17$ for frames 1,2, 3, 4, 5, 6
 - $d = 7/34$ for frames 0 and 7.
- fade recovery, state 4: the paging receiver is enabled only for the synchronization codeword enlarged by one bit on both sides; this results in a duty cycle of approximately $1/11$ (50/544).

- carrier off, state 5: the paging receiver is enabled for the duration of one codeword (32 bits) every 18 codewords; the resultant duty cycle is $3/32$.

The duty cycle values quoted above include the paging receiver establishment time. The average paging receiver duty cycle is determined by the reception conditions since the Paging Decoder may switch between states as the RF signal strength varies.

2.3 Crystal Oscillator

A 32.768 kHz crystal oscillator generates all the internal and external timing and drive signals. The crystal oscillator frequency is 64 times the data bit rate of the incoming POCSAG data. Crystal frequency deviations of up to about ± 50 ppm due to aging or temperature drift are compensated for by the bit clock recovery mechanism described in Section 2.2.2. However, we recommend to use a crystal with no more than ± 20 ppm tolerance.

The crystal forms part of a two pin oscillator circuit, X1, pin 5, is the input and X2, pin 6, is the output of the internal inverter. A 4.7 MOhm resistor between X1 and X2 closes the feedback loop while a capacitor (30 pF, typical) from X1 to VDD allows the crystal oscillator frequency to be trimmed. A variable capacitor may be used in this place in order to allow for trimming of the reference frequency output, see also fig. 5.

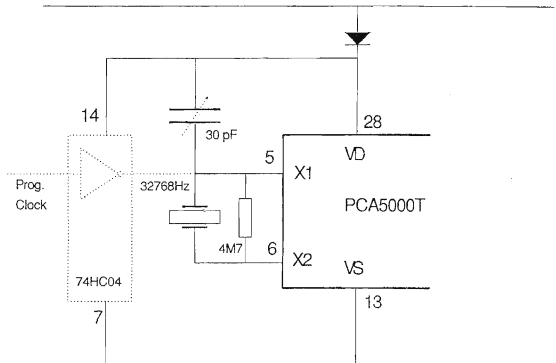


Fig. 5 PCA5000T Clock Drive Circuitry

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Circuitry During programming X1 is the input for the program clock signal. In this case, X1 can be driven directly from a CMOS inverter output (e.g. 74HC04), normal crystal oscillator operation is then suspended. However, the other external components may remain connected to the Paging Decoder. The X1 signal input during programming must be within the specified signal limits.

2.4 Alerter Interface

The PCA5000T can drive either a 2 kHz magnetic or a piezoceramic alerter to generate the audible call alert cadences and status indication tones. The alerter drive frequency is set to 2048 Hz with a 32.768 kHz crystal oscillator, the alerter drive signal is a modulated squarewave.

Two outputs from the PCA5000T are provided to drive the alerter:

- Output AL (pin 11) for a low-level intensity alert cadence. In this case, a 680 Ohm resistor is connected between AL and the alerter, the other end of the alerter must be connected to VDD. AL can be considered as an open drain output.
- Output QR (pin 8) for a high-level intensity alert cadence. QR is fed to an external transistor which drives the alerter at a high-level intensity. QR is not available when the vibrator option is used. Output QR can be considered to be a current source supplying a drive current to the base of the external transistor.

Outputs AL and QR have inverse polarity with respect to each other, so that if QR is a logic HIGH then AL is a logic LOW, and vice versa.

Figure 6 gives an example of the required external circuitry.

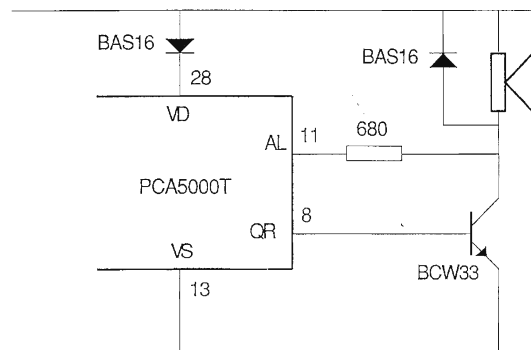


Fig. 6 PCA5000T Alerter Drive Configuration

2.4.1 Alert Cadence Generation

The Paging Decoder generates call alert cadences by sending a pulse modulated 2048 Hz squarewave to the alerter. The shape of the alert cadence (modulation pattern) is determined by the two function code bits of the address codeword (bits 20 and 21, as shown in Fig. 7).

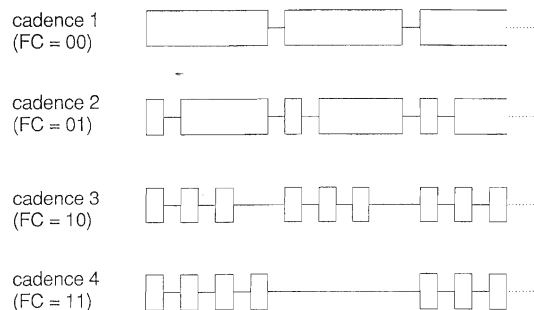


Fig. 7 PCA5000T Alert Cadences

Alert cadences are generated if the Paging Decoder is in the ON state and a valid call is received, or if the Paging Decoder is in the SILENT state and a silent override call is received, or if the Paging Decoder is programmed as an alert-only pager and it is switched from SILENT to ON and calls have been stored in the SILENT state.

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Alert cadence generation does not commence before one of the call termination conditions is satisfied, see Section 2.2.5.2. No alert cadences are generated in display pager mode (SPF01 = 1) if SPF02 is programmed to be a logic LOW and the call was not successfully terminated, i.e. the error correction algorithm failed to generate a valid codeword, see also table 1.

During the first four seconds low intensity alert cadences are generated by driving the AL output signal only. For the following 12 seconds the QR output is driven simultaneously to increase the alert cadence intensity. The high intensity alert cadences are not available if the vibrator option is in use. In this case, low intensity alert cadences continue for a further 12 seconds. Call alert cadences are automatically terminated after 16 seconds.

2.4.2 Status Indication

The Paging Decoder generates status indication tones as a result of user status interrogation, see Fig. 8. Status indication tones are generated always at low intensity, only the output AL is driven.

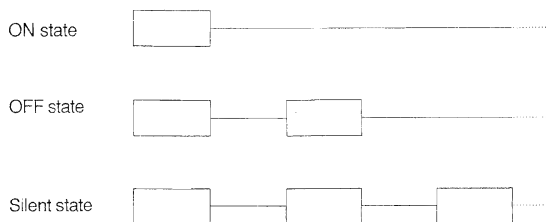


Fig. 8 PCA5000T Status Indication Tones

2.5 Vibrator Interface

A logic HIGH level on the QS input, pin 19, enables the vibrator logic and switches QR from the high intensity alert cadence output to the vibrator output. This disables the high intensity alert facility.

The QR output is capable of driving an external transistor to switch a vibrator-type alerter. The QR output is normally a logic LOW. If the Paging Decoder is in the SILENT state with the vibrator option enabled, no alert

cadences are generated when calls are received. Instead the QR output is switched to a logic HIGH for the duration of a normal alert cadence (16 seconds) or until terminated by the user. Silent call storage and silent override call facilities are disabled.

2.6 Out Of Range Indication

The PCA5000T provides a signal to indicate that the pager is not receiving any useful data, which means normally that it is out of the range of the transmitter. The output OR, pin 9, indicates an out-of-range condition. OR can drive an external transistor and is normally a logic LOW, refer to fig. 9.

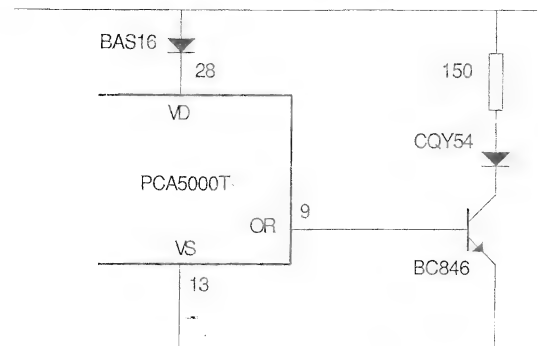


Fig. 9 PCA5000T Out of Range Indication

The out-of-range condition is derived from the synchronization state machine: when the Paging Decoder is in the carrier off state, the out-of-range condition is satisfied and output OR is set to a logic HIGH for the duration of the synchronization scan period. The output OR is modulated with a 2048 Hz squarewave, the resulting duty cycle is approximately 1/36.

Outputs OR and QR can be connected together to provide acoustic high-intensity out-of-range indication. However, diodes should be used to decouple the two outputs, if the resulting out-of-range indication during a high-level alert and vibrator activation is not desired. The out-of-range indication continues as long as the out-of-range condition is maintained, it cannot be terminated by the user.

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2.6 Power Supply

The PCA5000T is designed to operate from two battery power supplies. The main battery supplies power to the Paging Decoder and its external circuits. The second battery, normally a lithium cell, is used to retain the contents of the internal RAM memory when the main battery is disconnected from the Paging Decoder, for example during a main battery change.

An RC filter in the main battery supply to the Paging Decoder ensures that voltage supply transients (ramp up and ramp down) are sufficiently damped.

The second (back-up) battery is connected between VD, pin 28, and VB, pin 1. The main battery supply voltage must not exceed the back-up battery voltage by more than 0.8 V due to an internal diode between VS and VB.

The voltage supply input VS, pin 13, should not be left open-circuit when the main battery supply is disconnected. Instead, VS should be biased to approximately -0.9 V relative to VD to prevent the Paging Decoder from malfunctioning. This biasing is achieved by the 2.2 MOhm resistor between VB and VS. The recommended power supply connections are shown in Fig. 10.

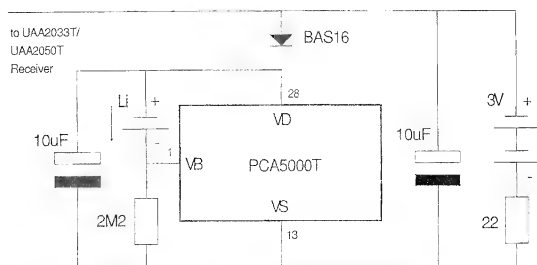


Fig. 10 PCA5000T Power Supply Scheme

2.7 Battery Control Logic

The PCA5000T includes built-in battery low-level control logic which monitors the condition of the main battery. A logic signal representing the actual condition of the battery must be supplied to the battery low-level input BS,

pin 12. A logic LOW level represents a good battery condition where as a logic HIGH level indicates that the main battery needs to be replaced. The Philips UAA2033T/UAA2050T integrated VHF/UHF digital paging receivers contain internal battery low-level detectors which provide an output signal to drive the BS input of the Paging Decoder directly.

The PCA5000T samples the input battery low-level signal BS at the end of each synchronization scan period when the ON or SILENT states are selected. Each logic level sample is copied to the battery low-level output BL, pin 15. As soon as four consecutive samples are a logic HIGH level a continuous high intensity alert tone is generated if the pager is programmed as an alert-only pager. This battery low-level alert tone is reset when the user operates one of the pushbuttons. After a reset the battery low-level control logic is disabled until re-enabled by selecting the OFF state.

2.8 Programming

The PCA5000T uses its internal static CMOS RAM memory to store two 18-bit address codes A and B, the three common frame number bits (FR0-2) and the six programmable Special Function Bits (SPF01-06), see Fig 11.

	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
WORD 0	A08	A07	A06	A05	A04	A03	A02	A01	A00
WORD 1	A17	A16	A15	A14	A13	A12	A11	A10	A09
WORD 2	B08	B07	B06	B05	B04	B03	B02	B01	B00
WORD 3	B17	B16	B15	B14	B13	B12	B11	B10	B09
WORD 4	FR2	FR1	FR0	SP6	SP5	SP4	SP3	SP2	SP1

Fig. 11 PCA5000T RAM Organisation

The RAM memory is organised as 5 words each of 9 bits. The lithium battery connected between VD and VB ensures data retention when the pager is disconnected from the main supply. A serial interface enables read and write access to the RAM memory and a special operating mode enables the RAM memory to be programmed and verified.

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2.8.1 Receiver Identification Code Mapping

Every user in a POCSAG paging system has a 21-bit Receiver Identification Code (RIC) which must be programmed into the Paging Decoder. The PCA5000T supports two RICs simultaneously, RIC A and RIC B, but in order to minimise battery power consumption both RICs must share the same frame number. Therefore, prior to programming, the two RICs are divided into two 18-bit address codes with one common 3-bit frame number. The 18-bit address codes are programmed into the appropriate RAM memory address bit locations while the frame number is programmed into bits FR0-2. An example with RIC A = 2468 (Dec.) and RIC B = 12468 (Dec.) is shown in Fig. 12.

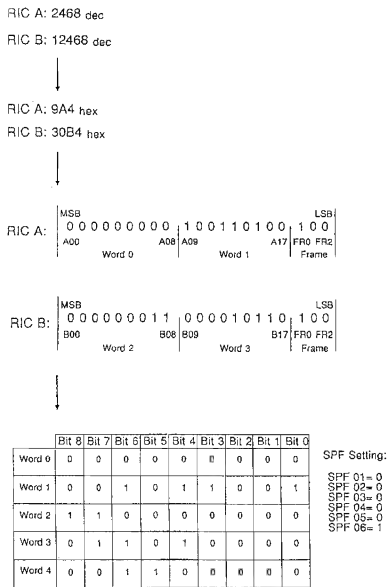


Fig. 12 Programming Example

2.8.2 Special Programmed Function Bits (SPF01-06)

In the PCA5000T, six bits of the internal RAM memory are the Special Programmed Function Bits (SPF01-06) which select the pager operating mode (alert-only or display pager) according to requirements, and allow the

choice of various options. Table 1 lists the bits SPF01-06 and their function.

TABLE 1

Special Programmed Function Bits

bit level option

- SPFO1: 0 selects alert-only pager mode
- 1 selects display pager mode
- SPF02: 0 enables voltage converter, if SPFO1 = 1.
Alert cadences are generated only for correctly received messages (applicable to FC = 00 and 11 only)
- 1 disables voltage converter, if SPFO1 = 1.
Alert cadence 1 is used also when FC = 11
- Note: SPF02 is active only if SPFO1 = 1!
- SPF03: 0 1-bit error correction on message codewords
- 1 4-bit burst error correction on message codewords for RIC B. FC = 00 or 11
- SPF04: Not used, user programmable
- SPF05: 0 silent override enabled on RIC B. FC = 01, 10, if SPFO1 = 1
- 1 silent override enabled on RIC B. FC = 00, 11, if SPFO1 = 1
- SPF06: 0 disable silent override on RIC A, FC = 10
- 1 Enable silent override on RIC A, FC = 10.

2.8.3 Program Timing

As previously mentioned, a serial interface is used to write data into the RAM memory and to read the stored data. Input DI, pin 3, and output DO, pin 20, are the RAM memory input and output pins respectively. Input PR, pin 2, selects the programming mode and the clock input X1, pin 5, serves as the shift clock input. The normal

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32.768 kHz crystal oscillator operation is disabled in the programming mode, however, the external components can be left connected to pins X1 and X2.

To enter the programming mode, PR has to be a logic HIGH level (i.e. connected to VD), during the power-on time. To leave the programming mode, the main battery supply is disconnected from VS. The back-up battery must remain connected to the PCA5000T to retain the RAM memory data when the main battery is disconnected.

During programming, inputs ON, OF, and SK (pins 18, 17 and 16) must not all be logic HIGH at the same time. In the programming mode, the voltage converter and the reference frequency output FL are disabled. No external voltage may be connected to VP when in the programming mode otherwise incorrect programming may result.

The RAM memory data can only be programmed (write) and verified (read) in a bit-by-bit, word-by-word sequence for the complete five data words in turn, starting with bit 0, word 0. The programming mode should be left as soon as the complete write or read sequence has been performed.

The timing of the program interface signals during a write and read operation is shown in Fig. 13.

The exact timing specification is given in the data sheet for the PCA5000T Paging Decoder. However, it is possible to slow the timing down sufficiently so that the five data words can be manually input into the RAM memory.

2.8.4 Recommended Program Interface

This section provides background information to program the PCA5000T in a production environment and how to arrange the external circuitry to allow easy and quick programming. It is assumed that during production no main power supply is connected to the Paging Decoder but that the back-up battery is connected.

The programming control inputs PR and WR have internal biasing resistors of a sufficiently low impedance to render the inputs inactive even if the pins are open-circuit during normal operation, thus ensuring safe

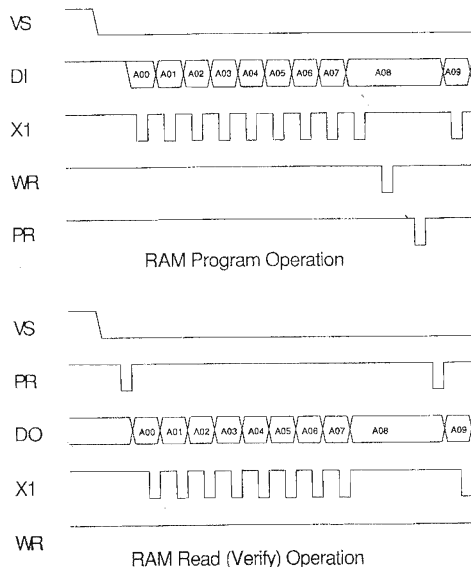


Fig. 13 PCA5000T Program Interface Timing

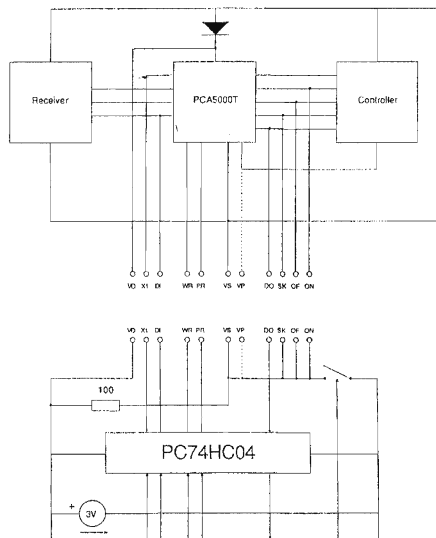


Fig. 14 PCA5000T Program Interface & Connections

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operation of the Paging Decoder. Therefore, normally no external biasing resistors are required on these inputs. Provide pads for probe connections to the following pins of the Paging Decoder: VS, VD, DI, DO, X1, PR, ON, OF, SK, VP and WR. Inputs DI, X1, PR and WR can be driven by a standard CMOS output, i.e. 74HC04; output DO can feed CMOS inputs. Ensure that the driver output voltages are compatible with the specified signal input range of the PCA5000T.

The Paging Decoder is separated from the other circuitry of the pager by a diode, see Fig. 14. Pads VS and VD are connected to an external power supply, which is initially switched off. All the driver outputs have to be at a logic HIGH level.

Perform the following sequence:

- connect the probe to the assembled printed-circuit board
- switch on the external voltage supply
- wait for internal power-on reset duration
- perform the required write or read sequence according to the timing shown in Fig. 13 and as specified in the PCA5000T Paging Decoder data sheet
- set all driver outputs to a logic HIGH level
- switch off the power supply, remembering that the voltage transient has not to be too fast
- disconnect the probe from the printed-circuit board.

If first a programming and then a verify operation are to be performed it is possible to go from step f) to step b) without disconnecting the probe.

One possible pager and probe configuration with the relevant connections for programming is shown in Fig. 14. The probe has also to incorporate the required level shifting from 3 V to the specific logic level of the driver circuitry. It may also be necessary to use additional pads to test the paging receiver and the microcontroller. The supply voltage must never exceed the back-up battery

voltage by more than 0.8 V, however, both voltages should be approximately the same during programming.

3. ALERT-ONLY PAGER APPLICATION

The PCA5000T supports an alert-only pager mode, selected by programming SPF01 to a logic LOW. In this mode no external microcontroller is required so that the complete alert-only pager consists of two ICs only, the PCA5000T plus a paging receiver like our UAA2033T (VHF) or UAA2050T (UHF) Integrated Digital Paging Receivers, see fig. 15.

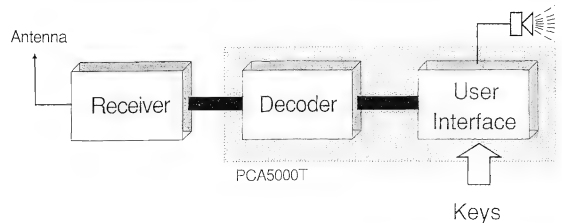


Fig. 15 Alert-Only Pager Functional Blocks

The PCA5000T performs the complete decoding, paging receiver control and user interface control functions.

3.1 Switch Interface

In the alert-only pager mode the PCA5000T accepts user inputs via a pushbutton interface. Three pushbutton-type switches are required, the three pushbuttons are connected between VD and the corresponding ON, OF and SK inputs (pins 18, 17, and 16). These inputs have internal pull-down resistors in the alert-only mode.

The PCA5000T periodically scans the three inputs to detect pushbutton operation, pushbutton operation causes the Paging Decoder to react accordingly. When two or more pushbuttons are pressed simultaneously the Paging Decoder ignores the pushbutton inputs until all the pushbuttons are released.

3.1.1 Status Selection

Each of the three pushbuttons is related to one of the

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three internal states of the Paging Decoder: the ON pushbutton relates to the ON state, the OF pushbutton relates to the OFF state and the SK pushbutton to the SILENT state. After power-on, the Paging Decoder is always in the ON state. A state is selected by pressing the appropriate pushbutton for at least 1.5 seconds. The Paging Decoder first indicates the current state and, after 1.5 seconds, indicates selection of the new state by generating status indication tones.

3.1.2 Status Interrogation

Pressing any of the three pushbuttons ON, OFF or SILENT for a duration less than 1.5 seconds causes the decoder to generate status indication tones, refer to section 2.4.2.

3.1.3 Alert Cadence and Battery Low Alarm Termination

When any of the ON, OFF or SILENT pushbuttons is pressed for less than 1.5 seconds the Paging Decoder terminates the generation of call alert cadences, vibrator operation or battery low-level alarm tones.

High-level intensity alert tones generated by activation of the alarm input AI, pin 14, can only be terminated by re-setting AI to its LOW-level inactive state. Input AI has an active internal pull-down resistor in the alert-only mode.

3.2 SILENT State Operation

The SILENT state is intended for users who do not wish to be disturbed by the alert cadences resulting from incoming calls.

3.2.1 Silent Call Storage

The PCA5000T includes silent call storage to record incoming calls when the pager is in the SILENT state. Silent call storage capacity is limited to four calls, calls received with the same function code are stored only once. The user is alerted to stored calls when the pager state is changed from SILENT to ON again. The stored calls are fed to the alerter starting with function code 00, irrespective of the order in which they were originally received. Silent override calls are not

stored in the silent call storage.

Silent call storage is inhibited if the vibrator option is used.

3.2.2 Silent Override Feature

The PCA5000T provides a silent override feature, which classifies the calls as urgent and allows them to override the SILENT state of the pager. The silent override feature is determined by the RIC and the function code of the address codeword received. When in the alert-only mode, all calls received with RIC B possess the silent override attribute, the special programmed function bit SPF05 is irrelevant. In addition, silent override on RIC A, function code 10, is enabled by programming SPF06 to a logic HIGH level. Silent override calls receded in the SILENT state cause the normal alert cadences to be generated. The silent override feature is not available if the vibrator option is in use.

3.3 Feature Not Available In The Alert-Only Pager Mode

The following features are not available if the PCA5000T is in the alert-only pager mode, i.e. when SPF01 = 0:

- the voltage converter is always disabled, VP must be connected to VS
- the reference frequency output FL is disabled
- no level shifting is provided for the microcontroller interface signals, since VP must be connected to VS
- the ON, OF and SK inputs are configured to pushbutton interface, the static input configuration is not available
- input PC is irrelevant and must be connected to VS
- input AI should be connected to VS if it is not driven by additional external logic
- alert cadences are always generated, no matter if the call was successfully terminated or not.

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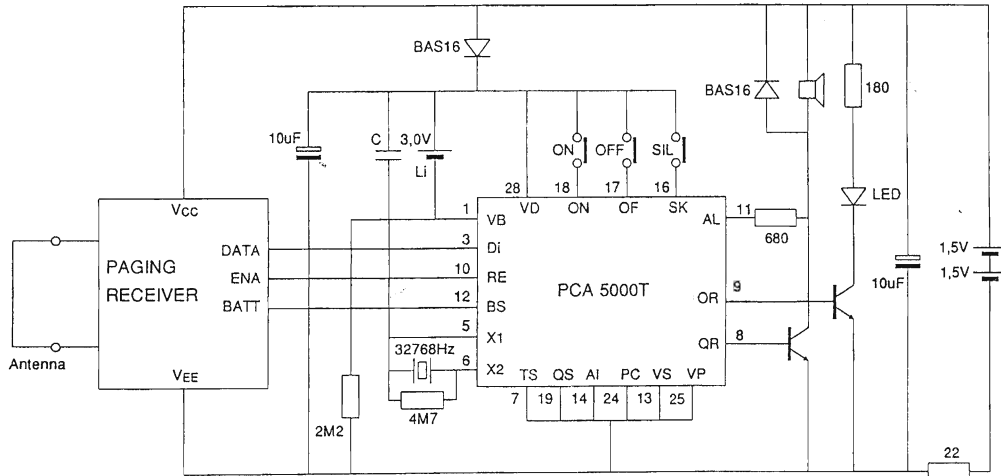


Fig. 16 PCA5000T Beep-Only Pager Application

3.4 Circuit Diagram

The circuit diagram of an alert-only pager using the PCA5000T is shown in Fig. 16. Neither the program interface nor the external components of the paging receiver are shown for clarity.

4. DISPLAY PAGER APPLICATION

The PCA5000T in the display pager mode easily supports numeric and alphanumeric pager applications, see fig. 17 for a functional block diagram. The display pager mode is selected by programming the Special Programmed Function bit SPF01 to a logic HIGH.

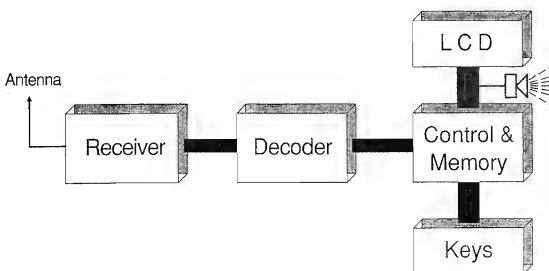


Fig. 17 Display Pager Functional Blocks

A serial microcontroller interface is provided for transfer of received calls and messages to an external microcontroller for postprocessing and generation of display information.

4.1 Microcontroller Interface

4.1.1 Status Selection

In the display pager mode the state of the Paging Decoder is determined by the logic levels applied to the ON and SK inputs. In the display pager mode these are fully static inputs without internal biasing resistors. The logic to select the ON, OFF or SILENT states is shown in Table 2.

TABLE 2
display pager state logic

state input	ON input	input SK
ON	HIGH	LOW
OFF	LOW	don't care
SILENT	HIGH	HIGH

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A status change is performed simply by applying new logic levels to the inputs ON and SK according to the logic levels shown in the logic table. A status change in the display pager mode does not automatically cause status indication tones to be generated.

4.1.2 Status Indication

The Paging Decoder input OF, pin 17, is also a static input in the display pager mode and is normally a logic LOW. A positive-going pulse on input OF causes the Paging Decoder to generate status indication tones according to the currently selected status as long as no alert cadences or battery low-level alarm tones are being generated.

4.1.3 Alert Cadence and Battery Low Alarm Termination

If either alert cadence generation or battery low-level alarm is active, a positive-going pulse on input OF terminates the existing tone generation. No status indication tones are generated in this case. Tones caused by the activation of the alarm input AI, pin 14, are not terminated by pulsing the OF input.

4.1.4 Alarm Input

The PCA5000T can generate high-level intensity alarm tones, alarm tone generation is activated by a logic HIGH level on the AI input, pin 14. Alarm tone generation takes precedence over all other tone generation and continues as long as AI is a logic HIGH level. Input AI may be pulsed to generate a modulated alarm tone output, a feature which can be used to create alert tone cadences other than those normally implemented in the Paging Decoder. The AI input has no internal biasing input in the display pager mode.

4.1.5 Serial Microcontroller Interface

The PCA5000T incorporates a serial microcontroller interface to transfer call and message information from the Paging Decoder to the external microcontroller.

Serial data is transferred bit-by-bit on output DO, pin 20, a bit is valid whenever the data strobe output DS, pin 22,

is a logic LOW.
After a valid address codeword has been received the serial data transfer commences with a start command from the Paging Decoder to the microcontroller. The start command consists of eight bits (bit 0 is transmitted first) as shown in Table 3.

TABLE 3
start command format

start bit logic level	
Bit Meaning	
0	always 0
1	always 1
2	SPF03, as programmed
3	SPF06, as programmed
4	SPF05, as programmed
5	0, call received for RIC A 1, call received for RIC B
6	bit 20 of the received address codeword
7	bit 21 of the received address codeword

Bits 6 and 7 are the function code information which has been transmitted with the address codeword.

After the start command the message information of the message codewords is transmitted over the serial microcontroller interface in the message word format. Each message word consists of 24 bits, the first four bits are logic HIGH while bits 4 to 23 contain bits 2 to 21 of the received message codewords. The message information transfer continues until one of the call termination conditions is fulfilled. The end of a message transfer is defined by the transmission of a stop command which has the eight bit format shown in Table 4.

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TABLE 4

stop command format

stop bit logic level

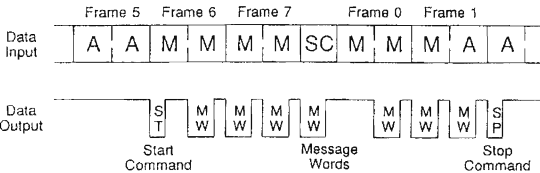
Bit Meaning

- 0 always 0
- 1 always 0
- 2 0, unsuccessful termination (uncorrectable
 codeword received or synchronisation lost)

 1, successful termination (address or idle codeword
 detected)
- 3 inverted copy of QS input
- 4 SPF04 as programmed
- 5 SPF02 as programmed
- 6 undefined
- 7 undefined

The end of a successful message transfer may also be indicated by sending a second start command word if the pager receives two successive calls.

An example of a complete message transfer is shown in Fig. 18 with a seminary of the start and stop command word formats.



a) Message Output Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	SPF 03	SPF 06	SPF 05	R/C A/B	Address CW Bit 20	Bit 21

b) Start Command Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 23
1	1	1	1		Message Codeword Bit 2 to Bit 21 as received

c) Message Word Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	0	ST	QS Input	SPF 04	SPF 02	Not Used	Not Used

d) Stop Command Format

Fig. 18 Serial Communication on Microcontroller Interface

4.1.6 Reference Frequency Output

The PCA5000T generates a reference frequency signal on output FL, pin 23, when operating in the display pager mode. The FL signal is a 16.384 kHz squarewave to enable the microcontroller to clock a timer or to drive a real-time clock. The reference frequency is derived directly from the crystal oscillator of the Paging Decoder.

The reference frequency FL is not generated when the Paging Decoder is in the programming mode. This feature can be used to check for proper entrance to the programming mode.

4.1.7 Battery Low Level Output

Each time the PCA5000T samples the battery sense input BS, the sampled logic value is output on the battery low output BL, pin 15. This output logic signal is intended to be fed to the external microcontroller to enable evaluation of the battery condition. In the display pager mode, the PCA5000T does not automatically generate battery low-level alarm tones; the microcontroller should use the AI input to signal to the user the battery is in a bad condition.

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4.2 Voltage Doubler

The PCA5000T contains an internal voltage converter to provide doubled supply voltage to the external microcontroller and other external circuits (e.g. LCD drivers). To use the internal voltage converter a 220 nF capacitor is connected between pins CN and CP, the Paging Decoder must be in the display pager mode (SPF01 = '1') and Special Function Bit SPF02 must be a logic LOW (SPF02 = '0').

The output voltage on VP, pin 25, is then set to approximately twice the voltage on VS, pin 13, measured with respect to the common reference VD.

The output impedance of the voltage doubler output VP is determined by the voltage converter control input PC, pin 24. If PC is a logic HIGH the voltage doubler output has a high output impedance, if PC is a logic LOW the voltage doubler output has a low output impedance.

When the voltage converter is selected the logic LOW voltage level for all the microcontroller inputs and outputs are shifted more negative, since VP is the LOW level reference voltage for the microcontroller's input and output stages. This voltage level-shifting facility enables the PCA5000T to operate directly with CMOS microcontrollers using Vpr as the microcontroller's supply voltage, see fig. 19.

If the power supply requirements of the external circuitry exceed the drive capability of the internal voltage converter an external power supply can be connected. The internal voltage converter is guaranteed to provide a minimum output current of 150 μA , $V_{\text{pr}} = -2.7\text{ V}$, when $V_{\text{S}} = -2.0\text{ V}$ and $\text{PC} = 0$ (all voltages measured with respect to VD). If an external power supply is required, in most cases also a voltage converter, the pump capacitor is removed from pins CN and CP and the external power supply is connected directly to VP. The voltage level-shifting of the serial microcontroller interface signals is maintained. An example of the power supply connections using an external voltage converter is shown in Fig. 20.

4.3 Silent Override Feature

The silent override feature is also available in the display

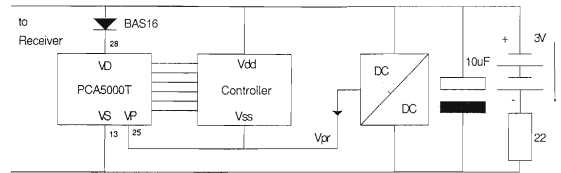


Fig. 20 PCA5000T with external Voltage Converter

paper mode. Calls and messages received with pre-defined addresses cause alert cadence generation even when the SILENT state has been selected. Silent override is enabled for calls with RIC B. function codes 01 and 10, if SPF05 = 0. Silent override is enabled for calls with RIC B. function codes 00 and 11, if SPF05 = 1. In addition, silent override is enabled with RIC A, function code 10, if SPF06 = 1.

Serial message transfer over the serial microcontroller interface, described in Section 4.1.5 will always occur, independent of the silent override feature as long as the Paging Decoder is not in the OFF state. Therefore, silent call storage is not required and is disabled in the display pager mode.

4.4 Features Not Available In The Display Pager Mode

The following features are not available if the PCA5000T is operated in the display pager mode:

- silent call storage is disabled
- battery low-level alarm tone generation is disabled
- input AI has no internal biasing resistor
- silent override on RIC B is determined by the function codes selected by SPF05
- inputs ON, OF and SK are in the static input mode without internal biasing resistors in the Paging Decoder.

Note that the out-of-range output OR is not level-shifted but can still drive an external bipolar transistor. Additional hardware may be required to interface the signal OR with the microcontroller.

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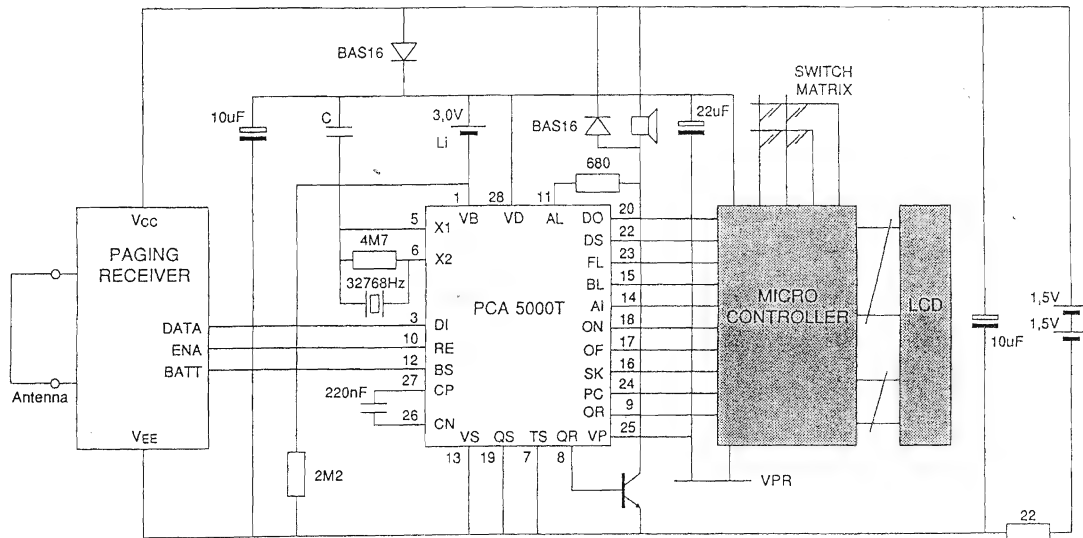


Fig. 19 PCA5000T Display Pager Application

4.5 Circuit Diagram

The circuit diagram of a display pager with the PCA5000T in the display pager mode is shown in Fig. 19. The connections to the program interface and the external components of the paging receiver are not shown for clarity.

5. OPERATING THE PCA5000T AT OTHER BAUD RATES

The PCA5000T was originally designed to be used in paging systems operating at a data bit rate of 512 bit/s. Nevertheless, the Paging Decoder can also be used in POCSAG paging systems with a different baud rate by changing the crystal oscillator frequency. However, there are some differences and restrictions which have to be taken into account when the crystal oscillator frequency is changed. Consult your local Philips Sales Organization before operating the PCA5000T at a different baud rate.

This section describes how to adapt the PCA5000T to 1200 bit/s operation and the changes in the parameters

which will occur. Parameters not mentioned can be calculated by scaling the corresponding value for 512 bit/s operation given in the PCA5000T data sheet.

The nominal input data bit rate is determined by the crystal oscillator resonant frequency. The crystal oscillator frequency is always 64 times the input data bit rate. Therefore, for 1200 bits/s a 76.8 kHz crystal oscillator is required. No other external components of the Paging Decoder need to be changed. The new timing values frequency parameters can be calculated by appropriately scaling the corresponding values given in the data sheet. In this case, 1200 bit/s and a 76.8 kHz crystal oscillator frequency gives a scaling factor of $512/1200 = 0.427$ for the timing values. Since an external programming clock is used to program and verify the RAM memory, the programming timing values are not changed. Neither are the transition times changed from the specified values given in the data sheet.

For conversion from 512 bits/s to 1200 bit/s baud rate the following major changes must be observed by the designer:

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- the paging receiver establishment time is reduced to 13.3 ms, which has to be considered in the design of the receiver. This time is still sufficiently long for the UAA2033T and UAA2050T paging receivers
- the status change delay in the alert-only mode (the minimum time that a pushbutton has to be pressed to effect a change of status) is reduced from 1.5 s to 0.64 s; the status indication cadences are shortened as is the status alert period, which is now 26.7 ms
- in the display pager mode, the reference frequency output FL is 38.4 kHz, the data rate on the serial microcontroller interface increases from 512 bit/s to 1200 bit/s and the minimum data strobe pulse width is reduced to 26 μ s
- the call alert cadence time of 16 s at 512 bit/s is reduced to 6.8 s at 1200 bit/s; the call alert cadence period is reduced from 1 s to 0.427 s
- the frequency of the alerter drive outputs AL and QR increases from 2048 Hz to 4800 Hz
- the internal voltage converter is clocked at 2.3 times the rate; this may lead to increased switching noise on the voltage supply rails
- at the higher clock frequency of 76.8 kHz, the typical supply current increases to approximately 50 μ A
- the synchronization strategy timing is determined by both the baud rate and the batch structure so that the synchronisation algorithm is clocked faster.

From the differences and restrictions listed above it is most obvious that, besides using the PCA5000T at its original 512 bit/s data rate, a 1200 bit/s application in display pager mode is most attractive, since then, inconvenient changes in parameters can be corrected for by the microcontroller.

6. PCB LAYOUT CONSIDERATIONS

In general, the PCB layout for an application using the PCA5000T is not critical. However, in the design of a complete alert-only or display pager, the designer must

take into account that the Paging Decoder incorporates a crystal oscillator and digital clock signals which can generate harmonics. These harmonics can influence the input sensitivity of the paging receiver if the Paging Decoder is located too close to the paging receiver, especially near the antenna input circuitry.

7. DEMONSTRATION SYSTEM

A complete POCSAG paging demonstration system comprising a receiver module with UAA2033T digital paging receiver, a decoder module with the PCA5000T paging decoder and a POCSAG codegenerator and program unit has been developed by the Philips Components Application Laboratory Hamburg, see fig. 21. This demonstration system is described in a separate report, see chapter 6; OM4718.

A working alert-only pager can be made with the modules, the codegenerator in connection with an R.F. signal generator can be used to issue calls addressed to this pager.

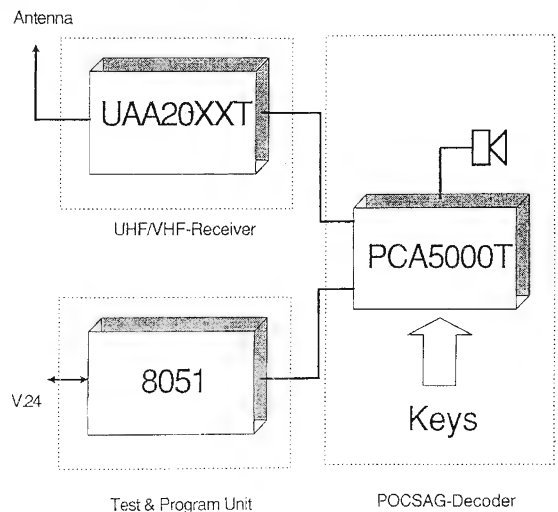


Fig. 21 POCSAG Paging Demonstration System, Overview of Modules

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8. PCA5000AT DECODER**8.1 Introduction**

The Philips POCSAG Decoder PCA5000T has been improved, leading to the type PCA5000AT. The PCA5000AT is fully compatible with the PCA5000T. The PCA5000AT mainly provides an improved synchronization behaviour. This note summarizes the improvements made. The application examples shown in the data sheet PCA5000T are also valid for the PCA5000AT.

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8.2 Description of the improvements in the PCA5000AT**8.2.1 Reset threshold voltage**

The reset threshold voltage has been reduced by 200 mV for the PCA5000AT. The nominal reset threshold voltage for the PCA5000AT is now - 1,4 V.

8.2.2 Switching transistor between VP and VS

The switching transistor between VP and VS, internal to the PCA5000T, has been omitted in the PCA5000AT. This transistor automatically short-circuits the VP and VS pin, if the PCA5000T is programmed for alert-only pager mode (SPF 01 = 0).

The PCA5000AT doesn't provide this facility any longer. If this connection is required, the VP and VS pin have to be short-circuited externally to the PCA5000AT. This will normally be necessary for alert-only applications.

Note:

If the PCA5000T is replaced by the PCA5000AT, please make sure that the VP pin is referenced correctly in your application. If you don't use any voltage converter or

voltage source to level shift the VP pin, VP has to be short-circuited with VS.

8.2.3 Improved re-synchronization behaviour in Carrier Off mode

The PCA5000AT is able to achieve fast synchronization while operating in Carrier Off mode without the need for preamble input. The PCA5000AT will synchronise to a POCSAG data stream within 17 batches in duration at the latest if a continuous data stream of at least 17 complete batches is being received.

8.2.4 Improved re-synchronization behaviour in Fade Recover,v mode

The PCA5000AT expands the synchronization test to 13 tests per batch (PCA5000T: 3 tests), while operating in Fade Recovery mode. The tests for synchronization codeword reception are performed around the predicted synchronization codeword position. The PCA5000AT will sample for synchronization codeword from -3 to +9bit around the predicted position, see fig. 22. The receiver enable duration is enlarged accordingly for the PCA5000AT.

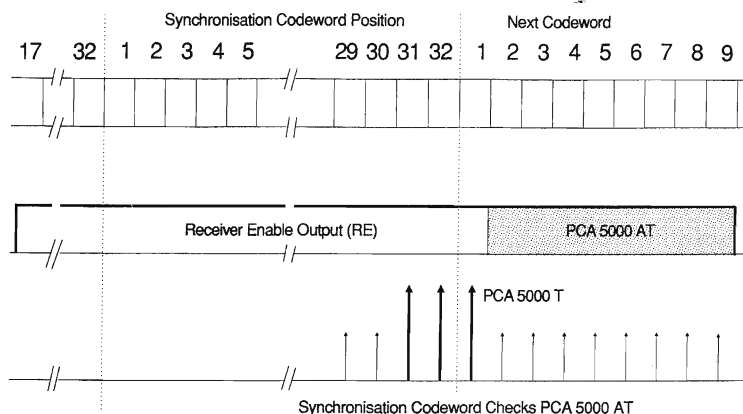


Fig. 22 Synchronization Codeword Scanning in Fade Recovery Mode PCA5000AT

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9. PROBILITY OF LOST CALL AT PCA5000T/AT

9.1 Introduction

The PCA5000T and PCA5000AT were originally designed to be powered from two batteries. Since more users are now applying a one battery concept, some precautions have to be taken to prevent lost calls, under certain "fresh-start-up" conditions.

The following paragraphs are discribing the phenomena caused by the failure and gives some recommendations to cope with it. Emphasis is put on display pager application. Operation of the new POCsAG decoder PCF5001T isn't affected and it may be used to replace the PCA5000T and PCA5000AT. However, please note that the PCF5001T is not pin compatible and provides an improved microcontroller interface.

9.2 Problem description

After a master reset condition the decoder may be found to sample for address codewords within the wrong frame, according to table 5.

programmed for	false scanning in
frame 0	frame 0
frame 1	frame 2
frame 2	frame 4
frame 3	frame 6
frame 4	frame 0
frame 5	frame 2
frame 6	frame 4
frame 7	frame 6

Consequently, the decoder doesn't respond to any address codeword transmitted in the frame it has been programmed for. Instead of it responds to an address codeword in the sampled frame, if it matches with the programmed address. Moreover, the receiver enable timing at the RE output will be found to be modified. Normally found to go low after frame scanning, the RE output now remains high, under special conditions, to go low later on. Call reception within the occupied frames. others than the false or programmed frame, hasn't been found to be possible. Figure 23 illustrates the receiver enable timing and the response to address codewords.

For example. programmed for frame 2 the decoder may sample frame 4, refer to the first and second batch in figure 23. The decoder maintains this operation, as long as it detects message codewords during frame scanning. Once it detects an address codeword of any type (local address, foreign address or idle codeword), it recovers to its normal operation. In other words, address word scanning occurs in the programmed frame and receiver enable timing is found to be correct, refer to the second and third batch in figure 23.

As mentioned, the phenomena occurs after a master reset condition only. A master reset condition is detected by the decoder, when the main power supply (VD VS) is removed form the device. This may take place, because of battery replacement, switch off operation for power consumption reasons or programming the device. However, it should be remarked that the frequency of occurrence for the phenomena also depend on process parameters, temperature and the power supply concept (exactly, the voltage step during power-up operation).

Table 5

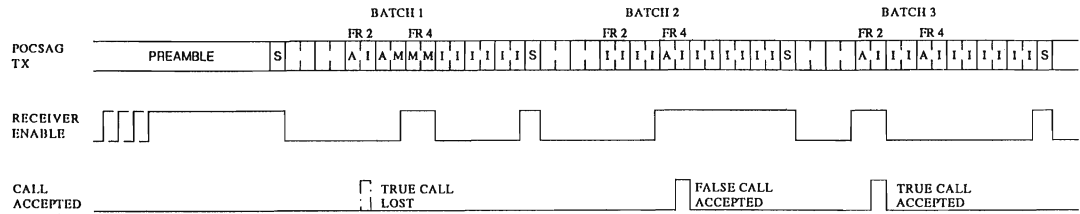


Figure 23 PCA5000 timing illustration during false scanning

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9.3 Problem solution by application

To overcome the problem, the application of the X1 input and the timing at the status inputs has to be modified. Goal is to provide a high level at the X1 input during master reset operation first. Secondly, to ensure proper decoder operation after master reset, the decoder status must be changed from OFF state to ON or SILENT state, while the crystal oscillator (X1/X2) is already running. Refer to figure 24 for an illustration. The second step may be delayed, as long as decoder operation isn't required. Tests made to prove the effectiveness didn't fail up to now.

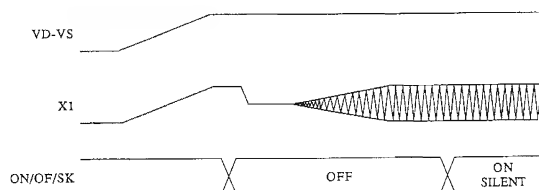


Figure 24 Illustration of the timing modification

Depending on the application of the decoder PCA5000T and PCA5000AT, the following application modifications can be used to overcome the failure. Emphasis is put on the display pager application.

9.3.1 Problem solution by hard- and software for display pager

As illustrated in figure 24, the X1 input has to be high during master reset operation. Four components connected externally to the crystal oscillator may be used to ensure this. refer to figure 25.

The circuitry is meant to detect the voltage slope during power-up, in order to force the X1 input high. Of course, the circuitry works the better, the larger and faster the voltage step is during power-up. The circuitry has been found to provide reliable operation, normally. After power-up operation, the microcontroller has to take care that the decoder is operating in OFF mode (ON input is low) and the status is changed to ON or SILENT, when decoder operation is required. If not applied already, this modification of the software is recommended.

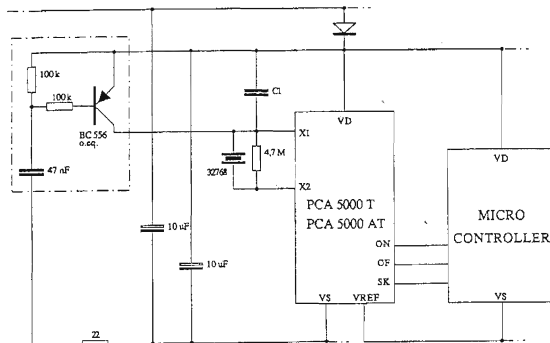


Figure 25 Principle modification of the display pager application

In the case the software can't be modified or the ON input is not controlled by the microcontroller, a RC delay circuit may be used to provide a similar function, refer to figure 26.

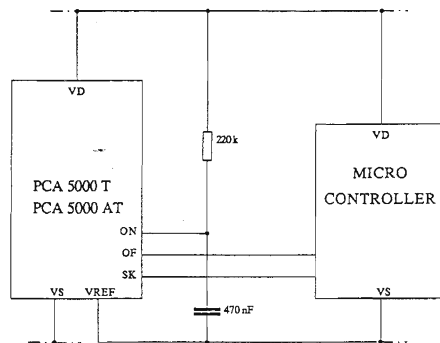


Figure 26 Maintaining decoder OFF mode after power-up by a RC delay circuit

9.3.2 Problem solution by software for display pager

To overcome the decoder failure without any additional components is possible for applications, which allow controlling of the X1 input by the microcontroller. For example any application, which omits the Lithium back-up battery and provides a re-programming of the decoder device every time after power-up, is suited. Under this

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circumstances it should be easy to modify the software according to the requirements given in figure 24.

A different method may be used, if the microcontroller provides any kind of reset signal during power-up. This signal may be used to force the X1 input high, for the desired time, by means of an additional diode (a schottky type is recommended). refer to figure 27 for the modification principle.

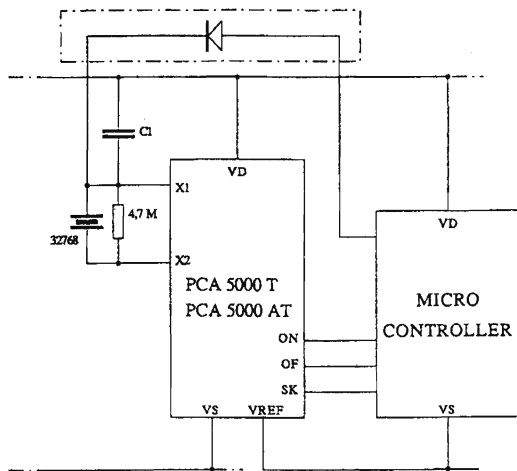


Figure 27 Using a microcontroller 'reset' signal to overdrive X1 input

9.4 Decoder problem and system specification

Because the decoder failure occurs after a master reset condition only, one may decide to run without any application modification. This is reasonable, if a master reset condition occurs very seldom. For example a pager, which maintains the power supply to the decoder PCA5000T or PCA5000AT all the time, may encounter a decoder failure after battery replacement only. Obviously, this is meant to happen very seldom.

Talking of off-site paging systems, comprising a large number of subscriber normally, one should remember that it is very unlikely that a call for the pager is transmitted within the false scanning batch. In other words, a lot of different calls are send, sometimes even

with call repetitions and several batches are transmitted normally, so it is very likely that the decoder recovers from the failure before it is paged. To run without any application modification may be reasonable, even if the pager is switched from off to on once per day and thereby encounters its functional failure for the very first batch.

Serious problems are expected for on-site paging systems, comprising a very small number of subscriber normally. However, even under these circumstances one can run without an application modification, if he has influence on the subscriber address allocation and allocates all subscriber within the system in frame 0. Consequently, false scanning occurs in frame 0 and therefore doesn't matter, refer to table 5. Moreover, allocation of all subscriber within framed saves transmitter time and thereby transmitter power consumption normally, if transmission is suspended after frame 0.

10. REFERENCES

- /1/ CCIR Recommendation 584: Standard Codes and Formats for International Radiopaging
- /2/ "The book of the CCIR Radiopaging Code No.1" issued by British Telecom, Radiopaging Code Standards Group (1986)
- /3/ PCA5000T Paging Decoder
Philips Data Book IC03, 1993
- /4/ UAA2050T Low Power UHF Digital Paging Receiver
Philips Data Book IC03, 1993
- /5/ Richard Blahut Theory and Practice of Error Control Codes Addison-Wesley, 1984

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PCF5001T versatile POCSAG decoder applications

Abstract

The PCF5001T is a very low power POCSAG decoder and pager controller specifically designed for use in radio pagers. It supports data rates of 512 bps and 1200 bps and uses advanced EEPROM technology to store four user addresses (RICs) on chip. Used in conjunction with the UAA2033T or UAA2050T paging receiver circuits the PCF5001T offers an attractive, miniature solution for alert-only and display pager applications.

This report describes PCF5001T circuit operation, its features and gives some application examples.

generated by direct driving of a bleeper device. In display pager configuration the decoder operates in combination with a microcontroller that performs display data processing and user interface handling. Received call information is passed to the microcontroller by using the serial microcontroller interface.

This report first describes decoder operation in general and focuses on configuration specific properties of the PCF5001T in the following sections. Application examples conclude these sections. A demonstration system board using the PCF5001T is available for evaluation by the customers.

1. Summary

The PCF5001T paging decoder has been designed to decode POCSAG coded data and to organize and control pager operation for wide-area and on-site paging systems. It decodes the POCSAG data received from the paging receiver circuit at data rates of 512 bps and 1200 bps. The decoder synchronizes a bit clock to the input data stream, performs batch synchronization, detects transmission errors and corrects received code words and performs address scanning to provide alert cadences, optical and mechanical indication and formatted message information upon call reception. The internal EEPROM not only holds four programmable user addresses (RICs) but is also used to define the application environment and to select specific options. The EEPROM does not require any backup supply voltage. To maximize battery economy the receiver circuit is only switched on when data is actually needed depending on the state of the synchronization algorithm. Other features of the PCF5001T include low-level alert and status indication, out-of-range indication, duplicate call suppression and an internal voltage doubler to operate an external microcontroller and display devices at doubled supply voltage.

The PCF5001T is designed to operate in two different configurations: The alert-only pager configuration requires just the receiver and the decoder circuits. In this case the complete user interface functions are already implemented in the decoder. This includes a three position slider switch interface for operating mode selection and a silent call storage. Alert cadences are

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2. Introduction

The PCF5001T is a very low power POCSAG decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCF5001T and its programmability allow for flexible application in alert-only as well as in display pagers.

The PCF5001T decodes the CCIR radio paging code No.1 (POCSAG Code) at data rates of 512 bit/s and 1200 bit/s. Used in conjunction with the Philips UAA2033T (VHF) or UAA2050T (UHF) low power digital paging receivers the PCF5001T offers an attractive miniature solution for alert-only and display pager applications.

The PCF5001T employs advanced EEPROM technology to hold four receiver identification codes (RICs) and 32 special programmed function bits (SPF01 - SPF32). The EEPROM technology eliminates the need for any external backup battery or additional storage devices.

Upon detection of either of the four stored receiver identity codes the PCF5001T generates output signals suitable for driving a magnetic or piezoceramic bleeped, an L.E.D indicator and optionally also a vibrator type motor device. The decoder provides eight different alert cadences, which allow for easy call identification by the user for each of the four RICs.

In the basic alert-only pager mode no external microcontroller is required. The decoder is designed to monitor a three position slider switch, which is used to select the operating state. The three operating states are On, Off and Silent. The Silent state is used to suspend alert cadence generation and to keep them in the silent call storage until the decoder is switched to On state again whereupon the stored calls are alerted again.

In display pager mode, received calls and messages are transferred to an external microcontroller via the ICs serial communication interface. The PCF5001T supplies formatted identity and message information together with error correction status and duplicate call suppression time out information. A built-in voltage converter can supply doubled supply voltage to the microcontroller and other additional circuits like LCD drivers, the interface signals are level shifted accordingly.

The PCF5001T is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

3. List of Features

The following is a list of features that are supported by the new decoder and pager controller circuit PCF5001T. Some of them are optional and described in more detail in later sections.

- wide operating supply voltage range (1.5 V to 6 V)
- extended temperature range
- very low supply current (60 μ A typ. with 76.8 kHz crystal, 25 μ A typ. with 32 kHz crystal)
- decodes CCIR Radiopaging Code No.1 (POCSAG Code)
- programmable call termination conditions
- full support for 512 and 1200 bit/s data rates, other data rates up to 2400 bit/s possible
- improved ACCESS synchronization algorithm
- supports four RICs in two independent frames
- on-chip non-volatile EEPROM storage
- eight different call alert cadences
- directly drives magnetic or piezoceramic bleeper
- high level alert requires only a single external transistor
- optional vibrator type alerting
- optional visual call data indication
- alert on low battery
- out-of-range indication with programmable hold-off
- provides silent call storage, up to eight different calls

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- repeat alarm facility
- programmable duplicate call suppression
- interfaces directly to UAA2033T / UAA2050T digital paging receivers
- programmable receiver power control for battery economy
- serial microcontroller interface for display pager applications
- on-chip voltage converter with high drive capability
- level shifted microcontroller interface signals
- integrated user interface functions
- contained in a 28-lead mini-pack (S0-28).

The typical applications of the decoder include alert-only and message pagers, telemetry and data receivers.

4. Paging Decoder Operation

The PCF5001T supports alert-only and display pager applications. The decoder has to be programmed for the specific application by means of the special programmed function bits (SPF-bits). This section describes the features and operation of the PCF5001T, which are common to both alert-only and display pager modes. Information relevant to one specific pager mode only is provided in sections 5 and 6.

A simplified block diagram of the PCF5001T POCSAG decoder and pager controller is shown in fig. 1.

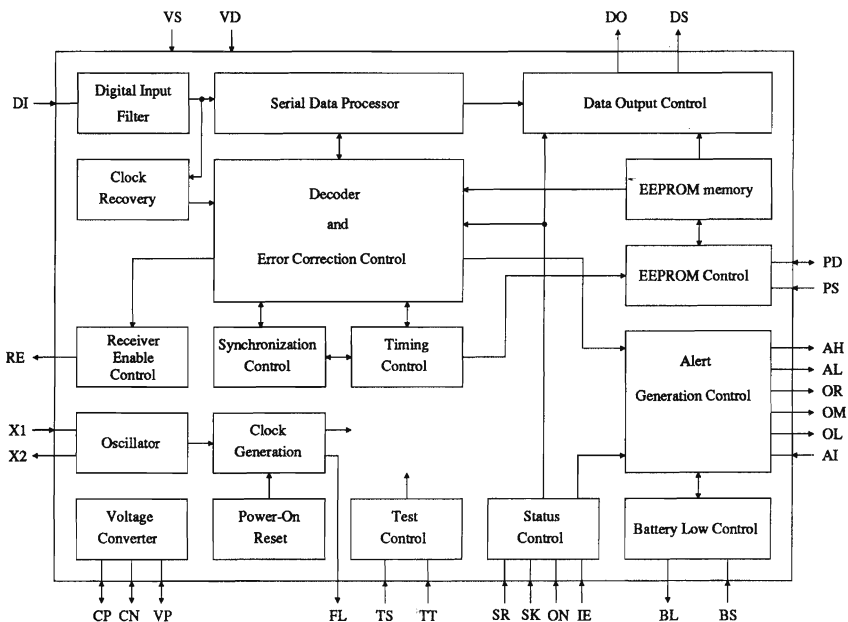


Fig.1 Blockdiagram of the PCF5001T decoder chip

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4.1 Decoder Status

The PCF5001T has three internal states: On, Off and Silent. A specific state is selected by slider switch operation in alert-only mode or by writing the appropriate status signals to the decoder in the display mode.

In the Off state the decoder keeps the paging receiver IC disabled and no data is processed. However, crystal oscillator operation is maintained to ensure that a status change can be detected and that status interrogation is possible. The decoder shall be put into Off state for either EEPROM write or verify operation.

The On state is the normal operating state of the paging decoder. The PCF5001T controls the receiver enable output to switch the receiver circuit on when data is needed. Received data is subsequently processed by the decoder. When a valid paging call is detected, the PCF5001T generates the appropriate user alert output signals.

The decoder Silent state lets the decoder operate as in On state except that incoming calls do not cause immediate call alert cadence generation. Instead, if programmed as alert-only pager, the decoder holds incoming calls in the silent call storage and generates the respective alert cadences after the decoder has been set to On state again. However, special silent override calls will cause generation of alert cadences, if enabled.

4.2 Data Reception

4.2.1 Data Input

The data input is fully asynchronous. The input data rate is directly related to the crystal oscillator frequency. The PCF5001T was designed to support two basic data rates: 512 bit/s and 1200 bit/s, but other data rates are also possible.

The PCF5001T expects the input data to have positive logic polarity. A logic "1" corresponds to a HIGH level voltage input and a logic "0" corresponds to a LOW level voltage input. The input data may contain jitter and spikes. Therefore, the data coming from the receiver is first passed through a digital noise filter. The digital noise

filter samples the input data at eight times the data rate. The filtered input data is fed to the main serial data processor and is also used to serve as a reference for the bit clock recovery circuit.

4.2.2 Bit Clock Recovery

From the filtered data input a sampling clock is derived. The bit clock is synchronized to the input data and has a nominal frequency equal to the input data rate, i.e. 512 Hz or 1200 Hz, respectively.

The bit clock is synchronized to the data such that it tries to sample each data bit at the centre of the bit period. The clock recovery circuit evaluates logic transitions in the data and adds or omits internal clock cycles to shift the sampling instant in fractions of the bit period. There is always only one shift per bit period possible. The clock recovery circuits supports fine and coarse resolution for bit clock synchronization. The resolution of the sampling instant shifts is

- 1/8 of a bit period (coarse) in Carrier-Off and Power-up state, and
- 1/32 of a bit period (fine) in Preamble-Receive, Data-Receive, Data-Fail and Fade-Recovery state.

The internal sampling clock is based on the crystal oscillator reference. The bit clock recovery algorithm also compensates for absolute errors, ageing and temperature drift effects of the crystal oscillator frequency within a wide range and is also effective if an external clock source is used.

4.2.3 Data Input Format (POCSAG Code)

The incoming data stream is processed by the PCF5001T according to the standards of the CCIR Radio Paging Code No.1 (POCSAG Code). The code format is independent of the data rate. Standard POCSAG based paging networks use 512 bit/s or 1200 bit/s data rates.

The transmission is coded according to the following rules, see fig. 2. The transmission is started by sending a preamble, which is a sequence of at least 576 continually alternating bits (10101010...). The preamble is provided for easy bit clock recovery in the decoder. The preamble

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precedes a number of batch blocks. There are as many batches transmitted as required by the amount of messages to be transmitted or as determined by the network operator. The transmission is terminated after the last batch.

Each batch comprises a synchronization code word with a fixed 32 bit pattern and eight frames that are numbered 0 to 7. The synchronization code word marks the beginning of a batch and is normally used to obtain word synchronization.

A frame consists of two 32 bit code words. These code words can be either an address code word or a message code word or an idle code word. Idle code words are used to fill empty batches when there are no more messages or to separate calls.

The address code word selects a specific pager out of the total pager population. An address code word is coded as shown in fig. 2. 18 bits of the 21 bit digital user

address (Receiver Identification Code, RIC) are coded in the code word itself (bits 2 to 19), which is protected against transmission errors by a number of check bits (bits 22 to 31). The remaining three bits of the RIC are coded in the frame number, in which the address code word is transmitted. The check bits are calculated using the (31,21) BCH code (Bose-Chaudhuri-Hocquenghem Cyclic Code). Bit 32 is a parity bit to establish even parity for the address code word. The check bits introduced in the code word can be used to increase the call success rate by error detection and correction in the paging decoder (Forward Error Correction).

Message code words contain the information to be displayed when numeric or alphanumeric calls are transmitted. The message code words are transmitted directly following the address code word. Messages, which are too long to fit into one code word, continue in the code word positions of subsequent frames and batches until the complete message has been transmitted. However, the synchronization code word is

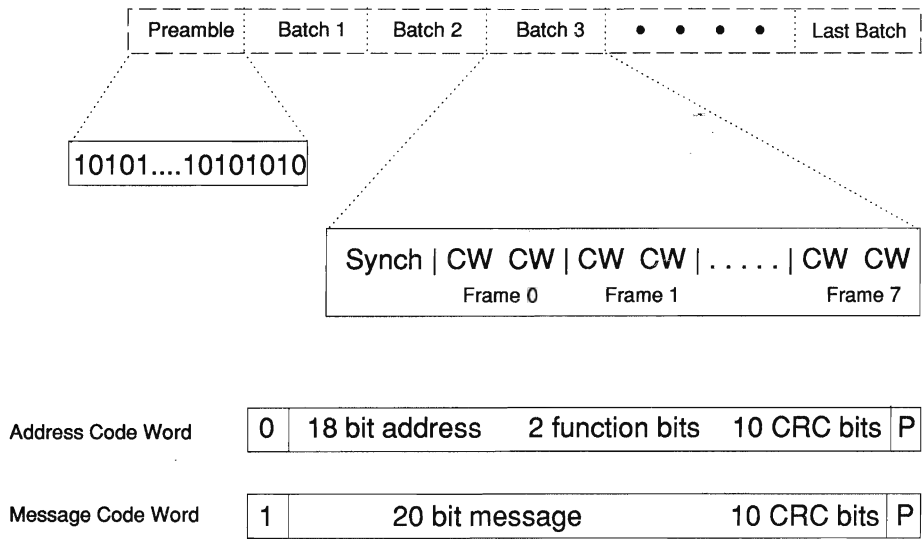


Fig.2 Structure of the POCSAG Code

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still maintained at the beginning of each batch. Bits 2 to 21 contain the information to be displayed, see fig. 2. Numeric messages are coded as nibbles of 4 bit, alphanumeric messages use a 7 bit ASCII code to carry the information. Message code words use the same error correcting code as address code words.

4.2.4 Synchronization Strategy

Synchronization to the POCSAG code structure is achieved in the PCF5001T by using the improved Philips ACCESS algorithm. The algorithm employs a state machine with six internal states. The state machine is active only in On and Silent state of the decoder. Prior to call data processing, the decoder has first to achieve bit synchronization and then word synchronization.

Power-on State: This state is entered by switching the decoder from Off to On or Silent state. Following the start-up alert period the PCF5001T keeps the paging receiver enabled for a period of up to 3 batches in duration. The decoder tests incoming data for preamble and synchronization code word pattern. If a preamble is detected the algorithm enters the preamble receive state. If a synchronization code word is found the algorithm enters the data receive state. If neither is detected within the three batch interval, the algorithm enters the carrier-off state.

Preamble Receive State: The decoder keeps the paging receiver enabled for the duration of preamble input. The PCF5001T checks received data bit-by-bit for preamble and synchronization pattern. Preamble detection causes the decoder to remain in the preamble receive state, while synchronization code word detection causes the decoder to enter the data receive state. Failure to detect preamble for a period equal to one batch in duration results in switching to the carrier-off state.

Data Receive State: This is the normal synchronized state of the decoder, in which the PCF5001T can detect and receive cells. In every incoming batch, the decoder scans the synchronization code word position and the code words in the programmed frames. The code words received in the frame position are processed as described in section 4.2.5.1.

The PCF5001T maintains the data receive state until it

fails to recognize the synchronization code word at the beginning of a batch, whereupon the algorithm switches to the data fail state. The test for synchronization code word is performed on the 32 bits received at exactly the expected synchronization code word position.

Data Fail State: In the data fail state the PCF5001T continues data reception as if in data receive state for the duration of a single batch including the next synchronization code word position. Call reception and processing is performed as in data receive state except that the conditions for call termination are modified.

At the expected synchronization code word position a test for synchronization code word and preamble is carried out. If preamble pattern is detected, the algorithm switches to the preamble receive state. If synchronization code word is recognised, the state machine goes back to the data receive state. If neither preamble nor synchronization code word pattern is found, the algorithm selects the fade recovery state and stops call data processing.

Fade Recovery State: In this state the decoder tries to compensate a small bit shift, which may happen due to noisy input signals or fading radio signals. This is achieved by testing not only the 32 bits at exactly the synchronization code word position for preamble and synchronization code word pattern. Instead, the decoder performs these tests bit-by-bit starting eight bits earlier and finishing eight bits later than the expected code word position (17 tests in total). This is equivalent to a sampling window with an eight bit margin on both sides of the original code word position.

Preamble detection causes switching to the preamble receive state, detection of synchronization code word results in change to the data receive state. The PCF5001T remains in this mode for 15 batches. After time out of 15 batches the algorithm switches to the carrier-off state.

Carrier-Off State: This is the power saving state, in which the decoder monitors the data from the receiver to detect a valid data stream. In the carrier-off state, the PCF5001T scans the received data taking a 32 bit block of data every 18 code words. As each new bit is received, the algorithm checks for preamble and synchronization

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code word pattern on the most recently received 32 bits. These 32 most recently received bits consist of n bits taken from the current block of data and $(32 - n)$ bits taken from the previous block. Therefore the algorithm shifts a 32 bit sampling window over every bit position of a batch within the time of 17 batches. Tests are carried out for preamble and synchronization code word pattern. Detection of preamble causes selection of the preamble receive state, the data receive state is entered upon detection of the synchronization code word.

Using this technique, resynchronization is obtained within a continuous data stream of at least 18 batches without preamble transmission.

4.2.5 Call Reception

4.2.5.1 Address Scanning and Detection

The PCF5001T supports four user addresses RIC A, B, C and D. RIC A and B reside in the frame defined by frame bits FR10-12 while RIC C and D reside in the frame defined by frame bits FR20-22. Call data processing is performed while the decoder is in data receive or data fail state, see section 4.2.4. Address scanning comprises the input of the two code words within either of the two programmed address frames defined by the respective frame bits. Each of the received code words is error-corrected. If the result is a valid address code word, then bits 2 to 19 of the code word are compared with each of the four sets of address bits stored in the decoder EEPROM. A call is successfully detected, if

- all 18 bits of one set match with the received address bits, and
- this set is enabled, and
- the programmed frame number of this set matches with the actual frame number.

Upon successful call detection, the decoder performs the following actions:

- Set a store for call alert cadence generation according to the combination of the function bits in the accepted address code word. The call alert cadence will not be generated before the call has been terminated and

data output has been completed.

- Keep the receiver enable output (RE) active and receive possibly subsequent message code words, until any of the call termination criteria is fulfilled, see section 4.2.5.2.
- Trigger the serial message transfer on the serial microcontroller interface by generating a start condition and sending an address word. Message code words, as attached to the address code word, are deformed and transferred via the microcontroller interface to an external microcontroller.

4.2.5.2 Call Termination

The PCF5001T is capable of handling message calls. The message code words of a message call directly follow the address code word and occupy code word positions in subsequent frames and batches. However, processing of synchronization code words at the beginning of each batch is maintained.

Upon a successful call detection, the decoder keeps the paging receiver enabled to receive subsequent codewords until one of the following call termination criteria is fulfilled. The PCF5001T supports three different methods of call termination with respect to call termination following reception of uncorrectable code words. The method is selected by appropriate setting of SPF bits, see section 4.10.2.

a) Method 1:

The call is terminated, if

- any valid address code word (including Idle) is received, or
- error correction is unable to correct the last received code word, or
- synchronization code word could not be detected at the beginning of the batch in data fail state.

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b) Method 2:

The call is terminated, if

- any valid address code word (including Idle) is received, or
- error correction is unable to correct the two lost received code words, or
- synchronization code word could not be detected at the beginning of the batch in data fail state.

c) Method 3 (Combination Method):

The call is terminated, if

- any valid address code word (including Idle) is received, or
- error correction is unable to correct the two last received code words, or
- error correction is unable to correct the code word directly following the starting address code word, or
- synchronization code word could not be detected at the beginning of the batch in data fail state.

Call termination is indicated by sending a termination word via the serial microcontroller interface and by generating a stop condition.

4.2.6 Error Correction Algorithms

As was explained in section 4.2.3, the POCSAG address and message code words contain redundant bits, which can be used to increase the call success rate by applying error correction techniques to the received code words. Preamble and synchronization code word patterns may be recognized by using correlation techniques. The PCF5001T was designed to handle the following errors, depending on the type of the code word:

- a) Preamble: A four bit random error correction is performed when inputting preamble.

- b) Synchronization Code Word: Up to two errors randomly distributed within the 32 bit synchronization code word can be corrected by the decoder.

- c) Address Code Words: A 4 bit burst error correction algorithm is applied to received address code words.

- d) Message Code Words: A single bit error can be corrected in received message code words.

The error correction capabilities of the PCF5001T decoder circuit have been optimized to give a high call success rate while keeping the false call rate low. The false call rate is related to calls that are received but which were not originally addressed to this pager. This is a general problem of forward error correction methods.

4.2.7 Paging Receiver Power Control

The bipolar paging receiver circuit consumes the most power in a pager. Therefore, the paging receiver IC has to be switched off as often as possible to maximize battery economy, see fig. 3.

4.2.7.1 Receiver Establishment Time Selection

The receiver power control algorithm activates the RF receiver circuit only when data is actually needed by the decoder. This information is taken from the synchronization state machine and the internal timing unit. Normally, a receiver circuit will require some time to settle and stabilize before it can produce valid data output. This is taken into account in the PCF5001T by activating the receiver power control output the receiver establishment time earlier before the actual data input takes place.

The receiver establishment time is programmable to allow for adaptation to the specific receiver circuit design requirements. Depending on the data rate in use, the receiver establishment time can vary between 4 and 32 bit in duration with 512 bits operation and between 8 and 64 bit in duration with 1200 bit/s operation, see section 4.10.2.

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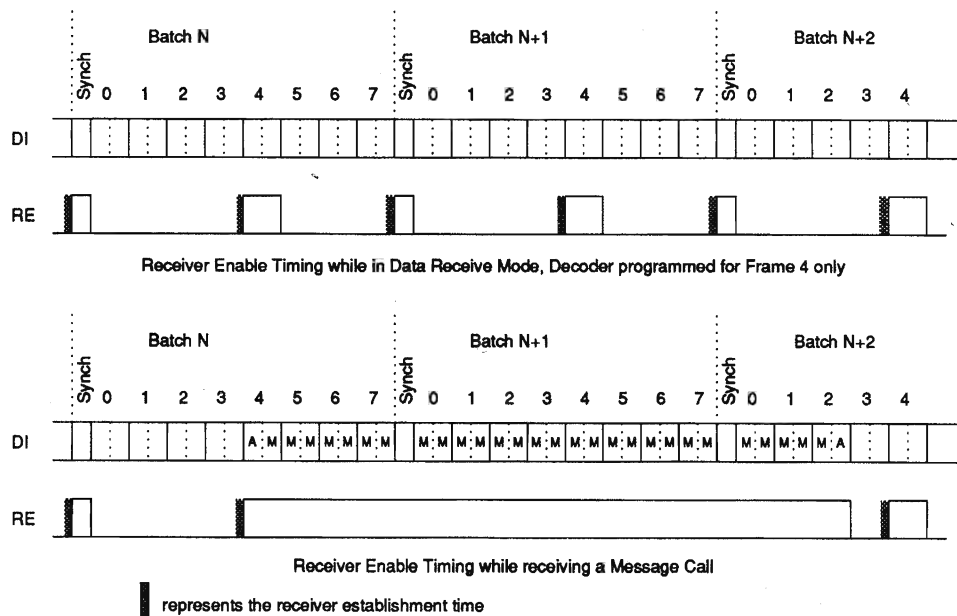


Fig. 3 Receiver power control in data receive state

4.2.7.2 Duty Cycle Computation

The algorithm used to control the receiver power control output is driven by the synchronization state machine and the internal timing unit. Therefore, the duty cycle must be calculated separately for every state of the synchronization state machine.

The resulting duty cycle figures are as follows.

- **Power-On State:** the paging receiver is always enabled
- **Preamble Receive State:** the paging receiver is always enabled
- **Data Receive State:** the paging receiver is enabled for the synchronization code word and for the frames defined by the programmed RICs. The resulting duty cycle depends on the programmed frame numbers.

$d = (96 + t_{RX}) / 544$,
for single frame programmed for 0 or 7
 $d = (96 + 2 t_{RX}) / 544$,
for single frame not programmed for 0 or 7
 $d = (160 + t_{RX}) / 544$,
for two frames concatenated to the synchronization code word position
 $d = (160 + 2 t_{RX}) / 544$,
for two frames, where either one frame is concatenated to the synchronization code word or the two frames are concatenated $d = (160 + 3 t_{RX}) / 544$,
for two frames, which are not concatenated to either themselves or the synchronization code word position
 Parameter t_{RX} is the receiver establishment time, see section 4.10.2.

- **Data Fail State:** as data receive state
- **Fade Recovery State:** the paging receiver is enabled only for the synchronization code word position enlarged by eight bit on both sides. This results in a

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duty cycle of

$$d = (48 + t_{RX}) / 544.$$

Parameter t_{RX} is the receiver establishment time taken in bit see section 4.10.2.

- Carrier-Off State: the paging receiver is enabled for the duration of one code word (32 bit) every 18 code words. The resulting duty cycle is $d = (32 + t_{RX}) / 544$.
Parameter t_{RX} is the receiver establishment time, see section 4.10.2.

The average paging receiver duty cycle is determined by the radio channel conditions and the signal strength since the decoder may switch between states as the data bit error rate varies. The average receiver duty cycle depends also on paging network parameters such as paging timeslot duration, preamble duration and transmitter cycle time.

4.3 Crystal Oscillator

A crystal oscillator circuit generates all the internal and external timing and drive signals. The PCF5001T was designed to basically operate with 76.800 kHz and 32.768 kHz crystal frequencies. A data rate of 1200 bit/s is possible with a 76.8 kHz crystal only, see section 4.10.2. A data rate of 2400 bit/s is possible if an external clock generator of 156.6 kHz is connected to X1 input. In this case the minimum supply voltage is restricted to 1.8 V.

The crystal oscillator frequency is a fixed multiple of the data bit rate of the incoming POCSAG data. This can be used to adapt the decoder to non-standard data rates. Crystal frequency deviations in excess of + 100 ppm are compensated for by the bit clock recovery circuit described in section 4.2.2. However, it is recommended to use crystals with no more than + 50 ppm tolerance to obtain best decoding results.

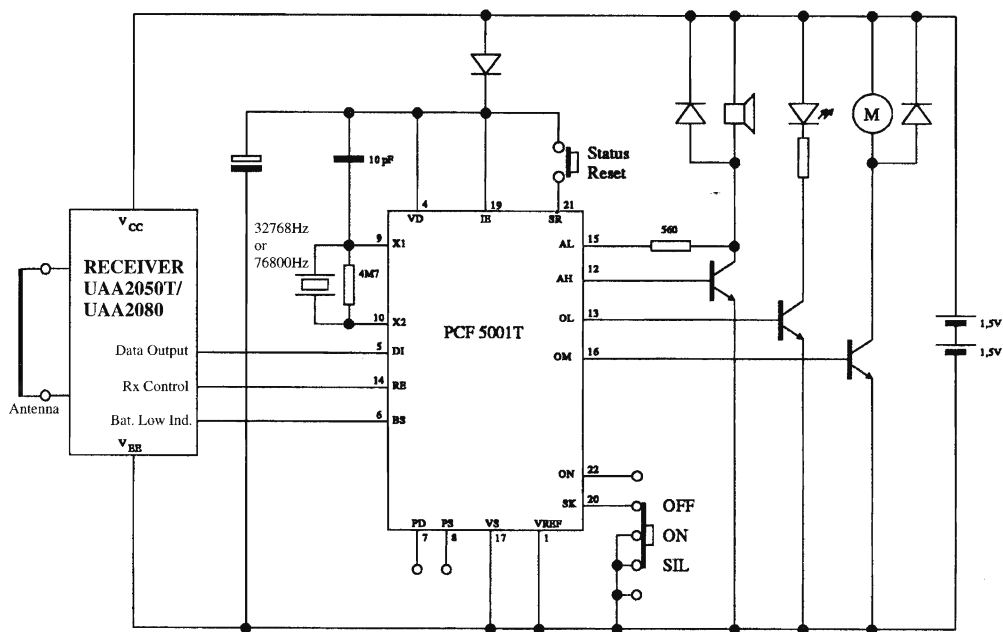
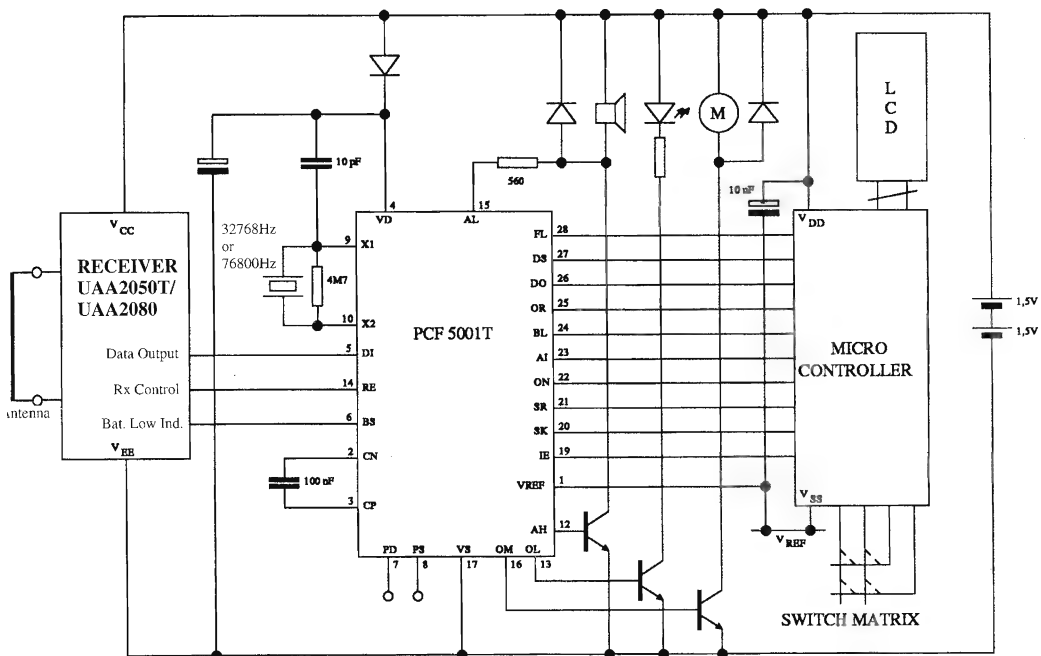


Fig. 4 Alert-only pager application circuit diagram

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AL, so that if AL is at logic LOW then AH is at logic HIGH, and vice versa.

4.4.1 Alert Cadence Generation

The PCF5001T decoder generates call alert cadences by sending a pulse modulated squarewave signal to the alerter. The shape of the alert cadence (modulation pattern) is determined by the two function code bits of the address code word (bit 20 and 21, see fig. 2) and the respective RIC, refer to fig. 6. Calls received under RIC A and C are alerted using the normal alert cadence while calls received under RIC B and D result in a warbled alert cadence.

During the first four seconds low intense alert cadences are generated by driving the AL output only. For the following 12 seconds the AH output is also driven to increase the alert intensity to high level. Call alert cadences are automatically terminated after 16 seconds.

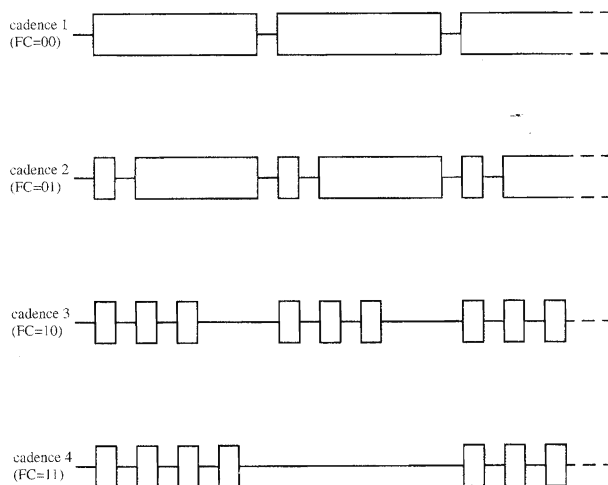
The alert cadences are generated after one of the call termination criteria has been fulfilled. However, alert cadence generation will not commence before the completion of a delay of about 52 ms after the termination word has been sent via the serial microcontroller interface. This delay may be used by the microcontroller to cancel alert cadence generation.

4.4.2 Status Indication

The decoder PCF5001T generates status indication tones as a result of user status interrogation. The status indication tones are generated at low intensity, only output AL is driven. The corresponding modulation patterns are shown in fig. 7.

4.4.3 Repeat Alert Indication

The decoder generates a repeat alert cadence for calls that have not been terminated by the user, if enabled by programming of the associated SPF bit. The repeat alert cadence is generated at high intensity.



Note: Cadences for calls received under RIC B or D have additional warble modulation

Fig. 6 Alert cadences of the PCF5001T

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4.4.4 Battery- Low Indication

A continuous high intensity battery low alert tone is generated whenever the battery low condition is detected by the battery low detection logic. Battery low alert is not repeated, see also section 6.8. The battery low alert tone is automatically terminated after a time out of 16 seconds.

4.4.5 Alarm Input

A logic HIGH level on input AI (pin 23) of the decoder with interface enable input IE active causes generation of a continuous high intensity alert tone on outputs AL and AH. Pulsing the input signal may be used to modulate the alert tone and to create proprietary alert cadences.

4.5 Vibrator Interface

The PCF5001T can drive a vibratortype motor using a bipolar transistor when the vibrator function is enabled by programming the appropriate SPF bit, see fig.4 and 5. The vibrator output OM, pin 16, is activated when the decoder is in Silent state and calls are received. In this case output OM switches to a static logic HIGH

output for the duration of the normal alert cadence (16 seconds) or until terminated by the user.

Silent override calls are not alerted by the vibrator. The vibrator output is inactive while operating in On state.

4.6 L.E.D Interface

An LED indicator is used to provide quiet alert for call alert, repeat alert, out-of-range indication, alarm output, call data output (optional, see section 4.11) and start-up alert. Output OL, pin 13, can drive the base of an external bipolar transistor, which in turn switches the LED, see fig. 4 and 5. Output OL is set to a logic HIGH, whenever the LED shall be activated. In general, the OL output is modulated with the same cadence pattern as the acoustical alert outputs AL and AH. However, output OL does not have the alerter frequency squarewave component.

4.6.1 Alert Cadence Indication

The PCF5001T provides for call alert indication in both the ON and Silent states of the decoder. The LED reflects the same alert cadence modulation as the alerter outputs AL and AH, see fig. 6. Warbled cadences cause the LED output to be "warbled" as well. LED indication may be terminated by the user or by time out after 16 seconds.

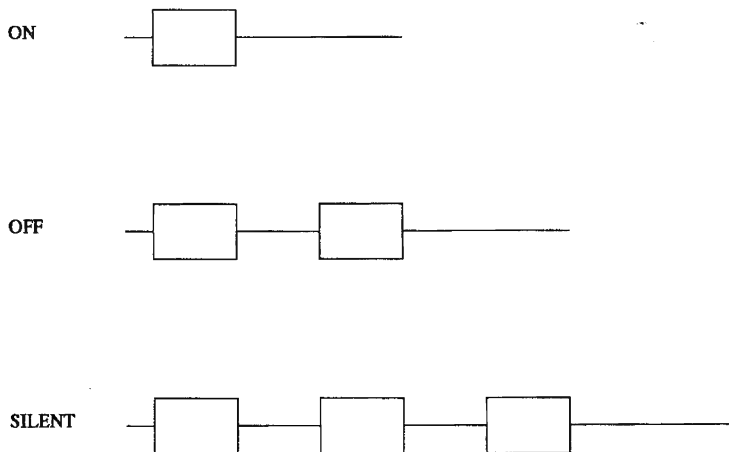


Fig. 7 Status indication toners

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4.6.2 Repeat Alert Indication

When the repeat alert function is enabled, the LED output generates the repeat alert cadence together with the audible alert in On state. In Silent state, the some LED indication is used to indicate the presence of calls stored in the silent call storage, but without acoustical alert.

4.6.3 Out-of-Range Indication

In alert-only pager mode, when the out-of-range function is enabled by programming the associated SPF bit, the decoder provides an out-of-range signal on the LED output OL in On and Silent state.

The out-of-range condition is derived from the synchronization state machine. Upon entry into fade recovery state following data fail state or upon entry into carrier-off state directly from power-on state, a hold-off timer is started. The hold-off time is programmable via SPF bits 6 and 7. After time out of this hold-off time the out-of-range indication is generated by activating the LED output for 62.5 ms every 2 seconds. This results in a small duty cycle of only 1/32.

The out-of-range condition is reset upon re-entry to the data receive state or by changing status to Off.

4.6.4 Alarm Input

Whenever the alarm input, pin 23, is set to logic HIGH level while the interface enable input is active, the LED output is activated and the LED switched on.

4.7 Start-up Alert

The decoder PCF5001T provides a start-up alert feature to allow for functional tests of the alerter, the LED and the vibrator. The start-up alert is generated by changing status from Off to On or Silent. The start-up alert takes the form of a continuous signal, 8 code words in duration for 512 bit/s configuration and 17 code words in duration for 1200 bit/s systems, this will take 500 msec respectively 453 msec.

When changing status from Off to On, start-up alert is generated on the alerter at low intensity and on the LED. Change of status from Off to Silent causes start-up alert generation on LED and vibrator output, irrespective of vibrator enable (SPF 11=1)

Upon completion of the start-up alert the synchronization state machine enters the power-on state and initiates the synchronization process. It's not possible to abbreviate the start-up alert. Receive operation and battery level low indication commences only upon completion of the start-up alert indication.

4.8 Battery Control Logic

The PCF5001T operates from a single supply voltage in the range from 1.5 V to 6 V. For 2400 bit/s data rate using an external clock source or when operation of the decoder in the temperature range between -40 °C and -10 °C is intended, however, the minimum supply voltage is restricted to 1.8 V.

The PCF5001T includes a built-in battery low level control logic, which monitors the condition of the battery. A logic signal representing the actual condition of the battery must be supplied to the battery low-level input BS, pin 6. A logic LOW level represents a good battery condition whereas a logic HIGH level indicates a poor battery condition, i.e. the battery needs to be replaced. The Philips UAA2033T/UAA2050T/UAA2080T integrated VHF/UHF digital paging receivers contain internal battery low level detectors which provide an output signal to drive the BS input of the decoder directly.

Sampling of the battery sense input BS occurs in On and Silent state. The PCF5001T samples the BS input

- on the 32nd bit of synchronization code word input when operating in data receive, data fail, fade recovery or carrier-off state,
- on every bit during power-on state.

A battery low condition is detected and the battery low latch set, if four consecutive samples are found to be logic HIGH. If the decoder operates in On state, the battery low alert is generated immediately. If the decoder is operated in Silent state, the battery low alert is inhibited until the decoder has been switched to On state again. If the repeat alarm function is active or an incoming call is alerted, battery low alert will be suspended until the respective cadence has been completed.

The battery low latch is reset by switching the decoder to Off state.

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4.9 Summary of Alert Generation Conditions and Priorities

This section summarizes the different output signals available and the conditions under which they are generated. Entries shown are available, if the decoder operates in On state. Entries shown in brackets are not available, if the decoder operates in Silent state. Some of the alert functions must be explicitly enabled by programming of the related SPF bit.

Alert function Output active	AL	AH	OL	OM	OR	BL
Start-up	(yes)	-	yes	yes	-	-
Status ind.	yes	-	-	-	-	-
Call reception	(yes)	(yes)	yes	SPF11	-	-
Repeat mode	(SPF16)	(SPF16)	SPF16	-	-	-
Out of range	-	-	SPF15	-	yes	-
Battery low	(yes)	(yes)	-	-	-	yes
Alarm input	(yes)	(yes)	yes	-	-	-

Note to the table:

Reception of special silent override calls causes the decoder to generate call alert indication via AL and AH even if it operates in Silent state.

If there are requests for more than one alert operation at the same time, the decoder resolves these simultaneous requests based on the following rules.

- If more than one call alert cadence has to be generated, the cadences are generated in order of the silent call storage number (see section 5.2.1) regardless of order of receipt.
- Call alert cadence generation overrides generation of battery low alert generation.
- Status indication is completed before starting either call alert cadence generation or battery low alert.
- The alarm input function (pin 23) overrides generation of any internal alert cadence.

4.10 Programming

The PCF5001T decoder uses on-chip electrically eraseable, programmable non-volatile memory (EEPROM) to store up to four possible user address codes, two frame numbers and 32 Special Programmed Function bits (SPF bits, SPF01 - SPF32). The EEPROM technology makes any external backup battery unnecessary and helps to reduce cost. The on-chip EEPROM is organized as three arrays of 38 bit capacity each, see fig. 8 for the allocation of the individual bus to EEPROM addresses and their meaning.

A special program mode is implemented in the decoder to support EEPROM write and read operations. The decoder must be in Off state for EEPROM write or verify operation. The program mode is entered by setting the PD input, pin 7, to a logic LOW and the PS input, pin 8, to a logic HIGH at any time. The program mode is left and normal decoder operation resumed upon

- removing the power supply, or
- setting the PD input to a logic HIGH after the 38th data bit of an EEPROM operation while continuing to clock the PS input, see timing diagrams for more details.

A specific EEPROM array is selected by setting data bits SEL0 and SEL1 on input PD to the predefined values during the second and third pulse on input PS, see also fig. 9 and 10:

SEL0	SEL1	Selected Array
0	x	1
1	0	2
1	1	3

x is a don't care.

The three EEPROM arrays can be programmed and verified in any arbitrary order. The program mode has to be left after write or read operation on any of the three arrays.

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EEPROM ARRAY 1

Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	ENA

Bit37	Bit36	Bit35	Bit34	Bit33	Bit32	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19
B17	B16	B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	ENB

EEPROM ARRAY 2

Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C17	C16	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00	ENC

Bit37	Bit36	Bit35	Bit34	Bit33	Bit32	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19
D17	D16	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	END

EEPROM ARRAY 3

Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPF13	SPF12	SPF11	SPF10	SPF09	SPF08	SPF07	SPF06	SPF05	SPF04	SPF03	SPF02	SPF01	FR20	FR21	FR22	FR10	FR11	FR12

Bit37	Bit36	Bit35	Bit34	Bit33	Bit32	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19
SPF32	SPF31	SPF30	SPF29	SPF28	SPF27	SPF26	SPF25	SPF24	SPF23	SPF22	SPF21	SPF20	SPF19	SPF18	SPF17	SPF16	SPF15	SPF14

Fig. 8 PCF5001T EEPROM bit allocation

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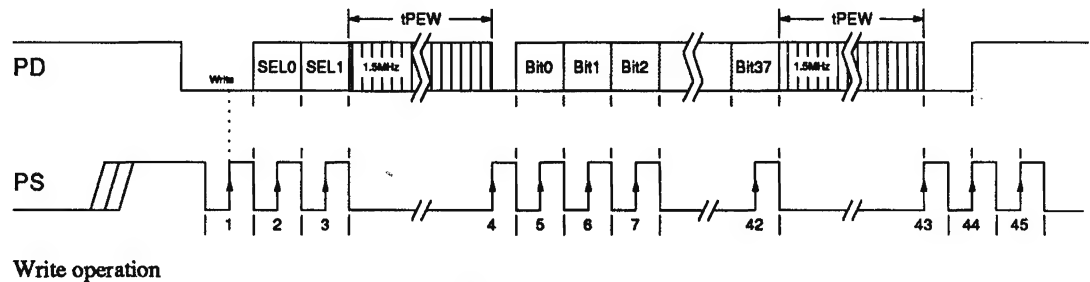


Fig. 9 EEPROM write operation

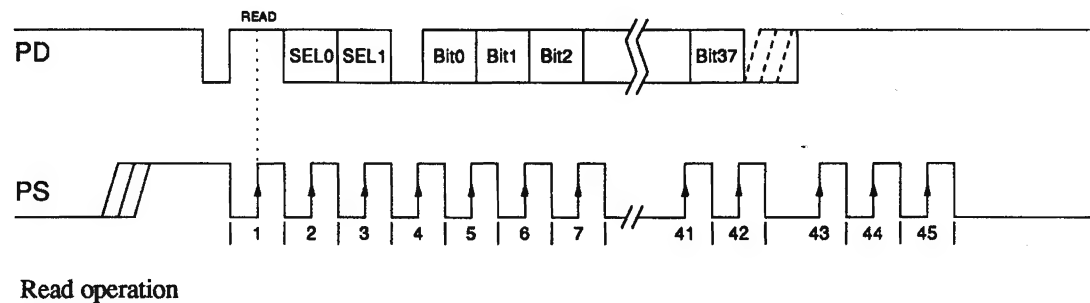


Fig. 10 EEPROM read operation

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4.10.1 Receiver Identification Code Mapping

A digital user address (RIC) in the POCSAG system comprises 21 bit, but the three least significant bits are coded in the frame number and therefore not explicitly transmitted. The PCF5001T supports four user addresses: RIC A, B, C and D. RICs A/B and RIC C/D must share the same frame number. RICs A and B reside in frame FR1 (FR10 FR11, FR12) while RICs C and D are allocated to frame FR2 (FR20, FR21, FR22). Prior to programming, RICs A/B and C/D are divided into two 18 bits address codes and a common frame number. An example for decimal address to EEPROM bit content conversion is given in fig. 11. Every address must be explicitly enabled by resetting the associated enable bit to 0. The frame numbers shall be programmed to the same frame, if only one frame number is allocated to the pager.

4.10.2 Special Programmed Function Bits

EEPROM array 3 contains storage for the two frame numbers and 32 Special Programmed Function Bits SPF01 to SPF32. The SPF bus allow for application specific configuration of the decoder circuits. The following features can be selected by appropriate programming of the SPF bits:

- SPF01: 0:

1:
- Alert-only mode

Display pager mode
- SPF02: 0:

1:
- 512 bit/s data rate

1200 bit/s data rate, fixed 76.8 kHz crystal configuration
- SPF03: 0:

1:
- 32768 Hz crystal configuration

76800 Hz crystal configuration

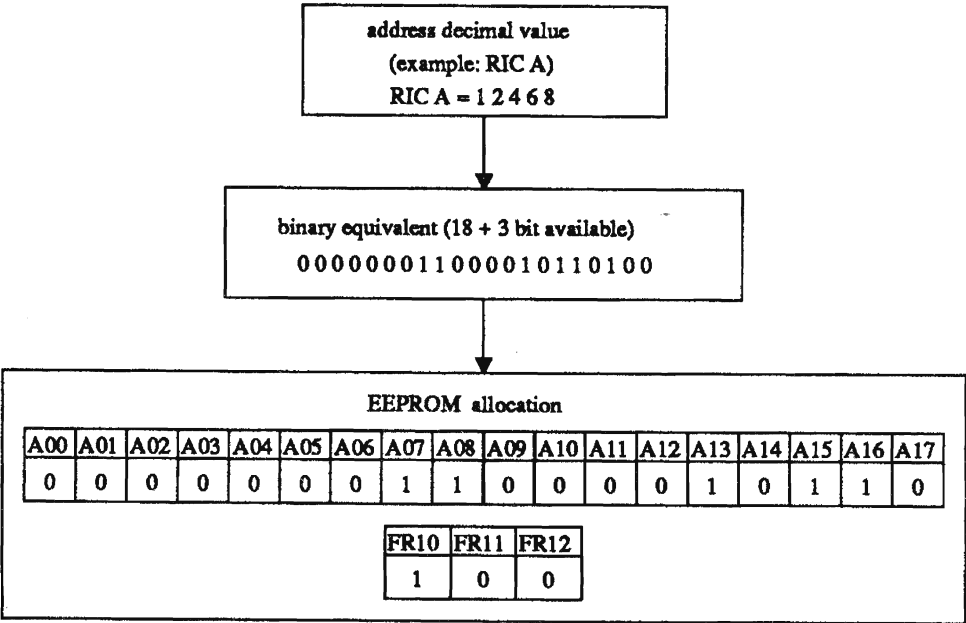


Fig. 11 User address to EEPROM bit content conversion example

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SPF04, SPF05: receiver establishment time
(depending on data rate)

512 bit/s data rate:

- 0 0: 7.8 ms (4 bit duration)
- 0 1: 15.6 ms (8 bit duration)
- 1 0: 31.3 ms (16 bit duration)
- 1 1: 62.5 ms (32 bit duration)

1200 bits data rate:

- 0 0: 53.3 ms (64 bit duration)
- 0 1: 6.7 ms (8 bit duration)
- 1 0: 13.3 ms (16 bit duration)
- 1 1: 26.7 ms (32 bit duration)

SPF06, SPF07: Duplicate call suppression time out and
out-of-range hold-off time out

- 0 0: 30 s
- 0 1: 60 s
- 1 0: 120 s
- 1 1: 240 s

SPF08: 0: voltage converter disable, if SPF01=1
1: voltage converter enable, if SPF01=1

SPF09: 0: silent override on address C disabled
1: silent override on address C enabled

SPF10: 0: silent override on address D disabled
1: silent override on address D enabled

SPF11: 0: vibrator option disabled
1: vibrator option enabled

SPF12: 0: call termination method 3 (Combination
method)
1: call termination method defined by SPF13

SPF13: 0: numeric data deformatting,
call termination method 1
1: numeric data deformatting on function
code 00 only, call termination method 2

SPF14: 0: Duplicate call suppression disabled
1: Duplicate call suppression enabled

SPF15: 0: Out of range indication on OL output
disabled, hold-off period is zero
regardless of SPF06 and SPF07 setting

1: Out of range indication on OL output
enabled, if SPF01 = 0,
hold-off period according to SPF06 and
SPF07

SPF16: 0: Repeat alert disabled
1: Repeat alert enabled

SPF17: 0: Call data output on OL disabled
1: Call data output on OL enabled

SPF18: Spare, free for user defined use

SPF19: program always 0

SPF20 - SPF30: Spares, free for user defined use

SPF31: 0: Alerter frequency 2048 Hz
1: Alerter frequency 2731 Hz

SPF32: 0: Frequency reference output 16384 Hz, if
SPF01 = 1
1: Frequency reference output 32768 Hz, if
SPF01 = 1

Special Programmed Function bits SPF18 and SPF20 to
SPF30 have no meaning inside the decoder. They can be
used in display pager applications to select various other
user defined options prepared in the microcontroller
program memory, such as country specific character sets
and user interface options. The microcontroller can read
these user defined SPF bits by making use of the
EEPROM read back feature described in section 6.6.

4.10.3 Program Timing

4.10.3.1 Write Operation

The EEPROM write mode of the decoder is selected by
keeping input PD low during the first pulse on input PS
after entrance into program mode, see fig. 9. Data on pin
PD is input into the decoder serially with the rising edge
of the clock signal applied on input PS. All bits of one
array are input in turn starting with bit 0.
Before actually inputting data bit 0 and after the 37th bit,
a special erase/write cycle must be executed. During this
erase/write cycle period

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- the supply voltage of the decoder must be raised to 5 V, and
- a square wave clock signal with a nominal frequency of 1.5 MHz must be applied to input PD.

The 1.5 MHz clock signal shall switch between the two logic levels. Its frequency may vary in a reasonably wide range, see the data sheet for more information. A simple RC-type oscillator using a Schmitt-Trigger gate 74HCT132 with $R = 1\text{ k}\Omega$ and $C = 1\text{ nF}$ can be used to generate the required clock signal. The 32 kHz, respectively 76.8 kHz crystal oscillator must operate during programming independent of this 1.5 MHz clock signal.

The decoder must be operated at 5 V supply voltage during the erase/write cycle. It is possible to operate the decoder at 5 V supply voltage during the whole program operation. Although the decoder is able to operate at 5 V continuously, care must be taken to ensure that the maximum voltage level on pin VREF is not exceeded when using the internal or an external voltage doubler. A zener diode or an additional load may be required to keep the voltage below the specified limits during 5 V operation.

6.10.3.2 Read Operation

The EEPROM read or verify operation of the decoder is selected by keeping input PD high during the first pulse on input PS after entrance into the program mode, see fig. 10. EEPROM data contents of the selected array are output bit by bit using PD as data output starting with 0. Every positive edge on input PS switches to the next bit.

During read operation the supply voltage may be as low as 1.5 V. The crystal oscillator, pins X1 /X2, must operate during read operation. Refer to the data sheet for more details.

6.10.4 Recommended Program Interface

This section provides some background information on how to program and verify the PCF5001T EEPROM in a production environment and how to arrange the external circuitry to allow easy and quick program and verify operation. It is assumed that during production no power

supply (battery) is connected to the decoder and that the decoder is decoupled from other circuits parts by a diode as shown in the application examples fig. 4 and 5.

The program control inputs PD and PS have internal biasing resistors of a sufficiently low impedance so that selection of the inactive states is ensured even if the inputs are left open circuit during normal operation of the decoder. Input PD has an internal pull-up resistor while input PS has an internal pull-down resistor, additional external biasing resistors are not required.

Provide pads on the pager printed circuit board for probe connections to the following pins of the decoder circuit: VS, VD, VREF, IE, ON, SK, SR, AI, PD, PS. All inputs can be driven by a standard CMOS/HCMOS output. Pin PD is used as input and output thus requiring a bidirectional driver configuration. Ensure that the driver output voltages are compatible with the specified signal input range of the PCF5001T. The PCF5001T is decoupled from the other circuitry of the pager by means of a diode, see fig. 4 and 5. Pads VS and VD are connected to an external power supply. This power supply may be either 3 V or 5 V depending on whether the designer wishes to switch the supply voltage during the erase/write cycle mentioned in section 4.10.3.1 or not. If a 5 V supply is used, the designer must ensure that the remaining circuits parts can operate at this voltage and that the maximum voltage times on the microcontroller interface are not exceeded, if any voltage converter is in use. Inputs IE, ON, SK and SR are connected such that the Off state of the decoder is selected. Initially, all other drivers are in the high impedance state.

Perform the following sequence:

- Connect the probe to the assembled printed circuit board.
- Wait for the internal power-on reset duration.
- Activate the drivers for PS and PD and select the program mode.
- Perform the required write or read operation according to the timing shown in fig. 9 and 10 and as specified in the PCF5001T data sheet. If the decoder was not operated from a 5 V supply, the supply voltage must

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be switched to 5 V during the erase/write period of the write cycle. Please note that for read operation the driver connected to pin PD must be set for input after the third pulse on PS and switched back to output after the 42nd pulse on PS due to the fact that PD becomes output during the respective interval.

- e) Leave the program mode by driving input PD with a logic HIGH level and by supplying the specified number of pulses on input PS. Then disable the drivers.
- f) Continue with writing or reading of the other arrays by going back to step c).
- g) Disconnect the probe from the printed circuit board.

One possible pager and probe configuration with the relevant connections for programming is shown in fig.12. The probe has also to incorporate the required level shifting from 3 V to the specific logic level of the driver circuitry, if the decoder is not always operated from a 5 V supply. It may also be necessary to provide additional pads to test the paging receiver and the microcontroller.

4.11 Call Data Output on LE.D.

The PCF5001T allows for output of call data on the LED output OL, pin 13. This feature is selected by setting SPF17. The data is output concurrent to the output on the serial microcontroller interface outputs DO and DS in a RS232-type format with a data rate of 2048 bit/s. The start and stop conditions on the microcontroller interface are replaced by start and stop bits as required for asynchronous data transfer. The resulting data format is one start bit, eight data bits as on the microcontroller interface, one stop bit, see fig. 13. Data is transferred LSB first.

This feature may be used to drive an external printer device using an optical communication link or for call data evaluation during production or type approval tests.

4.12 Decoder Test Modes

The decoder supports two test modes, which are intended for use in production and type approval tests. These test modes enable or disable specific features of

the decoder to support these tests and to comply with the relevant requirements.

Inputs TS and TT, pin 11 and 18, which select chip test modes, are not intended for use by customers and must be left open circuit or connected to VS. Internal pull-down resistors on both inputs ensure proper operation without external connections to VS.

4.12.1 Board Test Mode

The board test mode is intended for pager manufacturer's production test and alignment procedures. The board test mode is entered by setting input PD to a logic LOW at any time. In board test mode the following special features are provided:

- receiver enable output RE is set constantly high (Receiver Tuning Procedure)
- output AL is activated upon low level on input ON.
- output AH is activated upon high level on input SR.
- outputs OL and OM are activated on high level on input SK.
- entrance to pager test mode is enabled, see section 4.12.2.

Exit from board test mode is made by setting input PD to a logic HIGH level again, which is the default due to the internal pull-up resistor on PD.

4.12.2 Pager Test Mode

Pager test mode is provided for PTT type approval tests. Entrance to the pagertest mode is only possible following operation in board test mode. Pagertest mode is entered upon reception of a call to any programmed and enabled user address with any function bit combination while being in board test mode, i.e. input PD is at logic LOW level. Once the decoder is in pager test mode, the features of the board test mode are no longer active. The following changes to normal operation apply:

- any call alert is terminated after 2 seconds
- duplicate call suppression is disabled, i.e. subsequent calls received under the same address and function bit combination are all alerted.

Exit from pager test mode is possible only by disconnecting the power supply from the decoder.

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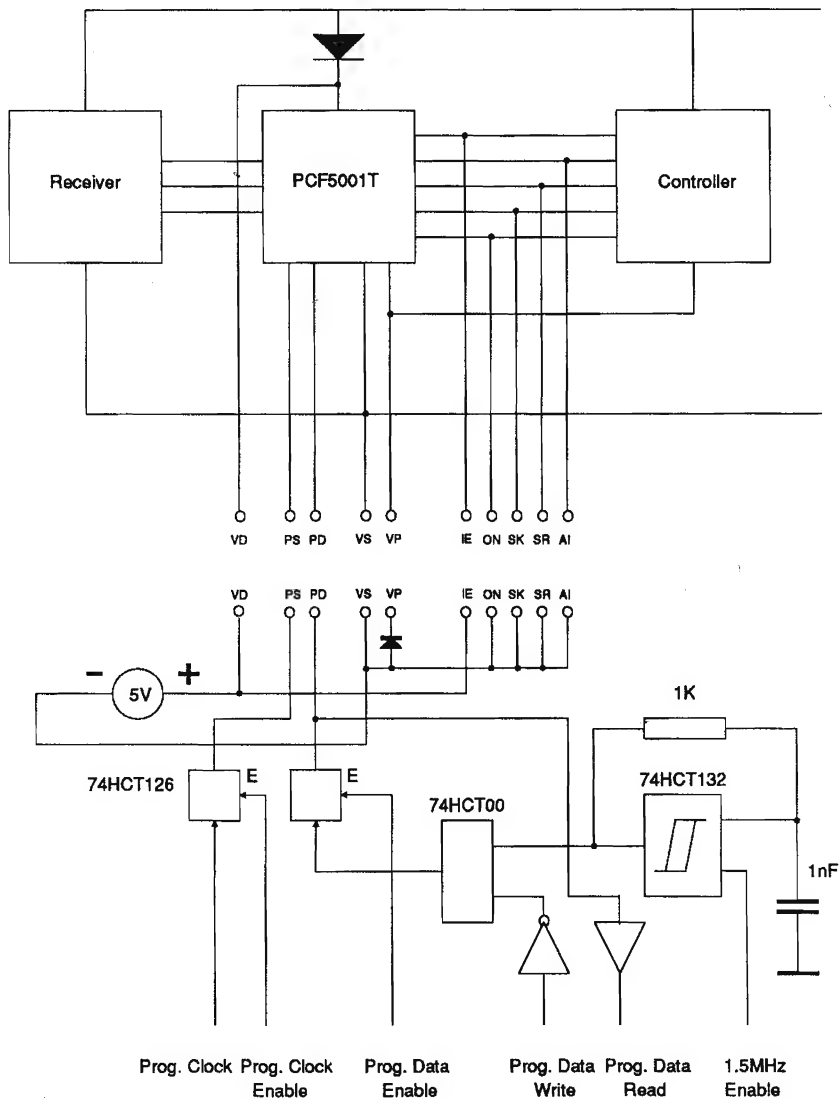
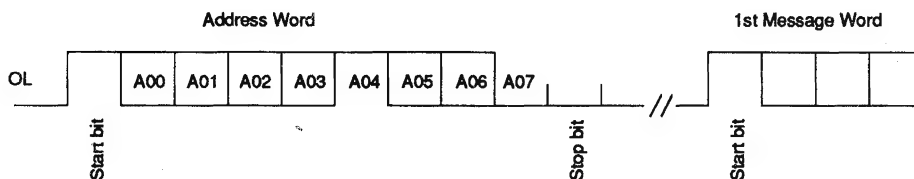


Fig. 12 PCF5001T program interface and connections

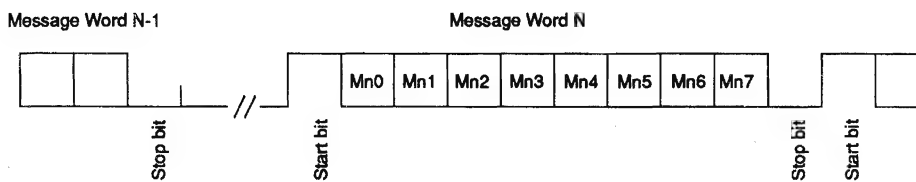
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Start of Transfer



Message Transfer



End of Transfer

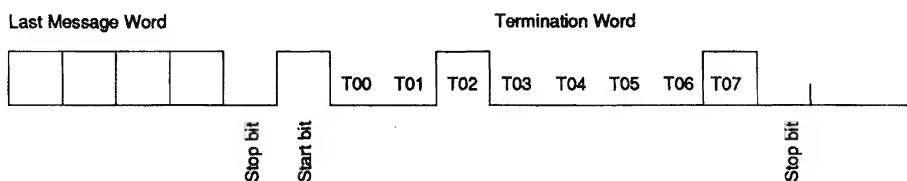


Fig. 13 Call data output on LED output

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5. Alert-Only Pager Operation

The PCF5001T supports alert-only pager applications. This mode is selected by resetting SPF01 to "0". In alert-only pager mode, all user interface functions are implemented in the PCF5001T, no external microcontroller is required. The complete alert-only pager consists of two integrated circuits only, the PCF5001T decoder and a paging receiver like our UAA2050T/ UAA2080T VHF/UHF integrated digital paging receiver, see fig. 4.

5.1 Switch Interface

In alert-only pager mode, the PCF5001T supports a slider switch interface for status input and a push-button interface for status interrogation and alert termination operation. Input SR must be activated for a duration longer than the switch scan period, which is about 62.5 ms, to cause the desired action. The decoder scans inputs ON, SK and SR periodically to detect any change in logic level, whereupon it takes the desired action.

Inputs ON and SK have internal pull-up resistors, input SR has an internal pull-down resistor. Input IE has no meaning in alert-only pager mode, but must be connected to either of the two supply pins VS and VD.

5.1.1 Status Selection

The operating state of the decoder is selected by applying the appropriate input levels to the decoder status inputs. The logic levels are assigned such that a three position slider switch can be used to provide the required sequence of logic levels, see fig. 4.

ON input	SK input	Selected State
0	don't care	Off
1	0	On
1	1	Silent

Any new operating state is selected by simply moving the slider switch to the desired position. The selected operating state - On, Off or Silent - is entered with a possible delay of one switch scan cycle period.

5.1.2 Status Interrogation

The operating status of the decoder may be interrogated by activating the "Status/Reset" pushbutton connected to input SR. As a result, generation of the appropriate status interrogation cadence is triggered.

5.1.3 Alert Cadence and Battew Low Alarm Termination

Any alert cadence generated by the decoder can be terminated by operating the "Status/Reset" pushbutton. The start-up alert cannot be terminated.

High-level intense alert tones generated by operating the alarm input AI can only be terminated by pulling input AI to the inactive state again. Input AI has an internal pull-down resistor in the alert-only pager mode of the decoder and is independent of the logic levels on input IE.

5.2 Silent State Operation

The Silent state of the PCF5001T decoder is intended for pager users who do not wish to be disturbed by the alert cadences resulting from incoming calls. In alert-only pager mode, the PCF5001T keeps track of incoming calls and maintains them in a special store for alert cadence generation following the exit from Silent to On state. However, optical and vibrator alert are also provided in Silent state.

5.2.1 Silent Call Storage

The PCF5001T provides a special call storage register with eight independent flags. The flags are numbered 1 to 8. Calls are stored in the flag that corresponds to the related call alert cadence, thus calls received under RIC A/C enter flags 1 to 4 and calls under RIC B/D go into flags 5 to 8.

The respective flag is set, whenever a valid call is detected. The flag remains set

- to allow for alert cadence generation after complete receipt of a call in On state,

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- to allow for regeneration of call alert cadences upon change from Silent to On state of the decoder,
- to support re-generation of call alert cadences in combination with the repeat alarm feature of the decoder, see section 5.3.

If more than one call is stored in the register, the calls are alerted in order of their respective flag positions independent of their order of receipt. Each flag of the silent call storage register remains set until it is reset upon call alert termination, see section 5.1.3. The flag is also reset and no alert cadence generated, a call was received when operating in data fail state and the call was terminated due to an uncorrectable code word directly following the address code word.

The silent call storage is active in alert-only mode only.

5.2.2 Silent Override Feature

In the PCF5001T, a silent override feature is provided, which allows to classify calls as urgent and let them override the silent state of the decoder. Silent override can be enabled on RIC C and D by programming SPF09 and SPF10 accordingly. Silent override calls received while operating in Silent state of the decoder cause the normal alert cadences to be generated as in On state. The vibrator output OM is not activated when alerting silent override calls.

5.3 Repeat Mode Operation

The repeat mode has been implemented to indicate calls to the user that have been received while he could not observe his pager. These calls are kept in the silent call storage and can be re-alerted upon request. The repeat mode of the decoder is entered as soon as the alert cadence of any incoming call is not terminated by the user. If enabled by SPF16, repeat mode operation is indicated to the user using a special repeat mode indication cadence. The repeat mode is left and the stored cadences are generated upon activation of the status/reset pushbutton. This will also clear the respective flags in the silent call storage register. If no calls have been stored and the status/reset pushbutton is activated, a status indication cadence is generated instead.

5.4 Duplicate Call Suppression

Some paging network operators automatically repeat paging calls to increase the call success rate, but do not want these repeated calls to be alerted again. The duplicate call suppression logic implements this feature in our decoder. In alert-only pager mode, it operates as follows.

An initial call sets the duplicate call suppression timer. This call is alerted normally. During the duplicate call suppression time out, set by SPF06 and SPF07, calls received under the same RIC and function bit combination as in the initial call are rejected and not alerted again. Any call received under any other RIC or function bit combination resets the duplicate call suppression logic and starts the time out again.

Duplicate call suppression time out is independent of out-of-range activity, but out-of-range hold-off time out is not started prior to finishing the duplicate call suppression time out.

5.5 Features not available in Alert-Only Pager Mode

The following features are not available, if the PCF5001T operates in alert-only pager mode, i.e. when SPF01 = 0:

- the voltage converter is always disabled, SPF08 is irrelevant. Leave pins CN and CP open and connect pin VREF to VS.
- the reference frequency output FL is disabled.
- no level shifting is provided for the serial microcontroller interface signals, although the call data transfer is maintained.
- the internal biasing resistors on inputs ON, SK, SR and AI are activated. The status input logic is configured for slider switch and pushbutton operation, respectively.
- the silent call storage is active in Silent state and repeat mode.

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- identical calls received within the duplicate call suppression time out are not alerted, if duplicate call suppression is enabled.
- the EEPROM data read back function is not available.
- input IE has no effect and must be connected to either VS or VD.
- special conditions for call alert cadence generation apply for calls received in data fail state.

5.6 Application Circuit Diagram

The circuit diagram of an alert-only pager using the PCF5001T is shown in fig. 4. The decoder interfaces directly to our integrated VHF/UHF paging receiver circuit UAA2050T/UAA2080T. Unused outputs of the decoder are not shown for clarity.

6. Display Pager Operation

In display pager mode, the PCF5001T POCSAG decoder supports numeric and alphanumeric message pager applications in combination with an external microcontroller. The display pager mode is selected by programming SPF01 = 1.

The PCF5001T provides a serial data output port for transfer of call and message related data upon receipt of valid paging calls. Normally, an external microcontroller is connected to this port for post-processing of received data.

One of the strongest features of our chipset in display pager applications is that the microcontroller can be kept in power-down mode most of the time to have as low a power consumption as possible. Wake-up signals implemented in the start condition preceding the serial call and message data transfer ensure that the microcontroller is activated in time.

6.1 Microcontroller Interface

In display pager mode, the control interface is configured to a bus-type structure. Input IE, pin 19, is used as the interface enable input. The interface is enabled whenever IE is set to a logic HIGH level. In this case inputs ON, SK,

SR and AI are active and outputs BL and OR are driven by the decoder. Data output pins DO and DS are always active. If the interface is not enabled, the inputs do not respond to applied signals and the outputs are brought to a high-impedance state.

The function of the status/reset pushbutton is also replaced by a logic input on input SR. A positive going pulse on input SR while the interface enable input IE is active results in status/reset operation.

6.1.1 Status Selection

Inputs ON and SK are used to select the operating state of the decoder. They are configured for static logic input without having internal biasing resistors. The status information has to be applied while input IE is active. The status is selected according to the following table:

ON input	SK input	Selected State
0	0	Off
0	1	Off, EEPROM read back mode
1	0	On
1	1	Silent

In order to avoid unwanted intermediate operating states, the status information should be applied prior to activating the IE input. It is possible to supply the old or the new status information and change during the active period of IE. The status information is changed according to the input signals and latched upon the falling edge of the IE input signal, see the data sheet for exact timing information.

6.1.2 Status Indication

As in alert-only pager mode, status indication tones are generated upon status interrogation. Status interrogation in display pager mode takes the form of a positive going pulse on input SR while the interface enable input IE is active. The status alert is generated following the rising edge of the pulse on input SR.

6.1.3 Alert Cadence and Battery Low Alarm Termination

Any alert cadence generated by the decoder can be terminated by a positive going pulse on input SR while

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the interface enable input IE is active ("Status/Reset" operation). The start-up alert and the alarm tone generated following activation of the AI input cannot be terminated.

The call alert cadence generation commences with a certain delay (min. 52 ms) after the call termination word has been sent and the stop condition was generated, see section 6.1.5.4. and the data sheet. This gives sufficient time to the microcontroller to cancel call alert generation for duplicate call suppression or user defined alert cadence patterns.

6.1.4 Alarm Input

High intensity alarm tones can be generated in On and Off state of the decoder by setting input AI to a logic HIGH level while the interface enable input IE is active. The status of the alarm input is latched on the falling edge of the signal on input IE. Generation of alarm indication is continued according to the latched status. The input on AI may be a sequence of pulses to obtain a modulated alarm tone output or to generate user defined alert cadences.

6.1.5 Serial Microcontroller Interface

The PCF5001T provides a serial data output port for transfer of call and message related data upon receipt of valid paging calls. Normally, an external microcontroller is connected to this port for post-processing of received data. The serial port is also provided to allow read-back of EEPROM information, see section 6.6

The basic concept of our chipset in display pager applications implies that the microcontroller is in power-down mode most of the time to have as low a power consumption as possible. As a result the microcontroller must get a wake-up signal upon reception of a valid call to ensure the data transfer will be successfully completed by the microcontroller. This wake-up signal is implemented in the start condition. Following the start condition and a delay for microcontroller activation, an address word is sent via the serial port, refer to fig. 14. Then, the transfer of call data information takes place. The data rate is fixed to 2048 bit/s independent of the input data rate. The information received in the current code word will be

buffered and transferred with a delay of one code word. The data transfer is synchronized with the beginning of the next code word. Completion of the call data transfer is indicated by issuing a termination word and generating the stop condition. Please note that the data transfer protocol is not compatible with the I²C-bus standard.

6.1.5.1 Start Condition

A start condition on the serial microcontroller interface indicates the beginning of a new call data transfer. The start condition is intended to cause a wake-up from power-down mode to the external microcontroller. During the start condition period data output DO is driven LOW while the data strobe output DS remains at logic HIGH level. This condition lasts long enough, min. 4750 μ -sec, to allow for the microcontroller to start the crystal oscillator, leave the power-down mode, enter the normal operating mode and prepare for data transfer.

After the start condition, an address word is transmitted. The address word gives call address related information. The first low going pulse on output DS indicates the first bit of the address word (Bit 0). The address word bus contain the following information:

- Bit 0: Bit 21 of the received address code word (Function code)
- Bit 1: Bit 20 of the received address code word (Function code)
- Bit 2 and 3: Call address information.
 - 0 0: Call received under RIC A
 - 0 1: Call received under RIC B
 - 1 0: Call received under RIC C
 - 1 1: Call received under RIC D
- Bit 4: always set (Bit 4 = 1)
- Bit 5: set, if the address code word was received while operating in data fail state of the synchronization algorithm
- Bit 6: set, if the duplicate call suppression time out is active, i.e. a call was received under the same RIC and function bit combination.
- Bit 7: always reset (Bit 7 = 0).

Bit 5 can be used to reject calls that have been received while the synchronization code word at the beginning of the current batch has been in error. Bit 6 indicates to the microcontroller that a call under the same RIC and

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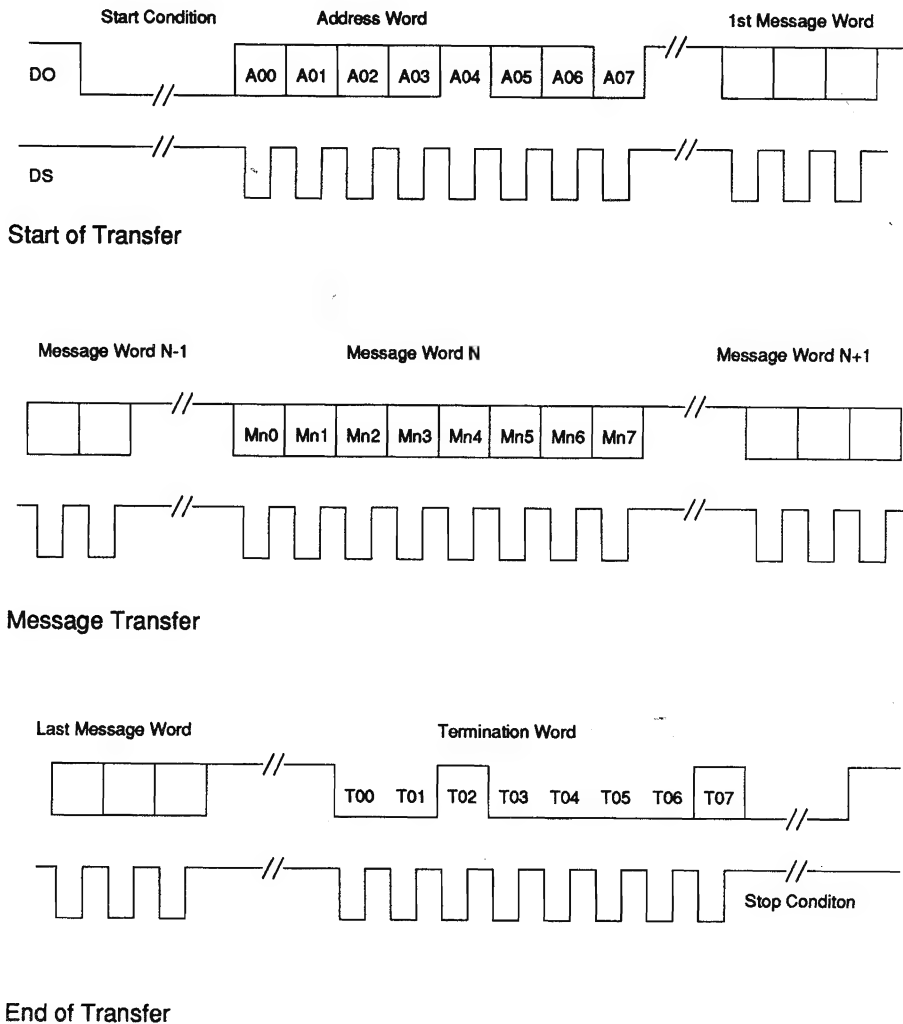


Fig. 14 Call data transfer on the serial microcontroller port

function bit combination was received within the duplicate call suppression time out. The microcontroller will normally compare the message bytes of those calls with the information from previously received messages to

detect duplicated calls and possibly cancel call alert generation. The PCF5001T performs no compare operation on received message code words for duplicate call detection!

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6.1.5.2 Data Transfer

In message paging systems, the actual call information is placed in message code words. The POCSAG standard defines numeric and alphanumeric type messages.

In numeric calls five digits of 4 bit (nibble) are packed into the 20 bits of the message code word's message field. This five digits can be transmitted in one message code word. Messages that exceed this five digit length require more message code words.

In alphanumeric calls the characters of the information to be transmitted are coded in 7 bit ASCII format. The whole message is represented as a string of such 7 bit ASCII characters. The transmitter packs the information bit-by-bit into the message fields of available message code words: The first message code word contains all bits from characters 1 and 2 but only 6 bits from character 3, the second code word contains the remaining bits from character 3, all bits from characters 4 and 5, and so on. Unused bit positions at the end of a message call are filled with special dummy characters.

The PCF5001T handles numeric and alphanumeric type messages differently, see the following section. In either case, data received in the current code word is held inside the decoder until the beginning of the next code word. After translation, see following section, the converted characters are output byte by byte in a block starting at the first bit of the next code word. In numeric pager applications always five bytes are output with the information taken completely from the previously received code word. In alphanumeric pager applications two or three bytes are output with the information taken from possibly the last two received code words.

The bytes within a block are separated by t_{BDV} min. 1210 μ s, to give sufficient time to the microcontroller to put the received byte into an intermediate store. After all bytes associated with the last message code word have been sent, there is a delay of t_{CWD} min. 3420 μ s, until the next byte from the next message code word is transmitted. This delay can be longer, if a synchronization code word was received between message code words.

In either case, numeric or alphanumeric, the information is transmitted byte wise. Each byte contains one

translated character or digit. The bits of each byte are transmitted LSB first. The last bit, Bit 7, is the error flag, which is set, if the transmitted byte contains bits from a message code word that could not be successfully error corrected. This indicates that this byte may possibly be in error. If, for any reason, the call termination criteria implemented in the PCF5001T do not match the specific customer / PTT requirements, the microcontroller can evaluate the error flags of subsequent bytes and implement the required call termination method in software by counting the number of concatenated erroneous bytes.

6.1.5.3 Call DataTranslation

The PCF5001T performs automatic deformatting of received message bits into characters (ASCII equivalents). The PCF5001T supports deformatting of numeric and alphanumeric paging message formats. The deformatting of received message bits into their ASCII equivalent bytes is controlled by SPF13 and the function bit combination, bit 20 and bit 21, in the received address code word:

SPF13	Bit 20	Bit 21	Message Handling
0	don't care	don't care	Numeric
1	0	0	Numeric
1	1	0	Alphanumeric
1	0	1	Alphanumeric
1	1	1	Alphanumeric

Simply saying, with SPF13 = 0, all message calls are deformatted as numeric calls. With SPF13 = 1, only calls for function code 00 are deformatted as numeric calls while all the others are deformatted as alphanumeric calls. Please note that SPF13 automatically also influences the choice of call termination methods, see sections 4.2.5.2 and 4.10.2.

In numeric calls, each digit is deformatted into its one byte ASCII equivalent according to the following conversion table.

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4 bit block				7 bit block character			
lsb		msb		lsb		msb	
0	0	0	0	"0"	0	0	0
1	0	0	0	"1"	1	0	0
0	1	0	0	"2"	0	1	0
1	1	0	0	"3"	1	1	0
0	0	1	0	"4"	0	0	1
1	0	1	0	"5"	1	0	1
0	1	1	0	"6"	0	1	1
1	1	1	0	"7"	1	1	1
0	0	0	1	"8"	0	0	1
1	0	0	1	"9"	1	0	1
0	1	0	1	"**"	0	1	0
1	1	0	1	"U"	1	0	1
0	0	1	1	" "	0	0	0
1	0	1	1	"_"	1	0	1
0	1	1	1	"")"	1	0	1
1	1	1	1	"("	1	1	0

In alphanumeric calls, to every seven message bits received the error flag is added and the whole byte output without any further conversion. The first bit in a byte (Bit 0) is the first received bit, Bit 6 is the last received bit.

The selection of deformatting algorithms is based on the POCSAG proposal for message call assignment to function codes. As there is a fixed mapping between the characters output on the serial port and the bits contained in the message bit fields of received message code words, it is always possible to reconstruct the original message bit fields in the microcontroller. This gives the flexibility to implement other conversion algorithms.

6.1.5.4 Stop Condition

Upon call termination, see section 4.2.5.2, the decoder first outputs any character that is not complete by appending the appropriate number of "0" bits to the buffered data bus, adding the error flag and transferring it as usual. There after an 8 bit termination word is output, which is basically the End of Texts (EOT, 04_{hex}) character plus an error flag, which is set whenever the call was terminated due to an excessive number of uncorrectable code words.

Following the termination word, a stop condition is generated. The stop condition is indicated by output DO being held at logic LOW level while output DS is set to logic HIGH level for a duration of T_{SP} , min. 595 μ s. It is the termination word together with the stop condition that indicate the end of a message transfer. In order to make the stop condition a unique combination of output signals on outputs DO and DS, both outputs are set to logic HIGH output during the inactive periods of a message transfer, i.e. between byte transfers, see also fig. 14.

6.1.6 Reference Frequency Output

In display pager applications, i.e. when SPF01 = 1, the PCF5001T provides a level shifted reference frequency output on FL, pin 28. The output signal is derived from the main crystal oscillator and intended for use by the external microcontroller or to drive a real time clock circuit.

The output signal frequency on FL is 16384 Hz or 32768 Hz, depending on SPF32, irrespective of the main oscillator frequency. Output FL provides exactly the selected number of pulses per second by switching between two frequencies when operating the decoder with a 76.8 kHz crystal frequency, for example a 16384 Hz output is generated by switching between $f_{osc} / 4$ and $f_{osc} / 5$.

6.1.7 Battery Low Level Output

The battery low latch may be sampled directly at the battery low output BL, pin 24, by activating the interface enable input IE. When input IE is inactive, output BL is made high impedance.

The battery low latch is set according to the conditions mentioned in section 6.8. A logic HIGH output represents a poor battery condition. This output may be sampled by the external microcontroller to activate battery low indication symbols in the liquid crystal display (LCD). The battery low latch can only be reset by switching the decoder to Off state.

8.1.8 Out of Range Output

The decoder provides an internal out-of-range latch, which is set whenever the out-of-range condition is

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detected and the half-off period has passed, see also section 4.6.3. The out-of-range latch may be sampled directly on output OR, pin 25, by activating the interface enable input IE. A logic HIGH level indicates the out-of-range condition. When input IE is inactive, output OR is made high impedance.

If $SPF15 = 0$, the out-of-range latch is set immediately following the detection of the out-of-range condition irrespective of the programmed hold-off period, $SPF06/07$. This feature can be used to implement an in-range indication.

Out-of-range indication on the LED output OL is not possible, if the decoder is programmed for display pager applications, i.e. if $SPF01 = 1$.

6.2 Voltage Doubler

The PCF5001T contains an internal switched capacitor voltage converter to provide doubled supply voltage to the external microcontroller and other external circuits such as LCD drivers, message memories and real time clock. To operate the voltage converter, a capacitor 100 nF must be connected between pins CN and CP, the voltage converter must be enabled by setting $SPF08 = 1$ and the display pager mode must be selected. A capacitor 100 μ F shall be connected between VREF and VD. Then, the output voltage on output VREF is set to approximately twice the voltage on pin VS, measured with respect to the common reference VD, i.e. the voltage on VREF is more negative.

When the voltage converter is selected, the logic LOW levels for all the microcontroller interface inputs and outputs are shifted more negative, since VREF is the low level reference for the respective input and output stages of the decoder. This Voltage Level Shifting feature of the decoder enables the chip to interface directly with microcontrollers that require a higher supply voltage than the decoder itself.

The internal voltage converter has improved drive capabilities. The switching frequency is fixed to 16 kHz independent of crystal frequency. Using VREF as the output for the doubled supply voltage, it can supply 600 μ A typ. with $V_{SS} = -2.0$ V and 900 A typ. with V_{SS} at -3.0 V, refer to the data sheet for the exact figures and

conditions. This is normally good enough to operate a CMOS microcontroller and the required peripheral circuits. If the power supply requirements of the external circuitry exceed the drive capabilities of the internal voltage converter, an external voltage converter circuit can be used instead. In this case, the capacitor has to be removed from pins CN and CP and the internal voltage converter should be disabled by resetting $SPF08$. The supply voltage on VREF in this mode must be equal or more negative than the main negative supply voltage on input VS. The voltage level shifting of the microcontroller interface signals is maintained.

It must be recognized by the designer that the output voltage of any voltage converter, internal or external, may exceed the maximum ratings of the decoder circuit during the erase/write cycle period of the EEPROM write operation, see section 4.10.3.1. Therefore, care must be taken to limit the output voltage in these cases. To limit the output voltage, a zener diode or an additional load resistor may be connected to the voltage converter output during programming.

If VREF is not used either to output the doubled supply voltage generated by the internal voltage doubler or to input any supply voltage provided by an external voltage doubler it must be connected to VS. In this case the microcontroller interface signals are referenced to the input voltage on input VS. This may be of interest in cases, where the decoder is operated at a supply voltage, which is directly suitable for the microcontroller.

6.3 Silent State Operation and Silent Override Feature

The serial message data transfer via the serial microcontroller port of the decoder is always maintained regardless of Silent state operation of the decoder. However, the silent call storage is disabled in display pager mode and thus calls received while operating in Silent state are not alerted again upon change to On state.

In the PCF5001T, a silent override feature is provided, which allows to classify calls as urgent and let them override the silent state of the decoder. Silent override can be enabled on RICs C and D by programming $SPF09$ and $SPF10$ accordingly. Silent override calls received while operating in Silent state of the decoder cause the

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normal alert cadences to be generated as in On state. The vibrator output OM is not activated when alerting silent override calls.

6.4 Duplicate Call Suppression

In display pager mode, the PCF5001T provides the same duplicate call suppression feature as in alert only pager mode, see section 5.4, except that call alert is not automatically cancelled by the decoder. Instead, the microcontroller can evaluate the duplicate call suppression flag provided in the address word and cancel generation of call alert during the period t_{ALD} , min. 52 ms, following the stop condition. If the microcontroller does not cancel the call alert during this period, the duplicate call suppression timer is restart. If the microcontroller resets the call alert in time, the duplicate call suppression timer is not restarted and left unchanged thus allowing for further call suppression.

6.5 Repeat Mode Operation

In display pager mode, the PCF5001T provides the same repeat alert feature as in alert only pager mode, see section 4.6.2 and 5.3, except that the call storage is not provided and therefore call alert cadences cannot be retrieved upon interrogation.

The repeat alert feature is activated by setting $\text{SPF16} = 1$. The repeat mode is entered upon 16 second time out of any call alert. Repeat alert is terminated and repeat mode left by any change that is registered by the PCF5001T on inputs ON, SK or SR while the interface enable input IE is active.

6.6 EEPROM Data Read Back Operation via Microcontroller Interface

The PCF5001T POCSAG decoder allows to transfer the complete data contents of the EEPROM to the external microcontroller via the serial output port. This feature can be used

- to implement a factory production check for the programmed RICs inside the decoder circuit in combination with the microcontroller software. In this case the microcontroller software is arranged such that upon request the EEPROM contents are transfer-

red and displayed on the message display in any convenient form.

- to implement country and customer specific versions of the pager configuration in combination with the unused special programmed function bus (Spare Bits). Following a hardware reset, the microcontroller would then first read the EEPROM contents and set the respective options according to the information programmed into the spare bits of EEPROM array 3.

The EEPROM data read back feature is available in display pager mode only.

The EEPROM read back mode is entered by selection of the special EEPROM transfer state of the decoder, see section 6.1.1. Inputs ON and SR have to be set to logic LOW and input SK to logic HIGH level while the interface enable input is activated. This is normally undefined a condition but the decoder operates in Off state. A positive going pulse on input SR during the active period of the interface enable signal triggers the data transfer using DO as data output and DS as the data strobe output. Output data bits are valid during the low period of the data strobe signal.

The contents of the three EEPROM arrays are transferred serially to the microcontroller. The transfer is organized as output of 15 bytes of 8 bits each. 40 bits are used for every array where the 38 bits of each array are extended to 40 bits by two trailing zeros. The very first bit is Bit 0 from array 1, the transfer is finished with the output of SPF32 from array 3 and the two trailing zeros. The output data rate is nominally 2048 bit/s, but the data output may be discontinuous due to the allowed variation in the data bit period, refer to parameter t_{DSE} in the data sheet.

6.7 Interfacing the Decoder to Philips Microcontrollers

The level shifted microcontroller interface signals together with the integrated voltage doubler allow for easy interfacing of the PCF5001 POCSAG decoder circuit to the components of the user interface section of a display pager. The user interface section normally comprises the microcontroller itself, a message memory to store received messages for later display on request, a

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real time clock circuit to time stamp received messages and a liquid crystal display with its associated driver circuits. The peripheral circuits are connected to the microcontroller via the serial I²C-bus, which results in less interconnect and interference problems and also smaller packages compared to devices with parallel bus interface structure.

The start condition shall normally be used to cause the microcontroller to exit the power-down mode and to start normal operation. The duration of the start condition is designed to allow for sufficient crystal oscillator start-up time. The controller should be active to receive the first data strobe following completion of the start condition. In general, ceramic resonators show much faster start-up time and can thus be used to speed up the wake-up, if required.

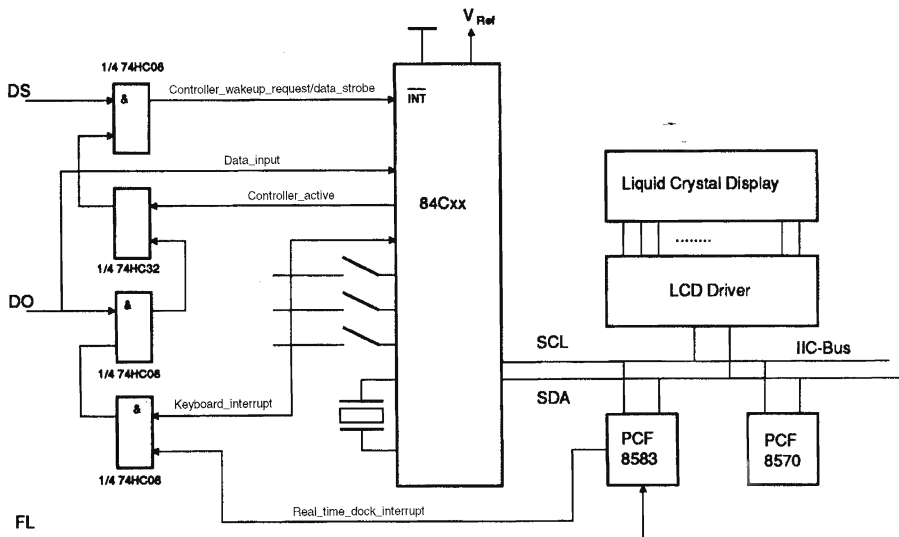
6.7.1 Interface to PCF84Cxx Series

All members of the PCF84Cxx series of Philips microcontrollers support two power down modes, IDLE mode and STOP mode, and provide a single external

interrupt input (INT/T0). As power consumption is most critical in pager applications the designer will normally try to keep the microcontroller in STOP mode for most of the time. Wake-up from STOP mode is possible by executing a reset operation or by applying a low pulse on the external interrupt input.

Basically four different interrupt sources have to be handled using this single interrupt input:

- Interrupt from DO activation indicating the start condition of a call message data transfer
- Interrupt from DS indicating that the next message data bit is available on output DO
- Keyboard interrupt indicating that there was any key operation, and
- Clock interrupt used to trigger possibly a regular keyboard scan operation or to indicate the time out of a longer time period inside the microcontroller software.



Note: Other interface signals not shown for clarity

Fig. 15 Interfacing the PCF5001T to 84Cxx microcontrollers

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Some interfacing glue logic is required to handle these four interrupt sources over the single interrupt input of the PCF84Cxx microcontrollers. One possible arrangement is shown in fig. 15. All four interrupt sources can cause the microcontroller to leave the STOP mode. Once the microcontroller is active, interrupt input can be restricted to DS interrupts only and the remaining inputs are directly polled by the software.

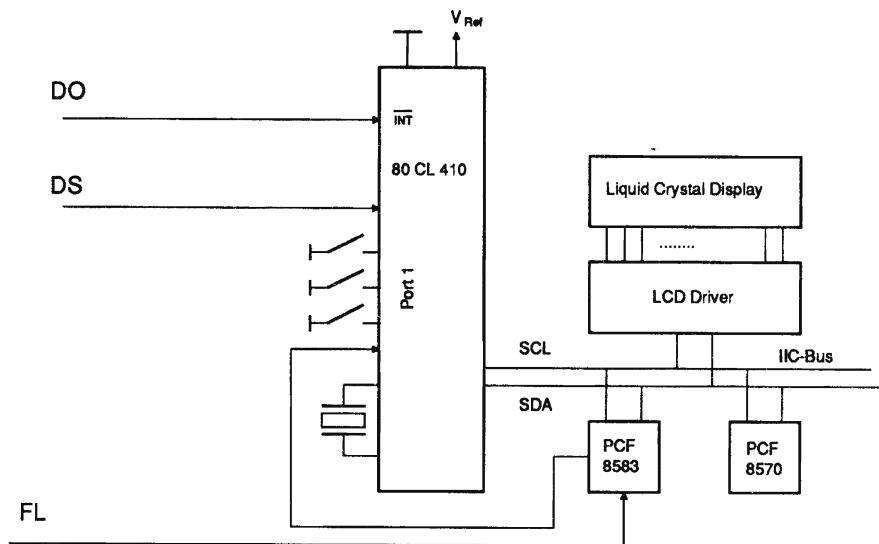
An alternative method of interrupt handling uses a PCF8574 8-bit I²C-bus expander circuit to collect interrupt requests from the four sources and forward them to the single interrupt input. This interrupt will wake up the controller, which in turn will first look for the most important interrupt source directly and finally read the interrupt combination via the I²C-bus. The PCF8574 can also relieve the controller from keyboard monitoring.

A direct connection to pins ON, SK, SR, AI, IE, OR and BL is provided using standard I/O pins of the controller. Output FL of the decoder is used to provide the 32768 Hz clock signal to drive the real time clock circuit.

6.7.2 Interface to P80CLxxx Series

All members of the P80CLxxx family of Philips microcontrollers support two power down modes, IDLE mode and STOP mode, and provide several external interrupt inputs. As power consumption is most critical in pager applications the designer will normally try to keep the microcontroller in STOP mode for most of the time. A hardware reset or logic signals applied to inputs INT2 through INT9 can be used to cause exit from the STOP mode of the controller.

The some four interrupt sources DO, DS, clock and keyboard interrupt as in the previous example have to be handled by the controller, but this time they can all be connected to individual interrupt inputs (Inputs INT2 through INT9) and also scanned via these inputs afterwards. This makes any additional glue logic unnecessary giving the most economic solution for a display pager concept, see fig. 16.



Note: Other interface signals not shown for clarity

Fig. 16 Interfacing the PCF5001T to P80CLxxx microcontrollers

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6.8 Features not available in Display-Pager Mode

The following features are not available, if the PCF5001 T operates in display pager mode, i.e. when SPF01 = 1:

- the user interface inputs and outputs ON, SK, SR, AI, OR, IE and BL are configured for a bus type interface. All internal biasing resistors are switched off except for the one connected to input SR.
- input AI is effective only when input IE is active.
- the duplicate call suppression does not automatically cancel call cadence generation. Instead, a flag in the address word indicates if the duplicate call suppression time out is still active. Operation of the duplicate call suppression timer becomes a function of alert termination.
- the silent call storage is not available neither in Silent state nor in combination with entrance into repeat mode. This implies that call alert cadences cannot be regenerated upon interrogation.
- the voltage converter operation becomes dependent on SPF08 only.
- any call alert cadence will not start before the message transfer and the call alert delay have been completed.
- calls received in data fail mode are alerted independent of call termination condition.
- status indication cadences are not automatically generated following a status change.
- output VREF is driven by the internal voltage converter, if enabled.
- the frequency reference output FL is driven by the decoder.
- the alarm input on input AI is latched on the falling edge of the interface enable input signal and the respective alarm tone maintained.
- optical out-of-range indication via the LED output OL

is disabled. Reset of SPF15 sets the out-of-range hold-off time to zero seconds.

6.9 Application Circuit Diagram

The circuit diagram of a display pager using the PCF5001T is shown in fig.5. The decoder interfaces directly to our integrated VHF/UHF paging receiver circuit UAA2050/UAA2080. Unused outputs of the decoder are not shown for clarity.

For details on possible implementations of the microcontroller section see fig. 15 and 16

7. Operating with non-standard Data Rates

The PCF5001 T basically supports data rates of 512 bit/s and 1200 bit/s. Especially the user interface functions such as alert tones and user interface signal timing are matched to crystal frequencies of 32768 Hz and 76800 Hz, respectively. However, it is possible to use the decoder circuits at non-standard data rate by changing the crystal frequency, but some changes have to be taken into account that may not be adequate in all cases.

The nominal input data rate is determined by the crystal frequency and the setting of special programmed function bits SPF02 and SPF03. The crystal oscillator frequency is a fixed multiple of the input data rate. The ratio is

- 150 for 512 bitts data rate using a 76800 Hz crystal
- 64 for 512 bit/s data rate using a 32768 Hz crystal
- 64 for 1200 bit/s data rate using a 76800 Hz crystal.

This ratio is of course maintained if the crystal oscillator frequency is changed to any arbitrary frequency. For processing of data at data rates other than the standard rates, choose a suitable ratio and determine the new crystal frequency. The new timing values and frequency parameters can be calculated by appropriately scaling the corresponding values given in the data sheet with the ratio of the two crystal frequencies.

With the new frequency, the following features of the decoder are affected and need to be reconsidered:

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- the pager receiver establishment time. Programming of other values into the respective SPF bits may be required.
- the timing of the key input scan algorithm
- the frequency reference output on output FL is no longer at the specified frequencies
- the data rate on the serial microcontroller port
- the duration of start and stop condition
- all call alert cadence timing for outputs AL, AH, OL and OM
- the alerter drive frequency
- the duplicate call suppression and out-of-range hold-off times
- EEPROM data read back timing
- the internal voltage converter
- the power consumption of the decoder.

From the differences listed above it is most obvious that using the decoder at non-standard data rates is most attractive in display pager applications, where inconvenient changes in parameters can be compensated for by the microcontroller software, especially in the user alert functions.

It is important to note that the internal oscillator circuit was not designed to operate with crystal frequencies above 76.8 kHz over the whole temperature and voltage range. For 2400 bit/s data rate, the 153.6 kHz clock input must be provided by an external oscillator circuit and the minimum supply voltage is then 1.8 V.

8. Printed Circuit Board Layout Considerations

In general, the printed circuit board layout (PCB layout) for an application using the PCF5001T is not critical. However, it is good practise to place the crystal resonator close to the oscillator input/output pins X1 and X2, respectively.

In the design of a complete, compact radio pager, the designer must take into account that the PCF5001T paging decoder incorporates a crystal oscillator and digital CMOS logic signals which can generate harmonics. These harmonics can influence the input sensitivity of the pager receiver, if the decoder circuit is located too close to the paging receiver, especially near the antenna input circuitry.

9. Demonstration System Module OM4706

Philips Components provide a modular POCSAG paging demonstration system that includes receiver and decoder modules. A test and program unit, which is also available, can program user addresses (RICs) into the decoder modules and deliver POCSAG coded data. A special report on the paging demonstration system is also available.

The OM4706 evaluation board is a decoder module based on the advanced PCF5001T POCSAG decoder and pager controller. It supports alert-only pager as well as display pager applications. Used in conjunction with existing modules of our demonstration system, this board can be used to evaluate all features of our new decoder chip. A complete alert-only pager can be demonstrated by using the OM4706 evaluation board and one of the receiver boards.

With the OM4706 evaluation board, the following features are provided:

- Complete evaluation of all PCF5001T features
- Rapid prototyping and field tests
- Full POCSAG data decoding
- Suitable for 512 bit/s and 1200 bit/s operation
- Interfaces directly to existing receiver modules

The evaluation board includes an update for the software required by the test and program unit to control PCF5001T programming.

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10. Additional application hints

In the following paragraphs, additional application hints will be given to help the designer to better understand some of the features of the versatile POCSAG decoder and pager controller circuit PCF5001T.

10.1 Repeat Alert

In Alert only pager mode any call alert indication which is not interrupted during the alert timeout period of 16 s is retained in the call store of the PCF5001T.

The Repeat Alert function is enabled by $SPF16 = 1$. As an indication of one or more unacknowledged call alerts the Repeat Alert function allows generation of a unique alert pattern at regular intervals when Repeat mode is active.

The alert tone frequency f_{AL} is warbled with the modulation frequencies f_{AWL} and f_{AWH} and is generated at high level with a Repeat Alert duration of 4 s and a Repeat Alert recurrence of 15 s. The first Repeat Alert duration is 3 s and the recurrence is 14 s.

When the Repeat Alert indication and the Out-of-Range indication are active both timings interfere at OL as described in fig.17.

The Repeat Alert is terminated upon key operation on the SR input. Upon release of the key input all stored calls are generated in numerical order.

10.2 Battery Level Low Detection

In On Status and Silent Status the PCF5001T samples the Battery Sense input (BS) at the 32nd bit of each synchronisation scan when operating in either Data Receive, Data Fail, Fade Recovery or Carrier Off modes.

BS is not sampled and no Battery Level Low condition is detected during Preamble Receive mode. In Power-up mode every received bit is sampled commencing from a period of two codewords after receiver output enable. The Battery Low (BL) output is set immediately upon detection and the appropriate alert commences 52 ms after the latch is set when the decoder is in On Status.

The decoder generates an uncadenced high level alert tone at AH and AL for a duration of 16 s or unless terminated by the user.

In Silent Status the output latch is also set immediately but the alert occurs only in Power-up state.

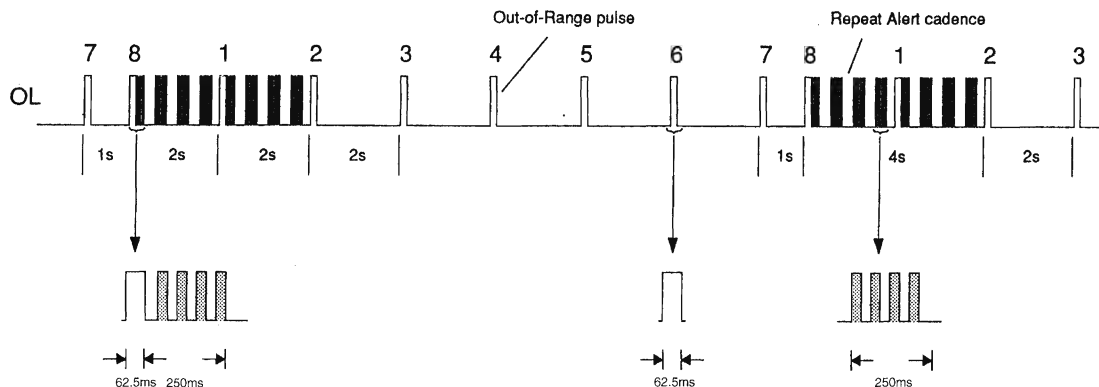


Fig. 17: Repeat Alert Indication & Out-of-Range Indication at OL

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When changing from Silent to On, 62.5 ms prior to the Battery Level Low alert, the output BL returns low for a short period before being set high again. The duration of the low period is fixed at 62.5 ms in Alert Only Pager mode and varies between 0 and 62.5 ms when the PCF5001T is in the Display Pager mode.

The BL output is set and the alert is given on change from Silent to On status even if the BS input is already reset during Silent status.

The Battery Level Low status is reset only by changing the status to Off. Upon changing to On or Silent status again, sampling of the BS input recommences.

In addition to call alerts being held off while the Status/Reset (SR) input is held in the high state, Battery Level Low detection and indication are inhibited.

10.3. Out-of-Range Indication

Whenever data has not been received, i.e. not in Data Receive or Data Fail mode for the selected Hold Off time, the PCF5001T generates an unmodulated indication of the Out-of-Range condition on OL- pin 13.

With the entry into Fade Recovery mode or Carrier Off mode a timer is started. Upon reaching the selected Hold Off time the indication timing commences. The cadence has 2s spacing between each 62.5 ms pulse, except between every 7th and 8th pulse for which the duration is 1s (see fig.17).

When both Duplicate Call Suppression and Out-of-Range are enabled and the Duplicate Call time out is active the Out-of-Range timing is held off until the Duplicate Call Suppression time out has completed. Before commencement of the Out-of-Range time out a pulse of 125 ms is generated on the OR output if interrogated with IE=1.

When the Out-of-Range function is disabled (SPF15=0), the Out-of-Range alert is not generated but the OR output is set immediately upon detection except when the Duplicate Call Suppression is enabled. In that case the OR output is not set until the Duplicate Call Suppression is completed.

10.4 Microcontroller Interface

The PCF5001T provides level-shifted inputs and outputs to form an interface with an external microcontroller. For example a serial data output for transferring of call and messages related data is available at DO & DS. In addition it is possible to transfer data stored in each EEPROM array to the microcontroller.

Upon reception of a valid User Address the PCF5001T transfers an 8-bit Address word indicating address and function.

In the case of a Numeric Message Call, message codewords concatenated to the Calling Address Codeword are deformatted into five 8-bit words per codeword. Each word consist of an 7-bit ASCII character and an Error Flag.

In the case of an Alphanumeric Message Call, message codewords are deformatted into 2 8-bit words per message codeword. The 8-bit words comprising the 7-bit received data and an Error Flag indicating the result of the error correction process.

Characters that are not completely received in a single codeword due to partitioning of the message codeword structure are buffered. When the remaining bits of that character are obtained, on reception of the following message codeword they are appended to the buffered data and transferred to the output as a complete byte. The error flag, appended as the 8th bit of a message word in which the character was divided, indicates erroneous reception of a character if either one of the codewords is incorrect.

The timing diagram in fig. 18 shows the procedure of deformatting the codewords in 8-bit words.

There is a particularity in the timing at the position where the error correction process of the 7th message codeword is finished and the words are transferred to the microcontroller.

In this situation the 20th message byte is transferred to the microcontroller after the 8th instead of the 7th codeword. But the delay of the message byte is not a problem.

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However the Error Flag of the 20th alphanumeric message byte is set if the 7th or the 8th message code-word is received in error, despite the fact that the byte is received complete in the 7th codeword.

Attaching of the error flag to the right message byte is easily done by a small software routine. Additional to the normal error flag check the software must be able to perform a special test at every 20th message byte transfer.

If the error flag of the 20th message byte is set, attaching of the error flag will be done by checking the previous message byte. If the error flag of the 19th message byte is not set the software of the microcontroller should reset the error flag of the 20th message byte.

Upon call termination the PCF5001T transfers any character that is not complete by appending the appropriate number of zero bits to the buffered data

Thereafter an 8-bit Termination character is transferred.

10.5 EEPROM data transfer

The contents of the three EEPROM arrays are transferred serially to the microcontroller upon initialisation by the microcontroller.

The transfer comprises fifteen 8-bit bytes and starts with Bit 0 of array 0. The contents of each array are extended to 40 bits by trailing zeros.

Initialisation of the data transfer is done by setting the SR input high for a period longer than 35µs. However if the pulse on SR input is longer than 50ms the full data transfer to the microcontroller is automatically repeated.

In addition it is possible to enable call data (SPF17 = 1) to appear at the OL output at the same time as the data is transferred on the data output port.

During the data transfer SPF17 is changing, thus the sequence on the L.E.D. is incorrect irrespective of programming. SPF02 and SPF03 are also changing during the data transfer resulting in an unsymmetrical timing at OL and DO.

10.6 Indication and Data Output on L.E.D.

The PCF5001T provides Call Alert indication on L.E.D. in both the On and Silent state. According to the acoustic alert four different alert cadences with warbled modulation as appropriate are possible.

The L.E.D. indication is terminated by operation of the Status/Reset input or by time out.

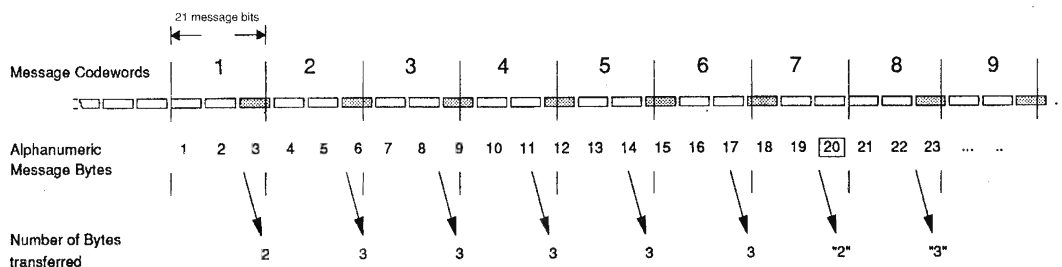


Fig. 18: Timing of the Message Byte Transfer to the Microcontroller

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PCF5001T Application Hints

As shown in fig.19 operation of the L.E.D. is not inhibited during call reception unless data output via L.E.D. is programmed.

10.7 Pager Test Features

The PCF5001T provides two different test modes in which some of the decoder features can be checked. The test modes are:

Board Test mode, Pager Test mode.

The Board Test mode is entered by setting the PD input low at any time. In this mode the following features are active:

- Receiver Enable output is set high
- low level alert output is set active on ON input low
- high level alert output is set active on SR input high
- L.E.D. output and Vibrator output are set active on SK input active

Exit from the Board Test mode is done by setting the Program Data input high again.

When in Board Test mode and upon reception of a call the PagerTest mode is entered. The condition of Board

Test mode ceases when the Pager Test mode is active. In this mode the following features are active:

- only audible call alerts are abbreviated to 2 s
- Duplicate Call Suppression is disabled

Exit from the Pager Test mode occurs by disconnecting the power supply from the PCF5001T.

11. References

- /1/ CCIR recommendation 584: Standard Codes and Formats for International Radio Paging
- /2/ PCF5001T POCSAG Paging Decoder
Philips Semiconductors Data Book SC03, 1993
- /3/ UAA2050T Low Power Digital UHF Paging Receiver
Philips Semiconductors Data Book SC03, 1993
- /4/ UAA2080T Advance Digital VHF Paging Receiver
Philips Semiconductors Data Book SC03, 1993
- /5/ Richard Blohut
Theory and Practice of Error Control Codes
Addison-Wesley, 1983

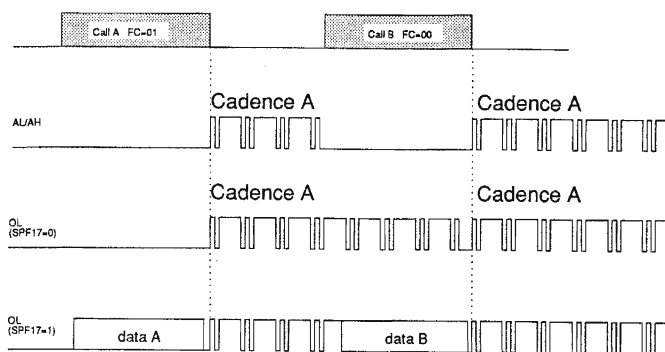


Fig. 19: Indication and Data Output on L.E.D.

CHAPTER 6

PAGER DEVELOPMENT TOOLS AND MATERIAL

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Pager development tools and materials

UAA2080H Demonstration board

Summary:

This document describes the UAA2080H pager receiver demoboards. It gives application diagrams for 173, 288 and 470 MHz, including component list and layout. A typical noise matching network for small magnetic loop antennas is given together with some simplified design formulas. A comparison is given between the battery life-time of a 2-cell supply concept and 1-cell supply concepts including a DC-DC converter. It provides a detailed tuning procedure for optimum receiver alignment, a complete set of crystal specifications and hints on PCB layout design.

1. Introduction

This application note describes demoboards of the UAA2080H pager receiver IC operating at frequencies of 172.941, 288.234 and 469.950 MHz. It is a supplement to the data sheets and Laboratory Report ETT91003 [1]. Typical performance figures of the three boards are given below. The receiver sensitivity has been measured for 3% bit error rate. When the UAA2080 is used in combination with the PCF5001 decoder or the OM4031 digital data filter, there is approximately 3 dB improvement in sensitivity, in addition to the figures mentioned below.

Pager development tools and materials

UAA2080H Demonstration board

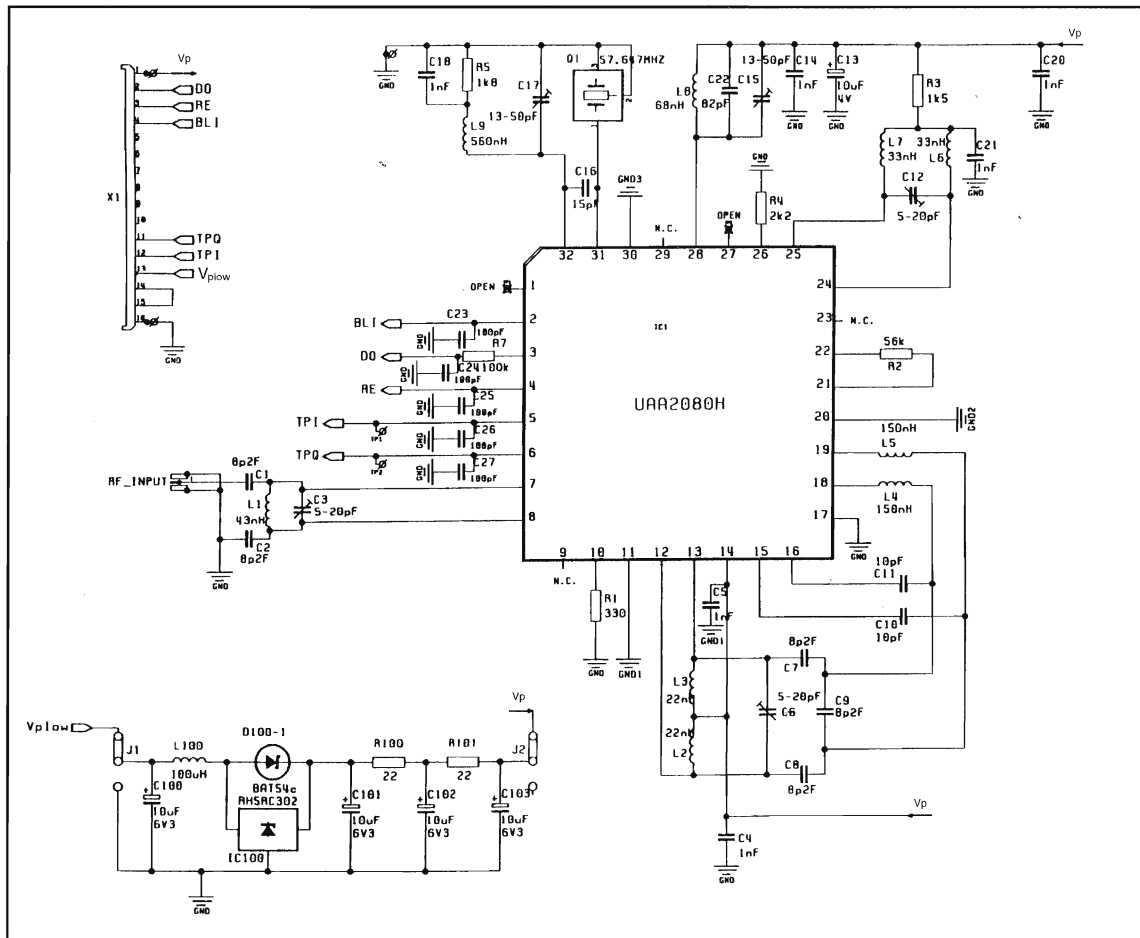


Figure 1. 172.941 MHz Receiver (OM4745)

Philips OM4745

This receiver operates at 172.941 MHz, and uses a 3rd overtone crystal of 57.647 MHz.

Sensitivity at 1200 baud and 4 kHz deviation : -123 dBm

Spurious Rejection : > 70 dB

Adjacent Channel rejection : 72 dB

Third-order intermodulation Intercept Point IP3 : -29 dBm

Pager development tools and materials

UAA2080H Demonstration board

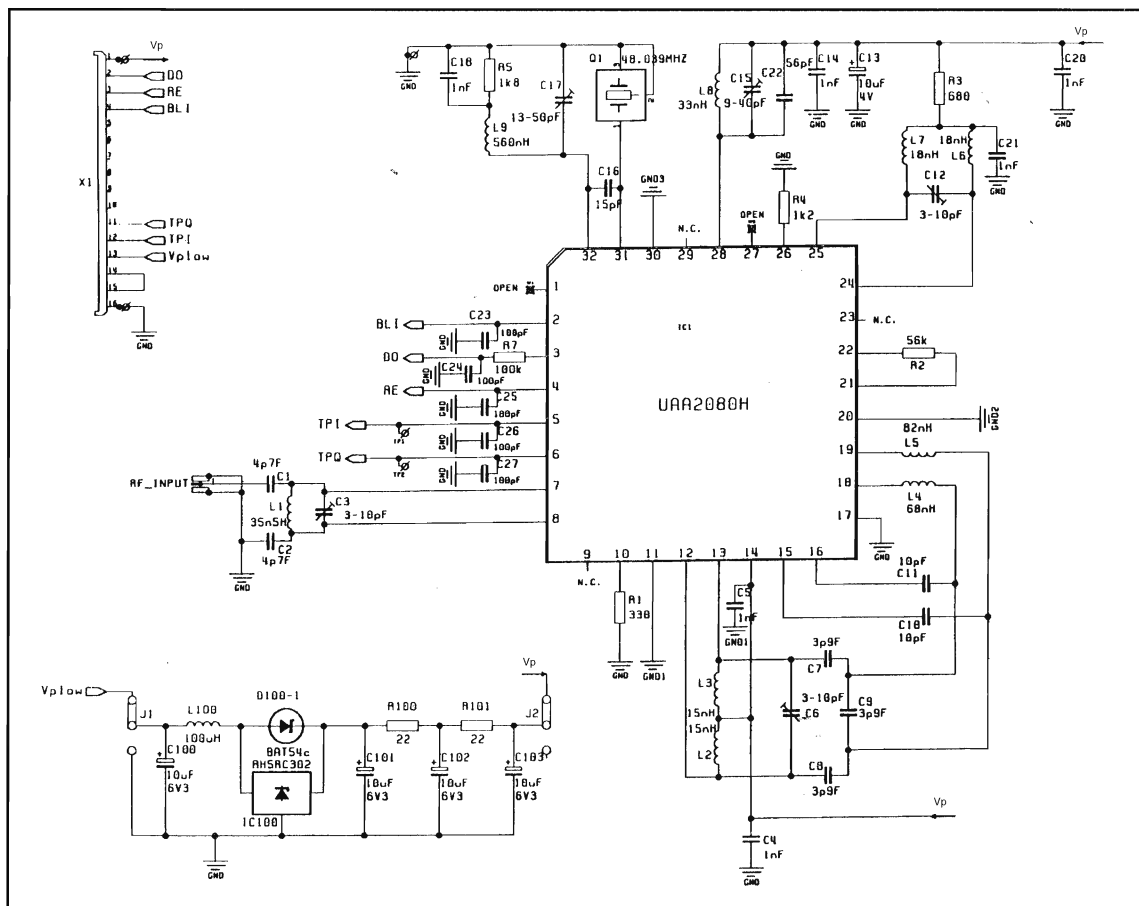


Figure 2. 288.234 MHz Receiver (OM4746)

Philips OM4746

This receiver operates at 288.234 MHz, and uses a 3rd overtone crystal of 48.029 MHz.

Sensitivity at 1200 baud and 4 kHz deviation : -123 dBm

Spurious Rejection : > 65 dB

Adjacent Channel Rejection : 72 dB

Third-order intermodulation Intercept point IP3 : -29 dBm

Pager development tools and materials

UAA2080H Demonstration board

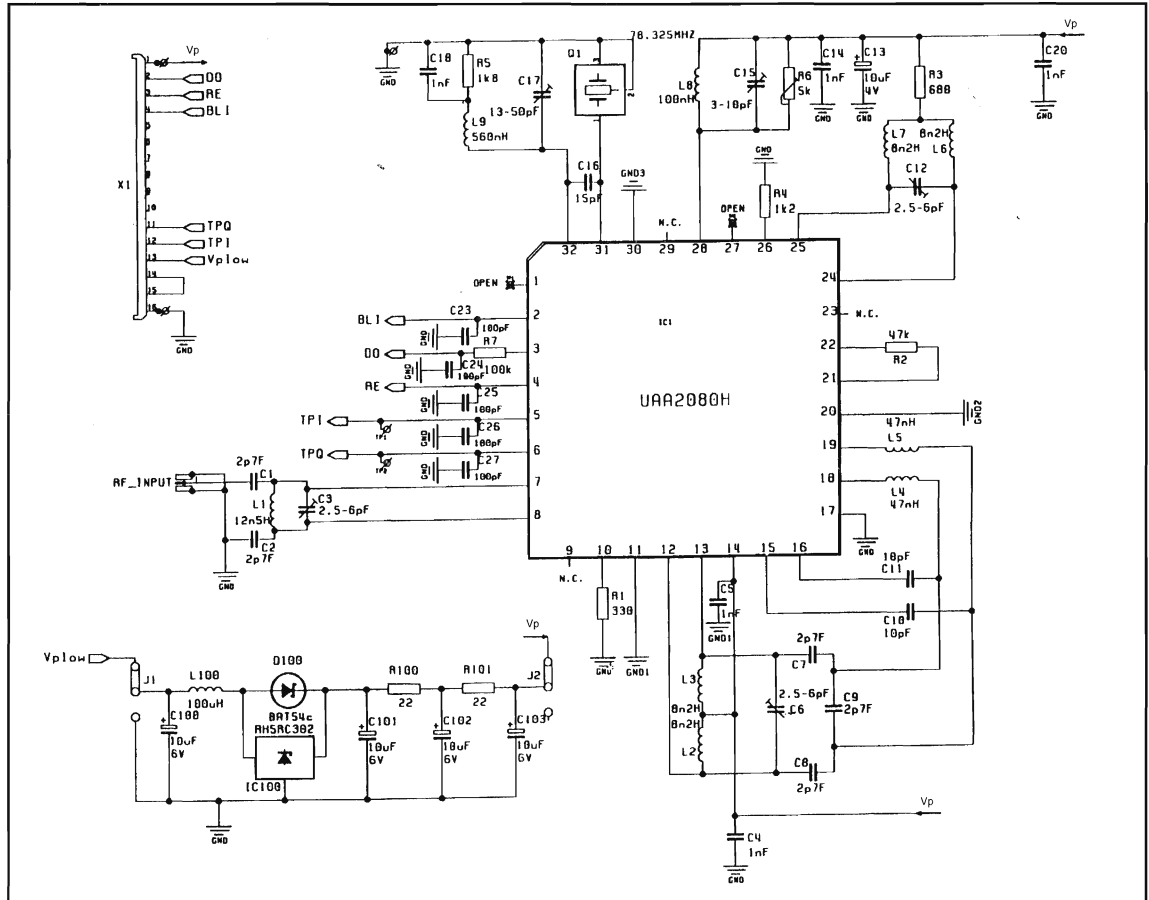


Figure 3. 469.950 MHz Receiver (OM4747)

Philips OM4747

This receiver operates at 469.950 MHz, and uses a 3rd overtone crystal of 78.325 MHz.

Sensitivity at 1200 baud and 4 kHz deviation : -121 dBm

Spurious Rejection : > 62 dB

Adjacent Channel Rejection : 72 dB

Third-order intermodulation Intercept point IP3 : -29 dBm

Philips OM4748

This is a blank printed circuit board with only the UAA2080H mounted on it. It can be used to build circuits at other frequencies.

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2. Circuit description

The UAA2080 contains a complete FSK receiver that is based on the direct conversion principle which results in a high level of integration. The front-end of the receiver, consisting of RF-stages and LO-train, is only partly integrated in order to allow application over a wide frequency range. The back-end of the receiver consisting of zero-IF stages and a demodulator is completely integrated. Figure 1, 2 and 3 depict complete application diagrams of the UAA2080H for 173, 288 and 470 MHz respectively.

2.1 50 Ω RF-input network

The input network of the UAA2080H demonstration boards has been designed at 50 Ω in order to match to RF equipment. The input network transforms the 50 Ω source resistance R_s into the optimum source resistance of the RF-amplifier R_{s_amp} of approx. 1 kΩ which gives a minimum noise figure of the amplifier. To avoid additional noise the losses in the matching network are minimized by using an air core coil. When losses and parasitics are ignored the impedance transformation gives the series reactance X_s of $C1 + C2$ (see Figs. 1, 2 and 3):

$$X_s = \sqrt{R_s * R_{s_amp}} - R_s$$

from this series reactance the values of $C1$ and $C2$ are obtained as follows:

$$C1 = C2 = 2 * \frac{1}{2 * \pi * f * X_s}$$

There is still design freedom to choose the absolute value of $L1$ and $C3$. The noise generated by the loss resistance of $L1$ is negligible if the loaded Q of the input network is at least a factor 5 smaller than the Q of $L1$ (typically >120). A practical value for Q_{loaded} is 12-18. The transformed source resistance R_{s_amp} together with the amplifier input resistance R_{in_amp} , are loading $L1$ the reactance of which is given by:

$$X_{L1} = \frac{R_{s_amp} // R_{in_amp}}{Q_{loaded}}$$

The input resistance R_{in_amp} is approx. 6k, 5k and 3k at 173, 288 and 470 MHz respectively [1]. $L1$ is tuned to resonance with trimmer $C3$ plus the transformed

capacitance C_{s_tr} and the parasitic capacitance C_{par} of the amplifier input circuit, package and PCB. The reactance of C_{s_tr} is given by:

$$X_{C_{s_tr}} = \frac{R_s * R_{s_amp}}{X_s}$$

The total parasitic capacitance C_{par} is approx. 1.5 pF. The required value of $C3$ then becomes:

$$C3 = \frac{1}{2 * \pi * f * X_{L1}} - C_{s_tr} - C_{par}$$

By grounding $C2$ the input network provides a unbalanced to balanced transformation.

Example

If $f = 470$ MHz, $R_s = 50$ and $R_{s_amp} = 1k$ then $C1 = C2 = 3.0$ pF. If $R_{in_amp} = 3$ kΩ and when the loaded Q is chosen as 20 then $X_{L1} = 37.5$ nH and $L1 = 12.7$ nH. The transformed series capacitance C_{s_tr} equals 1.5 pF. This results in a trimmer capacitance $C3$ of $9.0 - 1.5 - 1.5 = 6$ pF.

2.2 Antenna matching network

The matching network has to be optimized to the type and properties of the antenna used. In pagers most often a small magnetic loop antenna is used which is tuned to resonance with a trimmer and matched to the amplifier by means of fixed capacitors. The Q of this type of loop antenna can be high (200-500) with a real part of the antenna input impedance of typically a few tenths of an ohm [2]. Consequently, losses in the matching network due to series resistance of the capacitors are rather dominant and should be reduced as much as possible. Moreover, these losses have to be incorporated in the design of the matching network. Figure 4 gives a typical matching network. If we assume that all elements of the network have the same quality factor Q_{elem} , then the capacitor ratio $r = C_p/C_s$ is given by:

$$r = \frac{1}{2} * \left[\sqrt{\frac{X_{Lant} * Q_{elem}}{2 * R_{s_amp}}} - 1 \right]$$

in which R_{s_amp} is the parallel resistance seen by the amplifier looking into the matching network. To obtain

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noise match R_{s_amp} must be about 1 k Ω .

In order to tune the antenna to resonance the total equivalent parallel capacitance C_{tot} equals:

$$C_{tot} = \frac{1}{[2 * \pi * f]^2 * L_{ant}}$$

Because C_{tot} is realized partly by C_{tune} and partly by the matching capacitors C_s and C_p there is design freedom to optimize for practical component values. Assume that $C_{tune} = \alpha * C_{tot}$ then:

$$C_s = \frac{1 + 2 * r}{r} * \frac{1 - \alpha}{L_{ant} * [2 * \pi * f]^2}$$

in which $0 < \alpha < 1$. The amplifier input capacitance has to be incorporated in C_p .

Example

At 173 MHz a 1 x 6 cm rectangular copper wire loop has an inductance of approx. 80 nH and a Q factor of 300 which is approximately the same as the Q factor of a good trimmer and of normal SMD capacitors. For $R_{s_amp} = 1$ k Ω the capacitance ratio r becomes

$$r = \frac{1}{2} * \left[\sqrt{\frac{2 * \pi * 173e6 * 80e-9 * 300}{2 * 1000}} - 1 \right] = 1.3$$

The total parallel capacitance $C_{tot} = 10.58$ pF has to be divided over C_s , C_p and C_{tune} . If we choose $\alpha = 0.7$ then $C_{tune} = 0.7 * 10.58$ pF = 7.4 pF and $C_s = 8.78$ pF and $C_p = r * C_s = 11.46$ pF.

PCB tracks (even as short as 1 cm) between antenna and capacitors act as a transmission line. This gives a significant impedance transformation and deteriorates the matching towards the amplifier. Therefore, the matching- and trimming capacitors must be placed as close as possible to the antenna terminals.

Warning: Handsoldering small SMD capacitors with an iron that is too hot degrades the Q enormously!!

Losses of the loop antenna itself can be kept small by using a good conducting metal, like copper, with a smooth polished surface coated against corrosion. Sharp or irregular edges of strips should be avoided because

they increase skin effects.

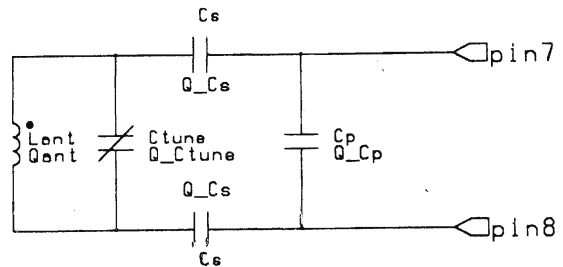


Figure 4. Antenna matching network

2.3 RF-amplifier output tank

The amplifier output tank circuit is designed for optimum power transfer towards the phase-shifter on one hand and optimum frequency selectivity (high loaded Q) on the other. Most losses are due to power dissipation in the SMD coils L2 and L3. A good compromise is obtained by choosing a loaded Q which is a factor 2 less than the Q of the SMD coils (typically 60). In this case half the loading is caused by the loss resistance of L2 and L3 and half the loading is caused by the resistive input impedance of the phase-shifter R_{ph} , which is transformed with $C7 = C8 = C9$ into a loading resistance R_{load} of:

$$R_{load} = \left[\frac{C7 + 2 * C9}{C7} \right]^2 * R_{sh} = 9 * R_{sh}$$

The phase shifter input resistance R_{sh} is approx. 250 Ω and is not a critical parameter in the design of the tank circuit.

2.4 Phase shifter

The capacitors C10 and C11 and the input resistance R_m of the mixer in the I-path provide a phase shift of +45° if the reactance $X_{C10} + X_{C11}$ is equal to the mixer input resistance R_m . The coils L4 and L5 and the mixer input resistance R_m in the Q-path provide -45° phase shift if the total reactance $X_{L4} + X_{L5}$ is equal to R_m . R_m is approx. 270, 230 and 180 Ω for 170, 288 and 470 MHz respectively. Especially at UHF this phase shifting network is rather sensitive to strays in the PCB. In practice C10 and C11 and/or L4 and L5 have to be optimized such that the phase difference between I and

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Q is $90^\circ \pm 10^\circ$ and their amplitudes are the same within 2 dB.

2.5 Oscillator

The colpitts oscillator is forced to oscillate at the third-overtone of the crystal by means of a mode selector coil L9. The DC-biasing is provided by the 1.8 k Ω resistor R5 which is optimized for minimum power consumption on one hand and reliable start-up on the other hand for the set of crystal specifications given on pages 14-16. The oscillator operates in class C. Therefore, its output current (pin 28) is peaked and contains strong harmonics. The output tank circuit is tuned to either the fundamental (173 MHz) or second harmonic (288, 470 MHz).

2.6 Frequency multiplier

The frequency multiplier is driven single ended with a relatively strong signal switching the multiplier stage. The balanced output current (pin 24 and 25) contains strong odd harmonics. The output tank circuit is tuned to the third harmonic which is equal to the receiving frequency. The output tank is internally connected to the LO-inputs of the mixers. The resistor R3 provides a DC voltage drop of approximately 0.3 V which is required for optimal DC biasing of the mixers.

2.7 DC-DC Converter

The demoboard offers the possibility to supply the UAA2080H via a DC-DC converter which can be switched on and off by means of jumpers. The converter used is of the boost type and has an efficiency of approx. 75% with the components used on the demoboard. The RC filter at the converter output suppresses LF and MF frequency components that are generated by the converter.

3. Power supply concepts

The UAA2080 can best be supplied by two 1.5 V batteries. This is simple and reliable compared to a single cell supply in combination with a DC-DC converter. Moreover, in a 2-cell concept the relatively small total current consumption of 2.7 mA results in a long battery life. However, the additional weight and extra space required for a second battery can be avoided by using a

DC-DC converter to supply the receiver.

3.1 2-cell supply concept

Figure 5. depicts a 2-cell supply concept for the UAA2080H in combination with the PCF5001 decoder. To suppress LF-interference from the digital circuitry to the susceptible receiver the batteries can best be connected as a star point. Both the receiver and decoder should be LF decoupled by a series resistor and a capacitor close to the IC.

In a direct conversion receiver the LF signal amplitude at the mixer outputs is small because most of the gain is provided by the LF stages. Due to the non-ideal power supply rejection, LF signals that are present on the supply line are being fed towards the internal signal path and reduce the receiver sensitivity. To prevent desensitization the power supply ripple at frequencies between 300 Hz and 10 kHz should be less than a few mVpp. Most often a RC or LC LF decoupling network in the supply line is necessary and sufficient to suppress interference from digital circuitry. Table 1. shows, for different modulating frequencies of the supply line, the signal amplitudes that give 3 dB sensitivity degradation of the receiver.

f_{mod} [Hz]	A_{fmod} [mVeff]
100	135
300	18
1k	5.6
3k	4.0
10k	19
30k	50
100k	107

Table 1. Supply interference giving 3 dB sensitivity reduction

Data-out contains LF frequency components which might interact with the receiver via the supply lines. Therefore, the data-out return path should be low-ohmic and preferably routed close to the data line.

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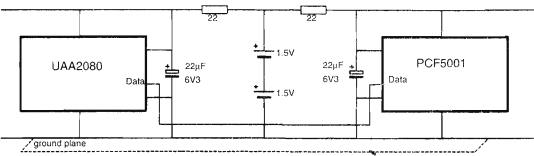


Figure 5. 2-cell supply concept for UAA2080 and PCF5001

3.2 1-cell supply concept

For a small size pager a single cell supply concept may be preferred over a two cell concept. In this case, the nominally 1.5 V battery voltage has to be enhanced by means of a DC-DC converter to supply both the receiver and decoder. The boost type converters are commonly used for this purpose. The output voltage of these converters is regulated by means of a comparator with hysteresis. The ripple caused by this stabilization mechanism has to be filtered by either an LC or RC network otherwise the receiver sensitivity will reduce. The coil L1 (TDK_TSL0707) is selected for optimum efficiency. A magnetically shielded coil might be attractive because it gives less radiation and has smaller dimensions, but it reduces the converter efficiency more than 10 %. The schottky diode has to be selected for a minimum forward voltage drop. Here, a PRLL5817 or BAT54 is a good choice. For optimum converter efficiency the filter resistors R1 and R2 has to be small compared to the effective load resistance. A good choice is 10-22 Ω. The bias current of the receiver is independent of the supply voltage. Thus, to minimize the power consumption of the receiver, the converter output voltage must be kept as low as possible (e.g. 2 V). This provides maximum battery life-time.

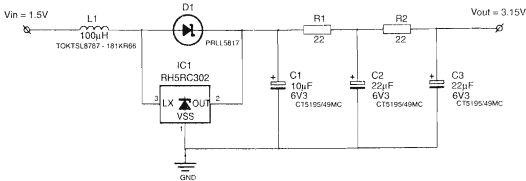


Figure 6. 1-cell supply concept with a 3 V RH5RC302 DC-DC converter

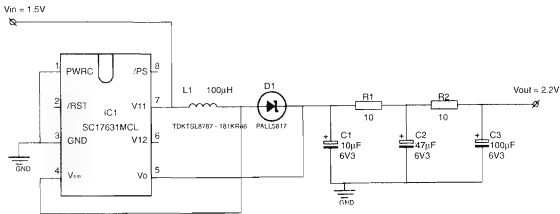


Figure 7. 1-cell supply concept with a 2.2 V SC17631MCL DC-DC converter

3.3 Battery life-time

In pager applications the total battery life-time is a major system parameter. Battery life-time depends on the power consumption of the receiver and digital part but also on the power supply concept used. Three examples corresponding with the two supply concepts above have been worked out in more detail. It is assumed that battery voltage is constant during its life-time and that all bias currents are independent of the supply voltage.

Moreover, it is assumed that:

battery voltage	U _{bat} = 1.3 V
battery capacity	C _{bat} = 1000 mAh
receiver current	I _{rec} = 2.7 mA
current of digital part	I _{dig} = 0.2 mA
receiver on/off duty cycle	d = 0.08
DC-DC converter efficiency	η = 0.70
converter output voltage	U _{out} = 2.2 or 3 V

2-cell supply concept

For the 2-cell supply concept the battery life-time LT_{bat} can be calculated with the formula given below.

$$LT_{bat} = \frac{C_{bat}}{d * I_{rec} + I_{dig}}$$

For the conditions given above the battery life-time is 2404 h.

1-cell supply concept;

For a 1-cell supply concept the total power consumption of receiver and digital part is of interest because the converter transfers this power, with some loss, from the battery to its load.

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$$LT_{\text{bat}} = \frac{C_{\text{bat}}}{I_{\text{bat}}} = \frac{C_{\text{bat}}}{\frac{P_{\text{load}}}{n * U_{\text{bat}}}} = \frac{n * U_{\text{bat}} * C_{\text{bat}}}{U_{\text{out}} * (d * I_{\text{rec}} + I_{\text{dig}})}$$

According to this formula the battery life-time for a 2.2 V and 3 V converter is 994 h and 730 h respectively. Of course, in a single cell supply concept only half the amount of energy is available. Due to the power dissipation of the DC-DC converter the life-time reduces even further. However, by using a converter with an output voltage lower than the voltage of two batteries, the power loss in the converter is partly compensated:

3.4 Measuring the DC-DC converter efficiency

It is not possible to measure the DC-DC converter efficiency directly using a mA-meter, because the current drawn from the battery has both a direct and a pulsed component.

It is recommended to connect a measuring resistor R_m of $\leq 100 \Omega$ between the pins of jumper J1 in the ON position. Also, a measuring capacitor C_m of $\geq 680 \mu\text{F}$ must be connected in parallel with C100, e.g. between the pins of jumper J1 in the OFF position. The jumper itself must of course be removed for this measurement.

The input current of the converter I_{bat} is obtained from the voltage V_m across R_m , while the input voltage V_{bat} is measured across C_m :

$$I_{\text{bat}} = V_m / R_m$$

The output current I_{out} can be measured by connecting a mA-meter across the pins of jumper J2 in the ON position (with the jumper removed). The output voltage V_{out} is measured across capacitor C103.

The converter power efficiency η now becomes:

$$\eta = P_{\text{out}} / P_{\text{bat}} \quad \text{with:}$$

$$P_{\text{out}} = V_{\text{out}} * I_{\text{out}}$$

$$P_{\text{bat}} = V_{\text{bat}} * I_{\text{bat}} = V_{\text{bat}} * V_m / R_m$$

4. Layout design guidelines

At VHF and, especially, UHF frequencies the layout and component placement have to be chosen properly in order to obtain optimum performance with respect to sensitivity and spurious rejection. PCB tracks have to be short. Decoupling capacitors must be well placed for optimum decoupling and RF-coupling between the oscillator train and magnetic loop antenna has to be minimized. On pages 12 and 13 of Report No. ETT91003 "UAA2080T VHF/UHF Paging Receiver, Features and Applications" guidelines for PCB layout design are given. An overview of the most important design aspects are mentioned below.

4.1 Ground plane

The bias currents of the UAA2080 are stabilized by means of a bandgap voltage that refers to ground. Therefore, preferably all ground connections should be at the same potential both for DC and AC. This includes the ground pins of the IC as well as ground points of external components. In order to minimize RF-voltage drops between different grounds these grounds can best be connected to each other by means of a ground plane.

4.2 RF-decoupling of power supply

The oscillator, operating in class-C, causes relatively strong current peaks in the supply line. In order to minimize the current through the ground plane the decouple capacitor C14 should be placed close to the tank circuit L8, C15 and the oscillator ground connection of C15, R5, C18 and the crystal.

The frequency multiplier is driven asymmetrically. Consequently, a common-mode current flows through C21 and/or R3 via R4 to ground. Therefore, the grounded terminal of C21 can best be placed close to the ground connection of R4.

The capacitor C5 decouples the main supply of the UAA2080H. C4 decouples the supply of the RF-amplifier. Its ground connection can best be kept close to the ground connection of R1.

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4.3 LO pick-up

In a direct conversion receiver concept the frequency of the LO mixer injection signal is equal to the receiving frequency. The loop antenna and/or input network inevitably picks up some of the LO-signal. If the coupling between the oscillator/multiplier and RF-input is too strong the receiver sensitivity degrades. Therefore, the orientation of L6 and L7 can best be chosen such that coupling with the antenna is minimal. Moreover, both coils can best be placed side by side such that their magnetic fields cancel.

The antenna input circuit and the oscillator train are best kept on opposite sides of the IC.

4.4 Parasitic inductance

The inductance of a PCB track is typically 1 nH/mm. Because the required inductances in the tank circuits are, at UHF, in the order of 10 nH, the PCB tracks of these tank circuits should not be longer than a few mm. For optimum spurious rejection it is better to have some parasitic inductance present in series with a coil than in series with a capacitor. Therefore, the trimmers C6 and C12 should be placed as close as possible to the IC pins while L2, L3 and L6, L7 can be placed somewhat further away.

5. Receiver Tuning Procedure

a) Coarse tuning of the crystal

The three application circuits are to be tuned as follows. The signal generator (50 Ω source) is connected to the RF input of the receiver board, and the frequency is kept at the nominal receiver frequency. The RF signal amplitude is initially kept very large, at about 50 mV. The audio IF signal at TPI or TPQ is displayed on an oscilloscope (time base at 200 μ s/division). The crystal is tuned (by C16 or C17) till a signal of approximately 2-4 kHz is observed. The amplitude could be very small, so the voltage setting on the oscilloscope should be 1-5 mV/division. If a variable resistor R6 is used for damping, then it must be kept at the maximum value.

b) Tuning all tank circuits

After the coarse tuning of the crystal, the receiver's LO frequency is within a few kHz of the correct frequency, and therefore all the tank circuits can now be tuned. All other tuning capacitors are carefully adjusted in order to maximise the IF amplitude. The easiest sequence of trimming is: C15, C12, C6 and then C3. The signal generator level is decreased and adjusted so that the IF amplitude is always less than 25 mV (this avoids gain compression in the IF signal path). For the 470 and 288 MHz applications, C12 will have a large range over which the IF amplitude remains maximum. This is due to overdrive signal level at pin OSC. Proper tuning of C12 is given below under the section on Spurious Rejection.

c) Fine tuning of the crystal

The crystal is again tuned till there is no signal displayed, or the signal frequency is very small (this occurs when the LO frequency is nearly equal to the signal generator frequency, so that the difference in frequency which is the IF, is very small, say within 100 Hz). Under this condition, turning the tuning capacitor (C16 or C17) very slightly in either direction from the optimal position, increases the IF frequency.

The oscilloscope time-base is increased to 1 ms/division, and the crystal is carefully further fine-tuned to display the lowest possible frequency on the oscilloscope. At this stage, the LO has been tuned to the nominal receiver frequency, with an error equal to the frequency of the IF signal that is displayed on the oscilloscope.

d) Spurious Rejection

The IF signal is made 4 kHz (deviation frequency) at 20 mV amplitude by changing the signal generator frequency by 4 kHz from the nominal receiver frequency, and adjusting its attenuation. Next, R6 is reduced so that the IF amplitude decreases by half. This removes the overdrive at pin OSC, thus enabling the proper tuning of C15, which is now tuned again, along with C12, to maximise the IF level. R6 is then made maximum and the signal generator adjusted to give 20 mV IF level. R6 is reduced till the IF amplitude drops to 17 mV. This ensures that the LO level is just sufficient to switch the mixers, and not larger, as that would degrade spurious rejection.

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With this final adjustment, the receiver is fully tuned and its spurious rejection optimal. Reducing the IF level even further would result in an even better spurious rejection, with a slight decrease in sensitivity. In circuits that do not use the damping resistor R6, the IF level is finally reduced from 20 mV to 17 mV by detuning C15.

6. Component Description

A complete list of components used for each demoboard is given on pages 23-32 at the end of this document. Except for the DC-DC converter part all components are the same as for the UAA2080T (SO28 package) application diagram [3]. However, an additional resistor R7 (22 k-100 k) in series with pin DO is **recommended** in order to avoid de-sensitization that might occur due to current peaks caused by capacitive loading. The RF-decoupling capacitors C23-C27 are **optional** and only required when strong interfering RF signals are being expected.

Crystals

The crystal oscillator is optimized for a relatively low bias current [1, page 15-40]. This poses rather severe requirements on the motional resistance of the crystals. A complete specification for the crystals is given on the following pages. At the cost of yield a somewhat relaxed specification of the motional resistance may be used.

6.1 78.325 MHz Crystal Specifications

(All parameters to be measured with metallic holder and one lead grounded)

Application: 469.950 MHz (2 x 3 x 78.325 MHz)

Loaded Parallel Resonant Frequency, f_L : 78.325 MHz

Load Capacitance, C_L : 8 pF

Tolerance on C_L : ± 0.5 pF

Tolerance of f_L :

Calibration: ± 5 ppm at 25 °C

Total (temperature + aging, see Notes):

± 4.2 ppm over -10 °C to +55 °C (@ 20 kHz TX channel width, ± 4 kHz deviation)

± 5.3 ppm over -10 °C to +55 °C (@ 25 kHz TX channel width, ± 4.5 kHz deviation)

Overtone: third

Motional Resistance, R_1 : less than 20 Ω

Static Capacitance, C_0 : less than 6 pF

Pullability, F:

Definition: $F = (f_L - f_R)/f_R = C_1/[2(C_L + C_0)]$

in [ppm]

where f_R = unloaded series resonance frequency

C_1 = motional capacitance

Requirement: 55 ppm $\leq F \leq 70$ ppm when $C_L = 8$ pF

Holder: HC-52-SMD, with ground clamp or connection for metallic holder

Spurious rejection:

$R_N/R_1 \geq 2$ from $f_L/2.5$ to $2f_L$

where R_N is the dynamic resistance at the spurious frequency

Notes:

- The total frequency tolerance is based on a 3 dB loss of sensitivity of the UAA2080 due to frequency offset between transmitter and receiver.
- Aging requirements depend on the interval between service adjustments of the paging receiver. System aging is mainly determined by aging of the crystal, the tuning capacitor and the stray capacitance of the printed circuit board.

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6.2 48.039 MHz and 57.647 MHz Crystal Specifications

(All parameters to be measured with metallic holder and one lead grounded)

Applications: a) 172.941 MHz (3 x 57.647 MHz)
b) 288.234 MHz (2 x 3 x 48.039 MHz)

Loaded Parallel Resonant Frequency, f_L :

a) 57.647 MHz b) 48.039 MHz

Load Capacitance, C_L : 8 pF

Tolerance on C_L : ± 0.5 pF

Tolerance of f_L :

Calibration: ± 5 ppm at 25 °C

Total (temperature + aging, see Notes on previous page):

a. ± 11.5 ppm over -10 °C to +55 °C (@ 20 kHz channel width, ± 4 kHz deviation)

± 14.4 ppm over -10 °C to +55 °C (@ 25 kHz channel width, ± 4.5 kHz deviation)

b. ± 6.9 ppm over -10 °C to +55 °C (@ 20 kHz channel width, ± 4 kHz deviation)

± 8.7 ppm over -10 °C to +55 °C (@ 25 kHz channel width, ± 4.5 kHz deviation)

Overtone: third

Motional Resistance, R_1 : less than 30 Ω

Static Capacitance, C_0 : less than 5 pF

Pullability, F:

Definition: $F = (f_L - f_R)/f_R = C_1/[2(C_L + C_0)]$
in [ppm]

where f_R = unloaded series resonance frequency
 C_1 = motional capacitance

Requirement: 50 ppm $\leq F \leq 70$ ppm when $C_L = 8$ pF

Holder: HC-52-SMD, with ground clamp/connection for metallic holder

Spurious rejection:

$R_N/R_1 \geq 2$ from $f_L/2.5$ to $2f_L$

where R_N is the dynamic resistance at the spurious frequency

16 pin flat cable Connector

Pin # Signal

- 1 Positive battery supply (>1.9 V); DC-DC converter output when enabled
- 2 Data output (pin 3 of UAA2080H)
- 3 Receiver enable input (pin 4 of UAA2080H)
- 4 Battery low indicator output (pin 2 of UAA2080H)
- 5 -
- 6 -
- 7 -
- 8 -
- 9 -
- 10 -
- 11 TPQ (pin 5 of UAA2080H)
- 12 TPI (pin 6 of UAA2080H)
- 13 Low supply voltage (>0.9 V) to be used in combination with DC-DC converter
- 14 Shorted to pin 15 of connector (compatibility with OM4706 decoder board)
- 15 Shorted to pin 14 of connector (compatibility with OM4706 decoder board)
- 16 Ground

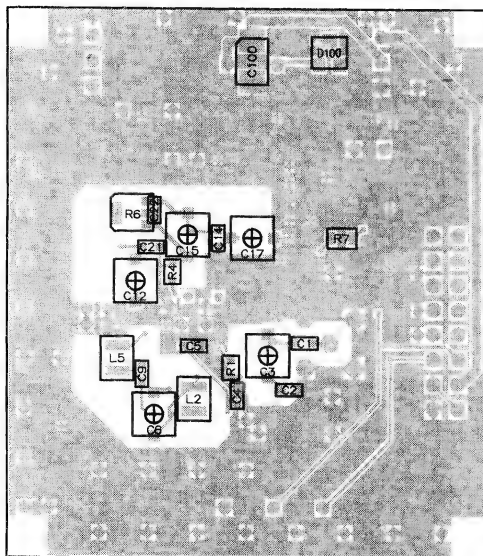
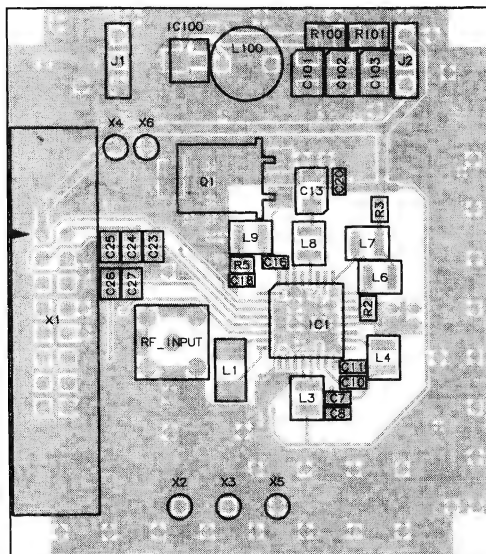
The flat cable connector of the 3 demoboards is pin compatible with the PCF5001 decoder demoboard OM4706. The two batteries on the OM4706 are used to supply both the decoder and the receiver IC. However, with a few minor modifications of the OM4706 both boards can be supplied by only one battery and the DC-DC converter on the receiver board.

Modifications for 1-cell supply of OM4706 and OM4745/46/47:

- 1- remove battery B1.
- 2- cut, at backside, the PCB track from connector pin13 to LED1.
- 4- connect positive side of battery socket B2 with connector pin13
- 3- switch on J1 and J2 of the receiver board

UAA2080H Demonstration board

Top Side



Bottom Side

Development tools and materials

OM4706 Decoder demonstration board

1. Introduction

1.1 Short description

The PCF5001T is a fully integrated low power decoder and pager controller. It decodes the CCIR Radiopaging Code No.1 (POCSAG Code) at 512 and 1200 bit/s data rates. The PCF5001T supports two basic modes of operation:

- In Alert-Only-Pager mode only a minimum number of external components are required to build a complete tone-only pager. Selection of operating states ON, OFF or SILENT is done using a slider switch interface.
- In Display-Pager mode the state input logic is switched to a bus interface structure. Received calls and messages are transferred to an external microcontroller via the serial microcontroller interface. A built-in voltage converter with increased drive capabilities can supply doubled supply voltage output, and appropriate logic level shifting on microcontroller interface signals is provided.

Upon reception of valid calls one of eight different call cadences is generated; upon status interrogation status indication tones make the current state of the decoder available to the user.

On-chip non-volatile 114 bit EEPROM storage is provided to hold up to four user addresses, two frame numbers and the programmed decoder configuration.

Synchronization to the input data stream is achieved using the improved ACCESS algorithm, which allows for data synchronization and re-synchronization without preamble detection while minimising battery power consumption by receiver power control. One of four error correction algorithms is applied to the received codewords to optimize the call success rate.

The PCF5001T is fabricated in SACMOS technology to ensure low power consumption at low supply voltages.

1.2 List of features

- wide operating supply voltage range (1.5 V to 6.0 V)
- very low supply current (60 μ A typ. with 76.8 kHz crystal)
- extended temperature range -40 °C to +85 °C
- decodes CCIR Radiopaging Code No.1 (POCSAG-Code)
- programmable call termination conditions
- 512 and 1200 bit/s data rates
- 2400 bit/s data rate*
- improved ACCESS synchronization algorithm
- supports 4 user addresses in two independent frames
- eight different alert cadences
- directly drives magnetic or piezoceramic bleeper
- high level alert requires only a single external transistor
- optional vibrator type alerting
- silent call storage up to eight different calls
- repeat alarm facility
- programmable duplicate call suppression
- interfaces directly to UAA2033T, UAA2050T and UAA2080T digital paging receivers
- programmable receiver power control for battery economy
- on-chip non-volatile EEPROM storage
- on-chip voltage converter with improved drive capability
- serial microcontroller interface for Display Pager applications
- optional visual indication of received call data using a modified RS 232 format
- level shifted microcontroller interface signals
- alert on low battery
- optional out of range indication

* with restricted voltage range (see data sheet PCF5001T)

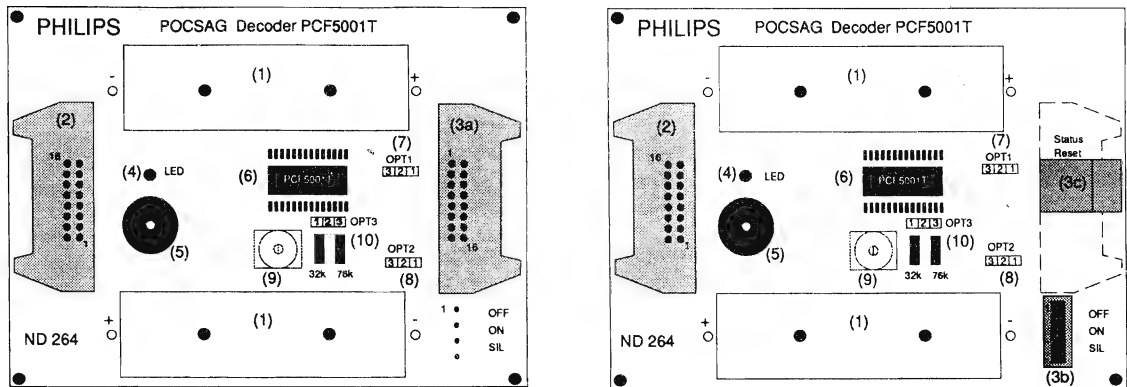
2. Decoder Module Hardware (PCF5001T)

2.1 Battery Socket (1)

Two Batteries (size AA) inserted into these sockets are used to provide the main power supply for the decoder module.

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a) Display Pager Configuration

b) Alert-Only Pager Configuration

Fig. 1: PCF5001T Decoder Module

2.2 Interface Connector (2)

To allow operation of the decoder module either the test and program unit or the receiver module has to be connected via this connector. The decoder module is switched off otherwise.

All necessary signals are available at this connector to allow programming and operation of the decoder module.

- PIN 1: VDD, main power supply, batteries positive side
- PIN 2: RDI, POCESAG data input (PCF5001T DI input)
- PIN 3: REN, receiver power control output (PCF5001T RE output)
- PIN 4: SR, Status/Reset input (PCF5001T SR input)
- PIN 5: N.C.
- PIN 6: PRCL, program clock input (PCF5001T PS input)
- PIN 7: PRDO, program data output (PCF5001T PD in-/output)
- PIN 8: PRDI, program data input (PCF5001T PD in-/output)

- PIN 9: N.C.
- PIN 10: POFF, display unit power control
- PIN 11: N.C.
- PIN 12: N.C.
- PIN 13: VDD, main power supply, batteries positive side
- PIN 14: VBAT, main power supply, batteries negative side
- PIN 15: VS, negative power supply decoder circuit (PCF5001T VS)
- PIN 16: VS

2.3 Display Unit Connector (3a)

If the decoder module is configured as a Display Pager this connector is used for interfacing the decoder module and the display module.

The following interface signals are available:

- PIN 1: VDD, main power supply, batteries positive side
- PIN 2: VDD
- PIN 3: ON, status ON input (PCF5001T ON input)
- PIN 4: OF, status OFF input (PCF5001T OF input)

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PIN 5:	SK, status SILENT input (PCF5001T SK input)
PIN 6:	DO, message data output (PCF5001T DO output)
PIN 7:	DS, message data strobe output (PCF5001T DS output)
PIN 8:	AI, alarm input (PCF5001T AI input)
PIN 9:	BL, battery low indication output (PCF5001T BL output)
PIN 10:	FL, frequency reference output (PCF5001T FL output)
PIN 11:	VP, voltage converter output (PCF5001T VP output)
PIN 12:	POFF, display unit power control
PIN 13:	IE, interface enable input (PCF5001T IE input)
PIN 14:	OR, Out-of-Range Output (PCF5001T OR output)
PIN 15:	VS, negative power supply decoder circuits
PIN 16:	VS, (PCF5001T VS input)

2.4 Slider switch (3b)

A three position slider switch forms the status control of an Alert-Only Pager.

Position OFF:	Pin ON is switched to ground (VS)
Position ON:	Pin SK is switched to ground (VS)
Position SILENT:	Pin's ON & SK are left open (internal pull-up resistances)

2.5 Status/Reset (3c)

For resetting of alert cadences or status interrogation the Status/Reset push-button is used. Switching input SR high for a period greater than the switch debounce time activates the status/reset function.

2.6 L.E.D. Indicator(4)

The L.E.D. indicator provides visible identification of:

- Call Receipt
- Repeat Alert
- Out-of-Range indication
- Alarm input
- Call data output
- Start-up alert indication

2.7 Acoustic Alert Indicator (5)

The PCF5001T drives an acoustic alerter as a means for:

- Call Alert indication
- Repeat Alert indication
- Status Alert indication
- Battery Level Low indication
- Alarm input activation
- Start-up Alert indication

2.8 Decoder IC Pin Allocation (6)

PIN No	Allocation	Description
1	VP	voltage converter negative output
2	CN	voltage converter shunt capacitor - negative
3	CP	voltage converter shunt capacitor - positive
4	VD	main positive supply input (common)
5	DI	serial data input
6	BS	battery sense input
7	PD	programming data input
8	PS	programming strobe input
9	X1	oscillator input
10	X2	oscillator output
11	TS	scan pass test enable input, always low
12	AH	alert high level output
13	OL	LED output
14	RE	receiver enable output
15	AL	alert low level output
16	OM	motor (vibrator) output
17	VS	main negative supply input
18	TT	test mode enable input (EEPROM)
19	IE	interface enable Input
20	SK	silent status / mute input
21	SR	status alert / reset input
22	ON	ON status / ON-OFF input
23	AI	alarm input
24	BL	battery low output
25	OR	Out-of-Range output
26	DO	serial data output
27	DS	serial data strobe output
28	FL	frequency reference output

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2.9 Interface Enable (OPT1) (7)

In Alert-Only Pager mode the IE input shall have no effect, however it is necessary to connect the IE input to a valid logical level (VDD). Jumper position is 1-2 for Alert-Only Pager mode.

In Display Pager mode the IE input is activated by an externally connected microcontroller. The Jumper position is 2-3 or left open.

2.10 Voltage Converter (OPT2) (8)

When the Voltage Converter Enable is deactivated the voltage doubler circuit shall be made high-impedance such that the interface supply, Vpr, may be driven externally to reference the level shifters. Jumper position 2-3 for an external power supply.

In Alert-Only Pager applications in which the interface is not required the Vpr supply must be externally short-circuited to the main Vss supply. Jumper position 1-2 for Alert-Only Pager mode.

2.11 Oscillator Tuning Capacitor (9)

This capacitor can be used for tuning the crystal oscillator frequency.

2.12 Oscillator Frequency (OPT3) (10)

The PCF5001T operates at the following signalling speeds dependent upon setting of the Special Programmed Function Bits and connection of the appropriate crystal for the main oscillator.

Bit Rate	SPF02	SPF03	Crystal	Jumper Position Opt3
512 bps	0	0	32768 Hz	1 -2
512 bps	0	1	76800 Hz	2-3
1200 bps	1	X	76800 Hz	2-3

2.13 Details on Decoder Module Hardware

The circuit diagram for the PCF5001T decoder and the PCB layout can be found in the Appendix A1. The decoder module can either be configured as an Alert-Only Pager or as a Display Pager.

For the Alert-Only Pager module, see fig.1b, a slider switch with three positions determines the status of the decoder. A push-button is used to do the Status/Reset function.

On the Display Pager module, see fig.1a, slider switch and push button are omitted, in this case a connector is used to combine decoder module and display unit

The voltage converter capacitor between pin2 and pin3 is only present if the voltage doubler of the PCF5001T shall be used, otherwise these pins are left open.

The interface connector provides signals for testing and programming purposes. To allow programming of the decoder module with the test and program unit the negative supply voltage is passed through the interface connector ST1 pin 14 (VBAT) and pin 15 (VS). To program the internal EEPROM of the PCF5001T it is necessary to have a supply voltage of 5 V between pin4 (VD) and pin 17 (VS) of the decoder IC. The test and program unit is able to produce VDD = 5 V during programming the EEPROM. During verifying and testing the decoder module is supplied from the two batteries (VDD = 3 V). If the decoder module is connected to the receiver module the supply voltage will be switched on as long as the decoder is connected with the receiver module.

3. Test and Program Unit Hardware

POCSAG Code generation and programming of the decoder circuit is easily done with the test and program unit.

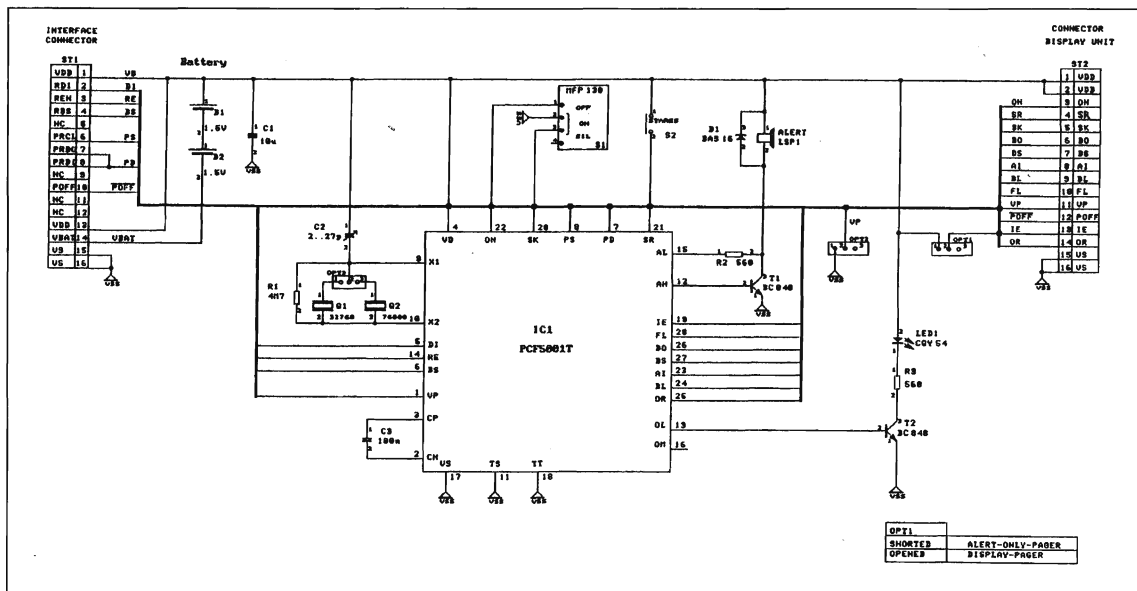
The PCF5001T provides three EEPROM arrays totalling 114 bits for the storage of four USER addresses, address enable plus storage of 32 special programmed function bits for pager configuration. The three EEPROM arrays are programmed within a special program mode during which the supply voltage must be at least VPG = 5 V.

For more information on the test and programming hardware please refer to the next chapter: OM4718 Pager test and programming.

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4. Circuit diagram



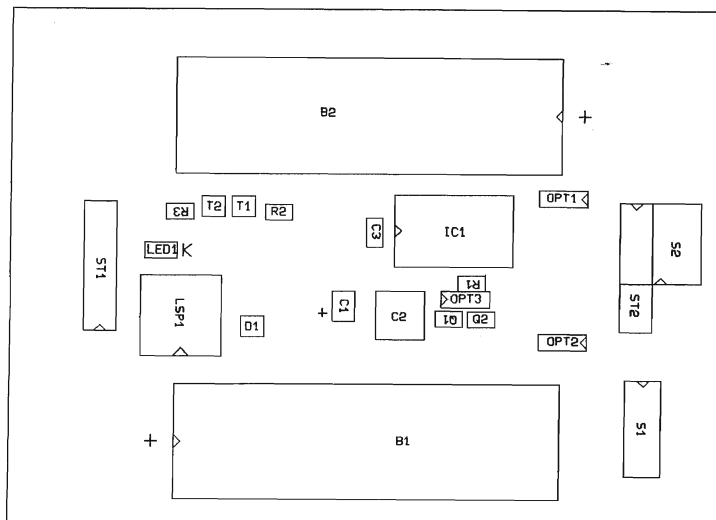
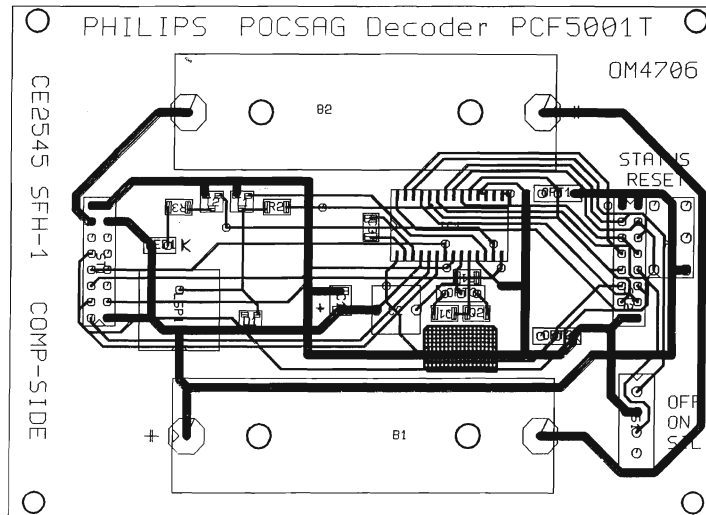
5. Components list

#	Part	Form	Component type	#	Part	Form	Component type
1	B1	DBAT1	1.5V	14	OPT1	DNET3	
2	B2	DBAT1	1.5V	15	OPT2	DNET3	
3	C1	ELCO267	10uF/4V	16	OPT3	DNET3	
4	C2	CRU2S	2..27p	17	Q1	R1206	32768
5	C3	C1206	100NF	18	Q2	R1206	76800
6	D1	SOT23	BAS16	19	R1	R1206	4M7
7	IC1	SO28F	PCF5001T	20	R2	R1206	560E
8	L1	LOCH		21	R3	R1206	560E
9	L2	LOCH		22	S1	DNET4	MFP130
10	L3	LOCH		23	S2	DTAST1	
11	L4	LOCH		24	ST1	D3M16	ANSLEY HAAKS-16P
12	LED1	CRM2B	HMP1385 (RED)	25	ST2	D3M16	ANSLEY HAAKS-16P NIETM
13	LSP1	BUZZER	QMB111	26	T1	SOT23	BC848
				27	T2	SOT23	BC848

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6. Board Lay-Out



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OM4718 Test and programming unit

1. The Demonstration System

The Pager Demonstration System originally was designed to show a typical pager application with the UAA2033T VHF Paging Receiver and the PCA5000T POCSAG Paging Decoder. Since its introduction a number of other pager circuits have been developed: the UAA2050T UHF/VHF Pager Receiver, the PCF5001T POCSAG Decoder and recently the UAA2080T UHF/VHF Pager Receiver. For all these products demonstration boards have been made which fit into the original concept.

2. Introduction to Concept

By combining a receiver with a decoder and a few additional components a beep-only (alert-only) pager can be built. The decoder then serves as pager controller (message decoding, keyboard interface, alert signal generation). For a display pager application a microcontroller interface is provided by the decoder to allow for easy control and call information transfer to the microcontroller of a display section.

A modular structure has been chosen to allow for quick and easy exchange of modules. The module configuration is shown in fig. 2-1.

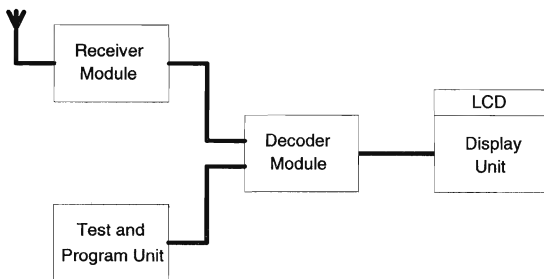


Fig. 2.1 Paging Demonstration System

The paging demonstration system comprises of four modules:

- **Receiver Module** (UAA2033T, UAA2050T, UAA2080T)
- **Decoder Module** (PCA5000(A)T, PCF5001T)
- **Display Unit**
- **Test and Program Unit.**

Receiver Module

The receiver module converts the FSK-modulated RF input signals into a binary data stream, which is then passed to the decoder module. The UAA2033T/2050T receivers operate according to the "Offset Receiver" principle, while the UAA2080T uses the "Direct Conversion" or "Zero-IF" method. The receive frequency is determined by a crystal oscillator.

Decoder Module

The decoder operates on the data stream presented by the receiver. The decoding algorithm is based on the rules of the POCSAG transmission code (i.e. CCIR Radiopaging Code No.1). If the decoder detects a valid call, appropriate call alert cadences will be generated and call information is output via the microcontroller interface. It also controls the power-down mode of the receiver: depending on the synchronization state of the decoder it only switches on the receiver when needed. This is possible because of the POCSAG "batch" transmission scheme.

The PCA5000(A)T decoder has a built-in SRAM section to hold its RIC and configuration information. This requires an external backup battery. The PCF5001T decoder uses EEPROM to store its address and configuration data.

The decoder module supports two applications: Display pager and beep-only (alert-only) pager. The choice is made by putting the right components on the board and by appropriate programming of the device.

Display Unit

Until now, no Display Unit demoboard has been produced for use with the demonstration system. Consequently, the description of the display unit is not part of this document. When a Display Unit demoboard becomes available, it will be described in a separate report.

Test and Program Unit

The Test and Program Unit can serve three purposes: The first is to replace the receiver module and to supply POCSAG coded data directly to the decoder module.

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OM4718 Test and programming unit

This provides a means for testing and demonstration of the decoder features in areas, where no suitable paging services are on the air. In this case, the Test and Program Unit can "transmit" calls, which are recognized by the decoder and thereby cause alert cadences to be generated. Message types include alert-only, numeric and alphanumeric at 512 or 1200 baud..

The second purpose is to provide the above mentioned POCSAG coded data to an RF-generator for generating an FSK-modulated signal. This in turn can be fed to the receiver module using a cable or an antenna. The demodulated data signal can then be processed by the decoder module.

The third purpose of this unit is to serve as a programmer for the Receiver Identification Codes (RIC) and the configuration bits (SPF) of the decoder module. In this case, the unit performs all necessary program interface handling, program data transfer and verification procedures. User switches are available to select either the PCA5000(A)T or the PCF5001T decoder.

3. Test and Program Unit

3.1 Overview of Operation

The Test and Program Unit (hereafter: TPU) is able to program the Philips POCSAG decoder circuits (both PCA5000(A)T and PCF5001T are supported) as well as generate a POCSAG coded signal for testing purposes. Complete POCSAG calls can be transmitted of which the call address, call type, message contents and data rate are under control of the user. The POCSAG coded signal can be passed directly to the decoder module. Alternatively, it can be used to modulate an RF-signal which is then fed to a receiver module via cable or antenna.

The TPU hardware was designed to operate in one of two basic modes:

- Stand alone Mode

Switches located on the PCB are used to control the TPU. Two modes of operation are available: Test Mode and Program Mode. In Test Mode the user can select

fixed POCSAG calls for transmission (all call types are supported). In Program Mode fixed pager configuration data (selected via switches) can be programmed into the decoder and verified. The execution of a selected function is indicated to the user by a LED indicator.

- Terminal Mode

An RS232 interface is available to support a Terminal Mode, but this mode is not supported by the current software (v.3.3 and below).

This document only describes the operation of the TPU in Standalone Mode. The user must make sure that Configuration Switch (8-1) is in the OFF position at power-on or manual reset (see section 3.3.8).

3.2 Pager Configurations

When used in Program Mode (selected by the Mode Switch, see section 3.3.13) fixed pager configurations can be programmed into the internal Special Function (SPF) memory of the selected decoder. Some settings can be controlled by means of the Configuration Switch on the board (see section 3.3.8). The following configurations are available:

PCA5000(A)T Configuration:

The addresses used are:

RIC A:2468 (Dec)	= 9 A4 (Hex)	in frame 4
RIC B:12468 (Dec)	= 30 B4 (Hex)	in frame 4

SPF settings:

SPF01: X	mode select: Alert-Only (0), Display Pager (1)
SPF02: 0	voltage converter enabled (SPF01 = 1)
SPF03: 0	1-bit error correction on message codewords
SPF04: 0	-spare- free for user application
SPF05: 0	silent override enabled on RIC B (FC = 01 or 10) (SPF01 = 1)
SPF06: 1	silent override enabled on RIC A (FC = 10)

Note: In Alert-Only mode (SPF01 = 0) silent override is enabled for all call types on RIC B, regardless of the setting of SPF05.

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PCF5001T Configuration:

The addresses used are:

RIC A:	2468 (Dec)	= 9A4 (Hex)	in frame 4
RIC B:	12468 (Dec)	= 30B4 (Hex)	in frame 4
RIC C:	799118 (Dec)	= C318E (Hex)	in frame 6
RIC D:	116358 (Dec)	= 1C686 (Hex)	in frame 6

SPF settings:

SPF01: X mode select: Alert-Only (0), Display Pager (1)

SPF02: X bit rate: 512 bps (0), 1200 bps (1)

SPF03: 0 crystal select: 32768 Hz for 512 bps,
76800 Hz for 1200 bps

SPF04: 1 receiver establishment time: 16 bits duration,
corresponding with 31.1 ms (512 bps),

SPF05: 0 13.3 ms (1200 bps)

SPF06: 0 duplicate call suppression time-out period and
Out-of-Range

SPF07: 0 hold-off time: 30 seconds

SPF08: 0 voltage converter disabled

SPF09: 0 silent override on RIC C disabled

SPF10: 1 silent override on RIC D enabled

SPF11: 0 vibrator output OM disabled

SPF12: 1 call termination after 2 consecutive
uncorrectable codewords

SPF13: 1 and numeric message deformatting on
FC = 00 only

SPF14: 1 duplicate call suppression enabled

SPF15: 1 Out-of-Range indication on OL enabled
(SPF01 = 0), hold-off time enabled
(determined by SPF06 and SPF07)

SPF16: 1 repeat alert enabled

SPF17: 0 call data output on OL disabled

SPF18: 0 _spare_ free for user application

SPF19: 0 must always be zero

SPF20: 0 _spare_ free for user application:

:

SPF30:0 _spare_ free for user application

SPF31:0 alerter frequency 2048 Hz

SPF32:1 frequency reference output on FL: 32768 Hz
(SPF01 = 1)

3.3 Hardware Description

In the following sections the hardware of the TPU is described as shown in fig. 3-1. Each component has been given a number for easy reference.

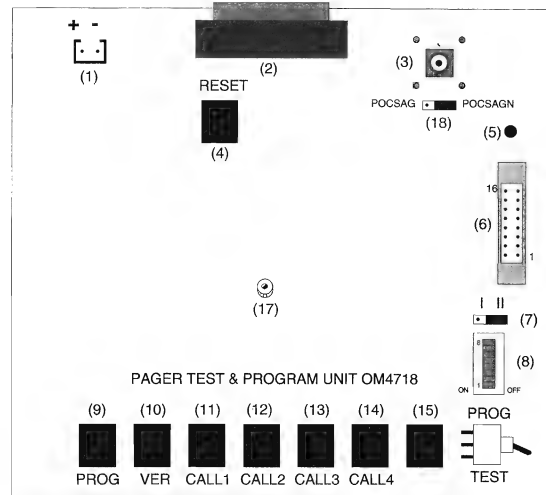


Fig. 3-5 Pager Test & Program Unit Hardware

3.3.1 Power Supply Connector (1)

The TPU operates from a single supply voltage of 5 volts. The TPU will sink 40-50 mA (CMOS EPROM) or 80-100 mA (NMOS EPROM), without any other module connected. A 2-pin bandcable connector is provided for power connection.

Note: No protection is provided against reversing the supply polarity! The supply connector pin closest to the RS-232 connector is GND or the negative supply side.

3.3.2 Terminal Connector (2)

This RS232 connector is intended for use in Terminal Mode only. The Terminal Mode is not implemented in the current software (v.3.3 and below).

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3.3.3 POCSAG Data Output (3)

In Test Mode this output provides POCSAG data at true TTL-Level: Logic "1" corresponds to HIGH level and Logic "0" to LOW level. A jumper (18) has been provided for selecting the signal polarity (POCSAG or POCSAGN). Instead of the mounted SMB-connector, a BNC-type can also be installed.

The output signal is not suitable for driving the receiver module directly. An RF-generator with TTL-Level input may be modulated with this signal. The POCSAG Data Output will not be active in Program Mode.

3.3.4 RESET pushbutton (4)

Pressing the RESET pushbutton initializes the TPU. After selection of the basic operation mode (Terminal or Standalone Mode) with Configuration DIP Switch (8-1), it is necessary to reset the TPU. This can be achieved with the RESET pushbutton, without the need for disconnecting the power supply.

3.3.5 LED Indicator (5)

The LED is used for acknowledgement to the user in the Stand-alone Mode (no action in Terminal Mode). In general one flash will occur after execution of a selected function or after changing the operating mode (Test to Program Mode or vice versa). The LED will also signal a reset.

If the Verify function (10) is activated in Program Mode (16) the LED will signal success or failure of verification:

- Single flash: signals that the configuration data read from the decoder's RAM or EEPROM correspond with the data expected by the TPU ("Decoder Data OK").
- Double flash: signals that a mismatch was found between the decoder's RAM or EEPROM data and the data expected by the TPU ("Decoder Data Error").

3.3.6 Decoder Module Connector (6)

Via this connector the decoder module can be attached to the TPU. This connection is required if the decoder RAM or EEPROM data are to be programmed or verified in Program Mode. In Test Mode the decoder module may be connected via this connector to allow direct POCSAG data transfer to the decoder. When an RF-signal modulated with POCSAG data is available the decoder will be connected to a receiver module for POCSAG data reception.

3.3.7 Logic Reference Option (7)

For flexible interfacing to the decoder module the logic reference for HIGH level can be selected using jumper (7).

- Option I: HIGH level reference is VDD from the decoder module. VDD is the positive battery supply voltage.
- Option II: HIGH level reference is VD from the decoder module. VD is the actual supply voltage of the decoder. This is the default setting.

In case of the PCA5000(A)T decoder board, VD is one diode voltage below VDD. Therefore, Option II should be selected for proper programming of the PCA5000(A)T. For the PCF5001T decoder board (OM4706) there is no preference, since both VDD and VD are connected to the positive battery terminal (no protective diode).

3.3.8 Configuration DIP Switch (8)

- DIP 1: *Basic Mode:* This switch selects the basic mode of the TPU. The setting of this switch will be recognized only after a reset (4) or power-on reset.
ON: Terminal Mode
OFF: Standalone Mode (default)
- DIP 2: *Decoder Type:* While operating in Program Mode the switch is used to select the decoder type, for proper programming and verification of the connected decoder. During Test Mode no function is applied.
ON: PCA5000(A)T
OFF: PCF5001T

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DIP 3: *Data Rate:* While operating in Test Mode the switch is used to select the employed data rate for POCSAG data transmission. In Program Mode this switch only has a function for the PCF5001T: it sets bits SPF02 and SPF03 according to the selected data rate (512 baud: 32768 Hz crystal, 1200 baud: 76800 Hz crystal). The option 512 baud with 76800 Hz crystal is not available.
ON: 512 bps
OFF: 1200 bps

DIP 4: *Decoder Basic Mode:* While operating in Program Mode the switch determines whether the decoder will be programmed as an Alert-only pager or as a Display pager. No function is applied while operating in Test Mode.
ON: Alert-only pager
OFF: Display pager

DIP 5,6: *Call Address (RIC):* During Test Mode these switches select the used call address, when a call is transmitted by the TPU. They also select the message that will be used when a numeric or alphanumeric call is generated (see 3.3.11). No function is applied while operating in Program Mode.

DIP 5	DIP 6	Address
ON	ON	RIC A
ON	OFF	RIC B
OFF	ON	RIC C (PCF5001T only)
OFF	OFF	RIC D (PCF5001T only)

DIP 7,8: No function

3.3.9 Pushbutton PROG (9)

When operating in Program Mode this key is used to program the decoder module. Only fixed RAM or EEPROM data are available. The decoder will be programmed according to the setting of the Configuration DIP Switch (8). The LED indicator (5) is activated during programming. No function applies when operating in Test Mode.

3.3.10 Pushbutton VER (10)

This key activates the Verify function when Program Mode has been selected. It is used to check decoder RAM or EEPROM data for proper setting. The decoder data will be compared with the fixed configuration data stored in the TPU. The Configuration DIP Switch (8) is used to select the pager configuration to be verified. The LED indicator (5) will signal success (one flash) or failure (double flash) of the verification. No function applies when operating in Test Mode.

3.3.11 Pushbuttons CALL1 (11) to CALL4 (14)

For testing purposes POCSAG calls can be transferred to the decoder, either directly via (6) or indirectly via (3). While operating in Test Mode 16 different POCSAG calls can be inserted into the continuous POCSAG data transmission. Configuration DIP Switches (8-5,6) determine which address shall be used and which of the fixed messages shall be used for numeric or alphanumeric calls.

The addresses are selected as shown in section 3.3.8 and are defined as follows:

RIC A:	2468 (Dec)	= 9A4 (Hex)	in frame 4
RIC B:	12468 (Dec)	= 30B4 (Hex)	in frame 4
RIC C:	799118 (Dec)	= C318E (Hex)	in frame 6 (PCF5001T only)
RIC D:	116358 (Dec)	= 1C686 (Hex)	in frame 6 (PCF5001T only)

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The following calls can be issued by pressing the appropriate pushbutton:

- CALL1:** Numeric call
 Function code: 00 binary
 Message (RIC A/C): 49-40-54007-0
 Message (RIC B/D): 2468-12468
- CALL2:** Beep-only call
 Function code: 01 binary
 Message: none
- CALL3:** Beep only call
 Function code: 10 binary
 Message: none
- CALL4:** Alphanumeric call
 Function code: 11 binary
 Message (RIC A/C):
 "Hello, call your wife at home! - Testmessage:"
 "The quick brown fox jumps over the lazy dog"
 "Display with 120 characters!"
 Message (RIC B/D):
 "PHILIPS Integrated Circuits for POCSAG
 Paging Systems"
 "Software Version 3.1"

No function occurs when operating the TPU in Program Mode.

3.3.12 Pushbutton (15)

No function implemented.

3.3.13 Mode Switch (16)

This switch selects the Test Mode or the Program Mode of operation.

Program Mode (switch position 'PROG'):

Upon switching into Program Mode the generation of POCSAG data will be aborted and the interface signals to the decoder will be made three-state (high impedance). The decoder module will remain under power, when connected to the TPU with batteries inserted into the decoder module, because of the state of the provided relay (RL401, see circuit diagram #4 in Appendix D).

Pushbuttons PROG (9) and VER (10) can be used to program respectively verify the decoder's RAM or EEPROM memory. During programming or verifying the decoder will be switched off briefly to enter and leave the Program Write or Program Read mode of the decoder. The program interface signals to the decoder will be enabled, as soon as the Program or Verify function is activated.

TestMode (switch position 'TEST'):

Switching into the Test Mode will enable generation of POCSAG data. The POCSAG data interface signals to the decoder will be enabled to allow continuous data transfer. The decoder module will be under power, when connected to the TPU with batteries inserted into the decoder module, because of the state of the provided relay (RL401, see TPU circuit diagram #4). The transmission of POCSAG data will start with a preamble (576 bits) followed by batches filled with idle codewords, each batch being preceded by a synchronization codeword. Upon pushing one of the four buttons CALL1 (11) to CALL4 (14) the associated POCSAG call will be inserted into the data stream.

3.3.14 Oscillator Adjust (17)

A variable capacitor is provided to allow adjustment of the microcontroller crystal to calibrate the transmission data rate.

3.4 Preparation and Operation

Connect a power supply of 5 volts to the TPU via connector (1), see fig. 3-1. Before switching on make sure that the supply polarity is not reversed, since no protection is provided. The TPU should sink a current of typ. 40-50 mA (CMOS EPROM or 80-100 mA (NMOS EPROM), without any other module connected.

3.4.1 Terminal Mode

Not implemented (software v.3.3 and below).

3.4.2 Standalone Mode

The Standalone Mode will be entered, when Configuration DIP Switch (8-1) is set to OFF position

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(Basic Mode = Standalone) and a reset is actuated. A single flash of the LED (5) will signal that the Standalone Mode has been entered.

3.4.2.1 Decoder Programming and Verification

Connect the decoder module to the TPU via the decoder module connector (6). Insert batteries into the decoder module in order to make it operational. After selecting the Program Mode with the Mode Switch (16) and setting of the Configuration DIP Switch (8), the decoder RAM/EEPROM data can be programmed and verified. The LED indicator (5) will acknowledge that the Program Mode had been entered. The Configuration DIP Switch (8) determines the selected decoder type and the decoder basic mode.

Upon pushing the Program button (9) the decoder will be programmed. The LED indicator (5) will acknowledge after completion of program operation.

Upon pushing the Verify button (10) the decoder RAM/EEPROM data will be verified. A single flash of the LED indicator will signal successful programming and a double flash will signal a programming failure.

Note: For correct verification no settings of the Configuration DIP Switch (8) may be changed between programming and verifying the decoder.

3.4.2.2 POCSAG Signal Generation

By selecting the Test Mode with the Mode Switch (16), generation of a POCSAG coded signal will be started. Data rates of 512 bps and 1200 bps can be selected according to the setting of the Configuration DIP Switch (8). Upon switching into Program Mode, generation of a POCSAG coded signal will be aborted. The LED indicator (5) will acknowledge when the Test or Program Mode is entered.

Generation of the POCSAG coded signal means that a *preamble* (576 bits) is transmitted, followed by batches filled with *idle codewords*, each batch being preceded by a *synchronization codeword* (see chapter III, pager system aspects for details on the POCSAG code structure).

The POCSAG coded signal is supplied to the user via the general purpose POCSAG data output (3) at TTL-Level, or directly to a connected decoder module via the decoder module connector (6). The signal polarity on connector (3) can be selected by means of jumper (18).

POCSAG calls can be transmitted, if one of the four pushbuttons CALL1 (11) to CALL4 (14) are pressed. Pushbutton CALL1 (11) will transmit a numeric call, pushbuttons CALL2 (12) and CALL3 (13) will send beep-only calls and push-button CALL4 (14) will issue a alphanumeric call. The LED indicator will acknowledge if the POCSAG call had been inserted into the continuous POCSAG data stream. Call address and call message contents are determined by the Configuration DIP Switch setting (8), see section 3.3.8. For address values and message contents see section 3.3.11.

3.5 Troubleshooting

Several conditions may arise, which seem to indicate equipment malfunctioning. A number of these conditions are listed below with the appropriate actions.

- **No acknowledge by the LED indicator (5):**
Make sure the Standalone Basic Operating Mode was selected by the Configuration DIP switch (8). The LED indicator is active in Standalone Mode only and will not acknowledge for Terminal Mode. Consider that the pushbuttons PROG (9) and VER (10) are active in Program Mode, and pushbuttons CALL1 (11) to CALL4 (15) are active in Test Mode only.
- **The decoder module cannot be programmed or verified:**
Check for a correct connection between the decoder module and the TPU via the decoder module connector (6). Make sure Program Mode is active (16), the appropriate decoder type and decoder basic mode were selected (8). Verify that and the decoder module is under power (batteries must be inserted into the decoder module). Check that the decoder module is operating, e.g. by generation of a status cadence. Check the battery condition with a voltmeter (min. supply voltage is 2.0 Volt for correct programming).

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- **The decoder module does not operate after programming a new configuration:**

Check for correct programming by a verify operation (10). Make sure the appropriate decoder Basic Operating Mode was selected while programming (Configuration Switch 8-4). Note that a decoder module with hardware configured for an Alert-only pager will not work properly when if it is programmed for Display pager application and vice versa.

- **The PCF5001T decoder module (OM4706) generates alert cadences at a wrong frequency and with wrong timing:**

Check that the crystal frequency used (OPT3 jumper on the OM4706) matches the Data Rate programmed into the decoder (Configuration DIP Switch 8-3): 32768 Hz for 512 bps and 76800 Hz for 1200 bps.

- **Calls transmitted are not recognized by the decoder module:**

Make sure that the connection between the decoder module and the TPU is correct, if the decoder module is connected directly.

When the decoder module is used in combination with a receiver module, check the connection between the general purpose POCSAG data output (3) and the RF-Generator as well as the connection between the receiver module's RF-Input and the RF-Generator.

Verify that the TTL-Level and the polarity of the POCSAG data on output (3) are suitable for modulation of the RF-Generator. If necessary the inverted (POCSAGN) signal can be selected using jumper (18).

Verify the FM transmitter frequency, the deviation (4 or 4.5 kHz) and the RF output level. It is assumed that the receiver module has been properly tuned.

The Data Rate selected for call transmission (Configuration DIP Switch, 8-3) should match the configuration programmed into the decoder. Make sure that the decoder is not in OFF state (check status cadence) and not in an Out-of-Range condition (Out-of-Range LED on decoder board flashing at 1 second intervals). For fast synchronization of the decoder, the

TPU can be switched to Program Mode and then back to Test Mode. This will initiate the transmission of a preamble, causing the decoder to synchronize immediately and subsequent calls to be recognized.

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4. Changing user addresses and configuration bits

The OM4718 software (version 3.3) does not support a Terminal mode of operation, which would allow downloading of user addresses, configuration bits and message contents. This has proved to be a handicap for many users of the system. Therefore, the following sections will describe how to modify those sections of the EPROM code of the 80C31 microcontroller where user addresses (RICs) and configuration bits reside. Also, the internal representation and location of the fixed message texts will be discussed.

The EPROM contents can be changed manually using an EPROM programmer or by changing the Intel Hex file. In the latter case the checksum at the end of each modified line must be re-calculated to avoid transfer errors.

The information in this section only applies to software version 3.3, 22 may 1991.

4.1 Modifying user addresses

4.1.1 Internal representation of RICs

The user addresses (RICs) are handled by the following software statements:

opcode	instruction	description
74 xx	MOV A,#data8	get byte 'xx' of address
90 yy zz	MOV DPTR,#adr16	load data pointer with external RAM address 'yyzz'
F0	MOVX @DPTR,A	write byte to external RAM

The fixed RICs are represented differently in the software, depending on the mode of operation (Test mode or Program mode). In Test mode the RIC is represented as a 3-byte hexadecimal number. For programming a 21-bit RIC (A00..A20, A00=MSB) is represented as an 18-bit address (A00..A17) followed by a 3-bit frame number (FR0..2, FR0=MSB).

RIC (dec)	RIC (hex)	RIC (0..17, hex)	Frame (0..2,bin)
A: 2468	00 09 A4	00 01 34	100 (=4 dec)
B: 12468	00 30 B4	00 06 16	100 "
C: 799118	0C 31 8E	01 86 31	110 (=6 dec)
D: 116358	01 C6 86	00 38 D0	110 "

For proper operation of the OM4718 it is imperative that both internal representations of the RICs are modified correctly. Please note that the frame bits for the PCF5001 RICs are stored in inverted order!

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4.1.2 EPROM locations of RICs for Test mode

For Test mode the RICs can be found in the EPROM on the following locations:

	ROM addr	opcode	description
RIC A:	1DD4	74 A4	MOV A, #LS byte
	1DDA	74 09	middle byte
	1DE0	74 00	MS byte
RIC B:	1E40	74 B4	LS byte
	1E46	74 30	middle byte
	1E4C	74 00	MS byte
RIC C:	1EB5	74 8E	LS byte
	1EBB	74 31	middle byte
	1EC1	74 0C	MS byte
RIC D:	1F21	74 86	LS byte
	1F27	74 C6	middle byte
	1F2D	74 01	MS byte

OM4718 EPROM contents (version 3.3)

Format: Intel Hex

Part: RICs for Test mode

:101DD0001C8E406C74A49000080F074099000081F017	Test mode: RIC A
:101DE00074009000082F0E53F90218DF828287380E0	
:101DF0004D9000083E4F0753A21753BE7753C007522	
:101E00003D85121C9A9000084F080339000083740109	
:101E1000F09000084E4F0802674029000083F090003B	
:101E200084E4F0801974039000083F0753A22753BC6	
:101E300000753C00753D85121C9A9000084F0806A04	
:101E400074B49000080F074309000081F0740090000C1	Test mode: RIC B
:101E500082F0E53F90219CF8282873804D900008304	
:101E6000E4F0753A21753BF5753C00753D85121C13	
:101E70009A9000084F0803390000837401F0900008485	
:101E8000E4F0802674029000083F09000084E4F080F7	
:101E90001974039000083F0753A22753B79753C0004	
:101EA000753D85121C9A9000084F0021F8B753A20B4	
:101EB000121C8E406C748E9000080F07431900008102	Test mode: RIC C
:101EC000F0740C9000082F0E53F9021ABF828287365	
:101ED000804D9000083E4F0753A21753BE7753C0036	
:101EE000753D85121C9A9000084F08033900008374B5	
:101EF00001F09000084E4F0802674029000083F0905A	
:101F000000084E4F0801974039000083F0753A227520	
:101F10003B00753C00753D85121C9A9000084F08052	
:101F20006A74869000080F074C69000081F07401900D	Test mode: RIC D

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4.1.3 EPROM locations of RICs for Program mode

In Program mode the RICs are separately stored for the PCA5000(A) and for the PCF5001 decoder.

PCA5000(A):

	ROM addr	opcode	description
RIC A:	1FBA	74 34	MOV A,#LS byte
	1FC0	74 01	middle byte
	1FC6	74 00	MS bits (bit 7:A00, bit 6:A01)
RIC B:	1FCC	74 16	LS byte
	1FD2	74 06	middle byte
	1FD8	74 00	MS bits (bit 7:A00, bit 6:A01)
Frame:	1FDE	74 04	frame nr. (LS nibble)

The lower 3 bits of RIC A and B contain the (common) frame number represented as FR0..2, FR0 being the most significant bit. These bits are stored in the lower nibble of the frame number byte as follows: bits 2..0 = FR0..2.

PCF5001:

	ROM addr	opcode	description
RIC A:	203B	74 34	MOV A,#LS byte
	2041	74 01	middle byte
	2047	74 00	MS bits (bit 7:A00, bit 6:A01)
RIC B:	204D	74 16	LS byte
	2053	74 06	middle byte
	2059	74 00	MS bits (bit 7:A00, bit 6:A01)
RIC C:	205F	74 31	LS byte
	2065	74 86	middle byte
	206B	74 40	MS bits (bit 7:A00, bit 6:A01)
RIC D:	2071	74 D0	LS byte
	2077	74 38	middle byte
	207D	74 00	MS bits (bit 7:A00, bit 6:A01)
Frame:	2083	74 31	frame nr. (A/B: LS nibble, C/D MS nibble)

The lower 3 bits of RICs A and B contain the (common) frame number represented as FR10..12, FR10 being the MSB. These bits are stored in the lower nibble of the frame number byte as follows: bits 2..0 = FR12..10 (order is reversed !!).

The common frame number of RICs C and D is represented by FR20..22, FR20 being the MSB. These bits are stored in the upper nibble of the frame number byte as follows: bits 6..4 = FR22..20 (order is reversed !!).

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OM4718 EPROM contents (version 3.3)

Format: Intel Hex

Part: RICs for Program mode

```

:101FB000E4F0800674029000FEF074349000FFF0AC      PCA5000: RIC A
:101FC0007401900100F07400900101F0741690010A      PCA5000: RIC B
:101FD00002F07406900103F07400900104F07404A0      PCA5000: frame
:101FE000900105F0753A08121C8EB3400874849075
:101FF0000106F080067404900106F0752C00752D22
:10200000FE121B36F53CE53C9021C9F82828737573
:102010003C028012753C01800D753C018008753CC6
:10202000028003753C020220FDE53BB401079001EC
:1020300007E4F080067402900107F0743490010800      PCF5001: RIC A
:10204000F07401900109F0740090010AF074169088      PCF5001: RIC B
:10205000010BF0740690010CF0740090010DF07407
:102060003190010EF0748690010FF07440900110D1      PCF5001: RIC C
:10207000F074D0900111F07438900112F074009057      PCF5001: RIC D
:102080000113F07431900114F0753A08121C8EB3EC      PCF5001: frames

```

4.2 Modifying decoder configurations**4.2.1 Internal representation of SPF bits**

The SPF configuration bits are handled by the following software statement:

<u>opcode</u>	<u>instruction</u>	<u>description</u>
74 xx	MOV A, #data8	get byte 'xx' of the configuration array

The internal representation of the SPF bits is different for the two decoder ICs.

PCA5000(A):

The 6 SPF bits are stored in configuration byte Dconfig, of which the lower 2 bits are not used (value: '0'):

```
Dconfig = SPF01..06 (MSB: SPF01), '0', '0'
```

The standard contents depend on the actual DIP switch settings:

```

Dconfig1 = 04 Hex      | alert-only
Dconfig1 = 84 Hex      | display

```

PCF5001:

The 32 SPF bits are stored in configuration array Econfig (4 bytes):

```

Econfig_0 = SPF01..08 (MSB: SPF01)
Econfig_1 = SPF09..16 (MSB: SPF09)
Econfig_2 = SPF17..24 (MSB: SPF17)
Econfig_3 = SPF25..36 (MSB: SPF25)

```

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Standard contents are:

Econfig_0 = Econfig_0A = 90 Hex (512 bps / alert only) | depends
Econfig_0 = Econfig_0B = D0 Hex (1200 bps / alert only) | on actual
Econfig_0 = Econfig_0A = 10 Hex (512 bps / display) | DIP switch
Econfig_0 = Econfig_0A = 50 Hex (1200 bps / display) | settings
Econfig_1 = 5F Hex |
Econfig_2 = 00 Hex | fixed
Econfig_3 = 01 Hex |

4.2.2 EPROM locations of SPF bits

The configuration bytes can be found in the following EPROM locations:
PCA5000(A):

	ROM addr	opcode	description
Dconfig1:	1FF5	74 04	SPF bits 1..6 (alert only)
Dconfig2:	1FED	74 84	SPF bits 1..6 (display)

PCF5001:

	ROM addr	opcode	description
Econfig_0A :	209A	74 90	SPF bits 1..8 (512 bps / alert only)
Econfig_0B :	20A2	74 D0	SPF bits 1..8 (1200 bps / alert only)
Econfig_0C :	20B2	74 10	SPF bits 1..8 (512 bps / display)
Econfig_0D :	20BA	74 50	SPF bits 1..8 (1200 bps / display)
Econfig_1 :	20C0	74 5F	SPF bits 9..16
Econfig_2 :	20C6	74 00	SPF bits 17..24
Econfig_3 :	20CC	74 01	SPF bits 25..32

OM4718 EPROM contents (version 3.3)

Format: Intel Hex

Part: SPF bits PCA5000(A)

:101FE000900105F0753A08121C8EB3400874849075 Dconfig2
:101FF0000106F080067404900106F0752C00752D22 Dconfig1

Format: Intel Hex

Part: SPF bits PCF5001

:102090004018753A04121C8E40087490900115F097 Econfig_0A
:1020A000800674D0900115F08016753A04121C8ECB Econfig_0B
:1020B00040087410900115F080067450900115F0DE Econfig_0C/0D
:1020C000745F900116F07400900117F07401900194 Econfig_1/2/3

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4.2.3 SPF bit functionality overview

This paragraph presents an overview of the SPF bit functionality in both the PCA5000(A) and the PCF5001 decoder. The default values used in the OM4718 software version 3.3 are given. Where relevant the controlling DIP switch is also indicated. A DIP switch position 'ON' corresponds with a logical value '0'.

PCA5000(A):

Bit name	Default	Function
SPF01	DIP4	Alert only (0) / Display Pager (1)
SPF02	0	Voltage doubler enable (1 = ON, only when SPF01=1); selects alert cadence 1 for FC = 11
SPF03	0	Message codeword error correction method (0 = 1-bit random, 1 = 4-bit burst on RIC B, FC = 00/11)
SPF04	0	spare
SPF05	0	Silent override on RIC B, only when SPF01=1 (0 = for FC=01/10, 1 = for FC=00/11)
SPF06	1	Silent override on RIC A, FC=10 (1 = enabled)

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PCF5001:

<u>Bit name</u>	<u>Default</u>	<u>Function</u>
SPF01	DIP4	Alert only (0) / Display Pager (1)
SPF02	DIP3	baudrate selection: 512 bps (0), 1200 bps (1)
SPF03	0	crystal selection: 32768 Hz (0), 76800 Hz (1, X if SPF02=1)
SPF04	1	Rec. Establ. time-select (MSB)
SPF05	0	Rec. Establ. time select (LSB)
SPF06	0	Hold Off time select (MSB)
SPF07	0	Hold Off time select (LSB)
SPF08	0	Voltage doubler enable (1 = ON, only when SPF01=1)
SPF09	0	Silent override on RIC C (1 = enabled)
SPF10	1	Silent override on RIC D (1 = enabled)
SPF11	0	Vibrator enable (1 = ON)
SPF12	1	Call termination method (0 = combination, 1 = acc. to SPF13)
SPF13	1	Numeric deformatting / Call termination method (0 = always / 1 erron. cw, 1 = only on FC=00 / 2 erron. cw's)
SPF14	1	Duplicate call suppression (1 = enabled)
SPF15	1	Out-of-Range indication on OL (1 = enabled with holdoff acc. to SPF06/07)
SPF16	1	Repeat alert (1 = enabled)
SPF17	0	Call data on OL (1 = enabled)
SPF18	0	spare
SPF19	0	always program as '0'
SPF20	0	spare
SPF21	0	"
SPF22	0	"
SPF23	0	"
SPF24	0	"
SPF25	0	spare
SPF26	0	"
SPF27	0	"
SPF28	0	"
SPF29	0	"
SPF30	0	"
SPF31	0	Alerter frequency (0 = 2048 Hz, 1 = 2731 Hz)
SPF32	1	Reference frequency on FL (0 = 16384 Hz, 1 = 32768 Hz), active only when SPF01 = 1

In the OM4718 software the crystal selection bit (SPF03) for the PCF5001 may remain fixed at '0', because a 76800 Hz crystal is automatically assumed when 1200 bps operation is selected (SPF02 = 1).

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4.3 Modifying message contents

4.3.1 Internal message representation

The paging messages transmitted when a CALL button is pressed in Test mode, are stored internally as byte arrays. The length of a message is determined implicitly by ending it with a special byte ('FF' Hex). Numeric digits are stored in the LS-nibble of a byte, the bits in the MS-nibble remaining '0'. Alphanumeric characters are stored in the lower 7 bits of a byte, the MSB remaining '0'. Since the messages are embedded in the code, their maximum length is fixed. Shorter messages may be used by placing the 'FF' termination byte at an earlier position in the EPROM code.

Message	Max. length	Default contents
Numeric A	13 digits	49-40-54007-0
Numeric B	10 digits	2468-12468
Alphanum. A	120 chars	Hello, call your wife...
Alphanum. B	75 chars	PHILIPS Integrated Circuits...

4.3.2 EPROM locations of message texts

The EPROM locations of the messages are given below. ROM End is the last location which may be used for message data in the byte array, the next location contains the 'FF' termination byte.

Message	ROM Start	ROM End	Contents (Hex)	Contents (text)
Numeric A:	21E7	21F3	04 09 0D 04 00...	49-40...
Numeric B:	21F5	21FE	02 04 06 08 0D...	2468...
Alphanum. A:	2200	2277	48 65 6C 6C 6F...	Hello...
Alphanum. B:	2279	22C3	50 48 49 4C 49...	PHILI...

OM4718 EPROM contents (version 3.3)

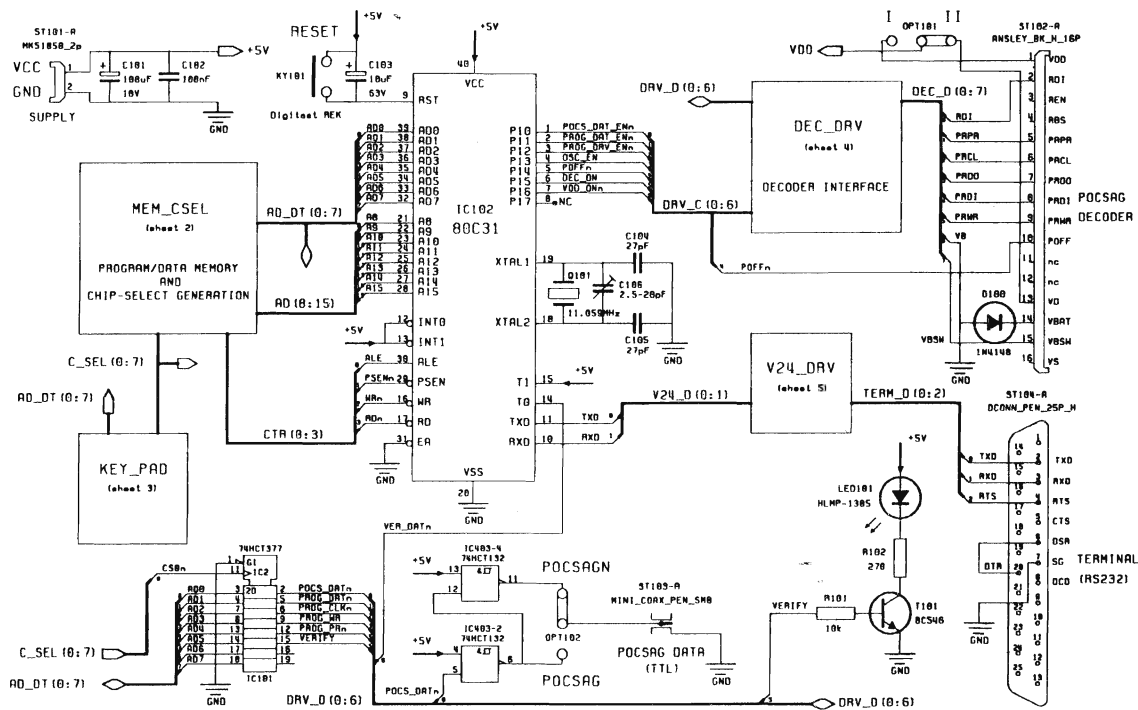
Format: Intel Hex
Part: Message texts

:1021E000F00220F50220FA04090D04000D05040098	Numeric A
:1021F00000070D00FF020406080D0102040608FF97	Numeric B
:1022000048656C6C6F2C2063616C6C20796F757203	Alphanum. A
:10221000207769666520617420686F6D65212020D4	
:10222000202D3E20546573746D6573736167653A44	
:1022300054686520717569636B2062726F776E20D8	
:10224000666F78206A756D7073206F766572207482	
:102250006865206C617A7920646F672044697370C7	
:102260006C6179207769746820313230204368616D	
:102270007261637465727321FF5048494C49505331	Alphanum. B
:1022800020496E7465677261746564204369726386	
:102290007569747320666F7220504F435341472015	
:1022A000506167696E672053797374656D73202080	
:1022B000536F6674776172652056657273696F6ECD	
:1022C00020332E31FF7CD215D87A89C197BC000FFC	

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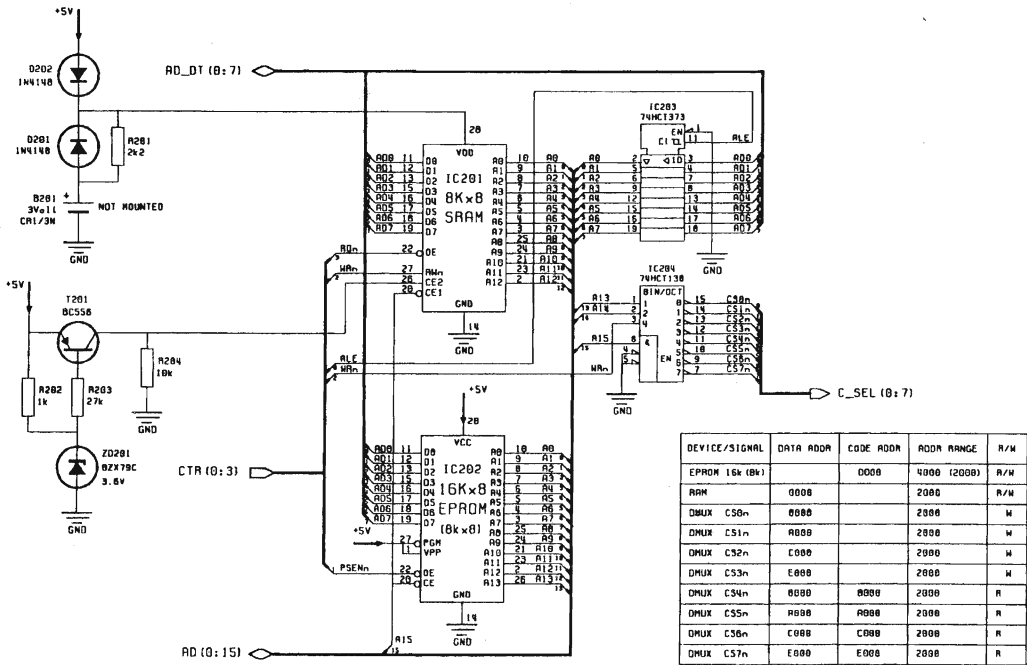
OM4718 Test and programming unit

System Overview



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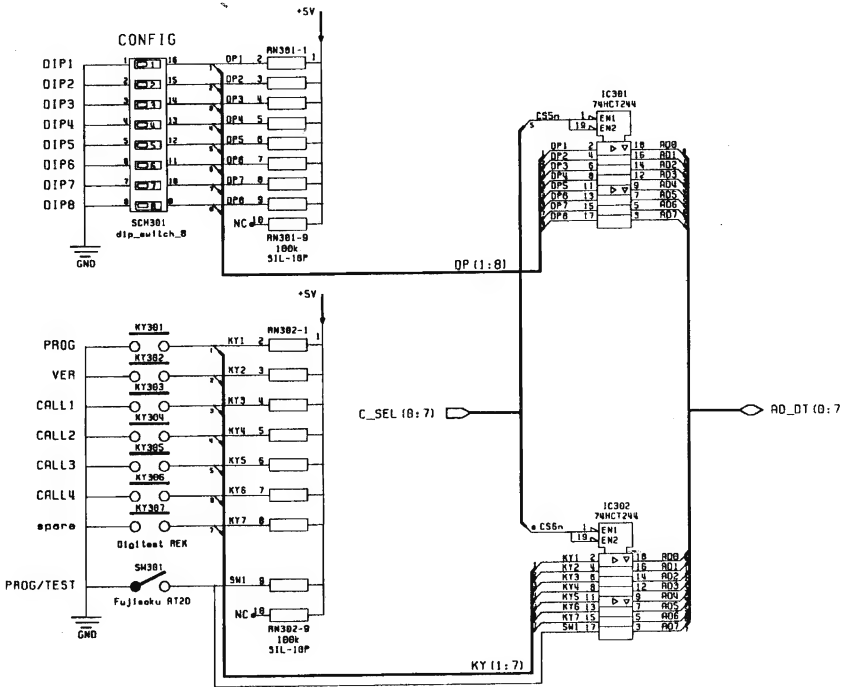
Memory Selection



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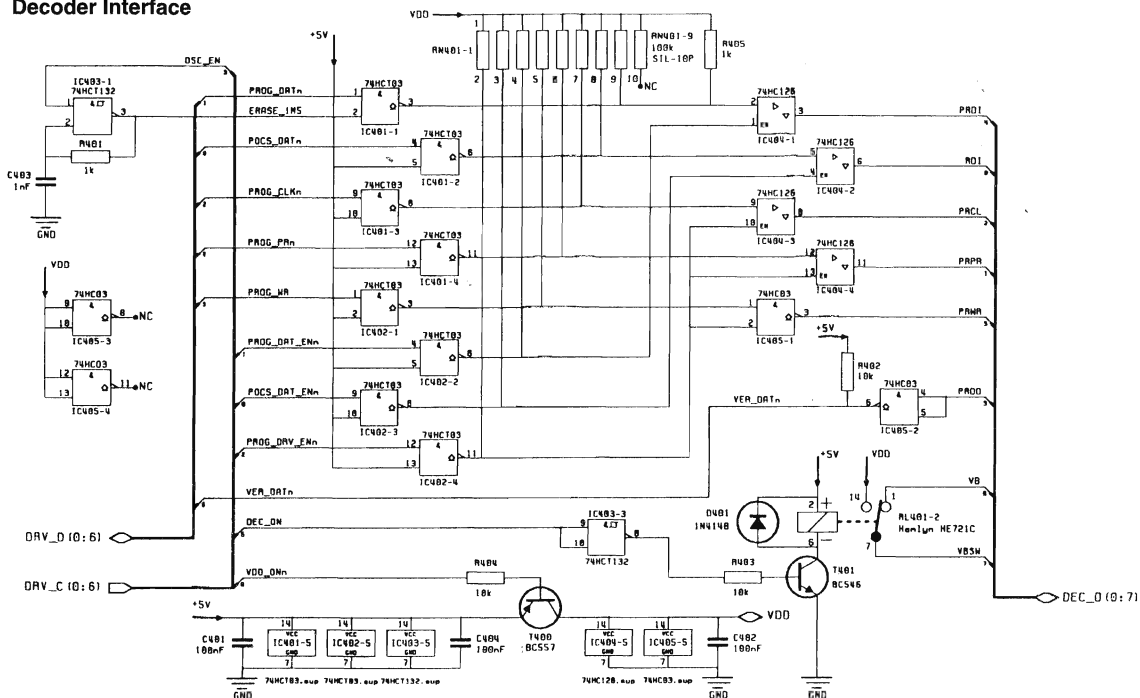
OM4718 Test and programming unit

Key Pad

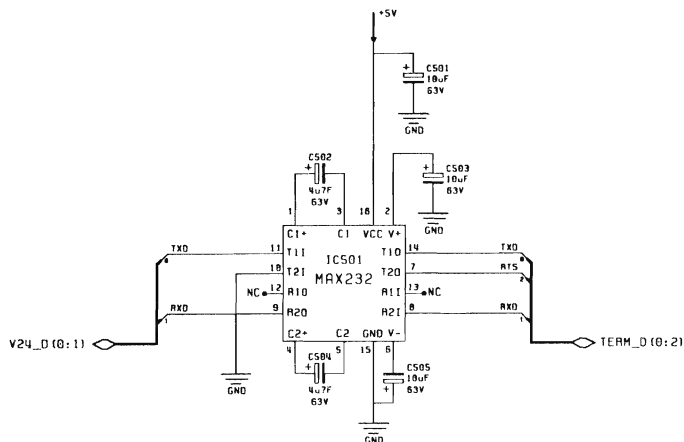


OM4718 Test and programming unit

Decoder Interface



RS232 Driver



Pager development tools and materials

OM4749 Bit Error Rate test board

THE BIT ERROR RATE TEST UNIT OM4749

This paper describes a BER-Test board specially designed for measurements on pager receivers. The test board is used together with an RF-generator. Using these two devices, pager receivers can be tested, using one out of four data types, which can all be transmitted with four different baud rates.

The BER-test board is a relatively cheap measuring-instrument for the evaluation of pager receivers. The concept of the test board has been kept as simple as possible: this makes the instrument very easy to use.

The measurement system will be explained, together with the hardware set-up. Finally, an explanation is given about I/O-synchronization, BER-calculations and PRBS-data generation.

1. Introduction

As the mobility of people is increasing everyday, the market for mobile communication equipment is growing with it. A cheap and convenient way of being in touch,

wherever you go, is carrying a Radio Pager with you. These can be very small and yet they can inform you about important messages.

Basically, pagers consist of two parts, the first is the receiver part and the second is the decoder part. Pagers can also be equipped with an LCD, displaying messages. This requires a microcontroller within the pager as well.

The receiver part converts the modulated RF-input signals into a binary data stream, which is then passed to the decoder. The decoding algorithm is based on the protocol of the POCSAG transmission code. On detecting a valid call, the decoder will generate a "beep" signal. This information is passed on to the microcontroller, together with any message content.

The performance of a pager is measured as the "call success rate". This performance is specified as the RF-level giving a success rate of 80% in the complete pager system, receiver and decoder.

This call success rate measurement may be accomplished by comparing the output data of the pager with the measurement system input in order to derive at the Bit Error Rate (BER).

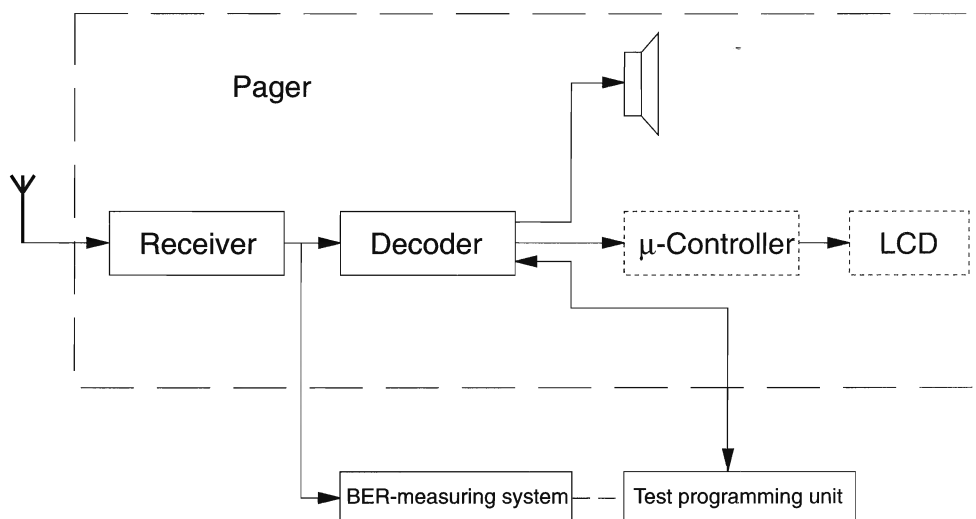


Fig. 1 Basic pager test system

Pager development tools and materials

OM4749 Bit Error Rate test board

This way, the performance is specified as the RF-level giving a BER of 3%.

2. The BER measurement system specification.

A multi-purpose transmission analyzer, capable of BER measurements, is usually expensive and complicated in its use. With this in mind, a BER-test board has been developed, aiming at a simple hardware design, without losing any functionality, and specially designed for measurements on pager receivers

A microcontroller based concept appeared to fulfil these requirements best.

The BER-test board is capable of the following:

- output data:
 - Preamble (101010...)
 - Pattern (optional pattern of 32 bits)
 - PRBS (random data: 2 exp.20 bits)
 - All 1's (111111...)
- Baudrate:
 - 512 bit/s
 - 600 bit/s
 - 1200 bit/s
 - 2400 bit/s
- Display accuracy of 0.01%.
- Output voltage level adjustable between 1 and 4 Volt for a logical one and -1 and -4 Volt for a logical zero, to shut most RF-generator types.
- Possibility for inverted output data.
- Direct input from the pager receiver. Input levels (max 5 Volt) are converted to TTL.
- No maximum amount of bits for BER-calculation.
- The test board can also be used as a data generator.

3. The BER measurement set-up.

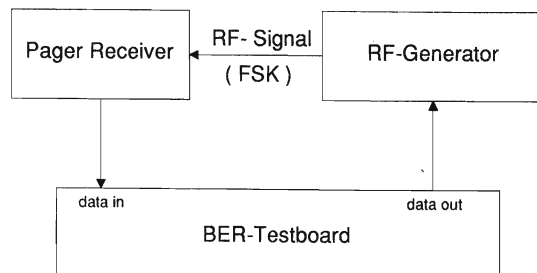


Fig. 2 The BER measurement set-up

The test board is used together with an RF-generator. The data output from the test board goes to the RF-generator.

Frequency bands used for wide area pagers are:

138 - 174 MHz	450 - 970 MHz
275 - 285 MHz	928 - 938 MHz.

The type of modulation is FSK with a frequency shift of ± 4.5 kHz for 25 kHz channels and ± 4 kHz for 20 kHz channels. The modulated signal is passed on to the pager receiver. Here, the RF-signals will be demodulated and a binary data signal is derived again. This binary signal is fed to the BER test-board, closing the loop. Depending on the RF-level of the input signal: high levels of RF input signal will be demodulated correctly, low levels may generate errors.

The I/O-synchronization can be controlled in two ways: automatically or manually. This option is set in a change menu. In case of automatic synchronization control, new synchronization is only obtained if necessary, i.e. before first BER-measurements or after changing the Baudrate. On manual synchronization, the user can decide to re-synchronize at the start of a new BER-measurement.

As the input sample moment is not PLL-controlled, it is very important to keep an eye on I/O-synchronization. For this a test pin is incorporated on the board.

Pager development tools and materials

OM4749 Bit Error Rate test board

The output data of the pager receiver can directly be passed to the test board, which also contains a filter facility.

The microcontroller is a 87C652 μ C, the EPROM version of 80C652. It has an on-board memory of 8k ROM and 256 bytes RAM.
The Baudrate of the data signals is controlled by the internal timers of the μ C, running on a 12 MHz clock.

4. BER-Calculation and Display

The user interface of the BER board consists of an LCD-display, functional keys and a few LED for indication purposes.

In order to display the BER with an accuracy of 0.01%, at least 10,000 bits have to be received. Therefore, the BER is displayed with three levels of accuracy.
Starting the measurements, no fractional part will be displayed. When sufficient bits have been received, the first fractional digit appears and at more information, also the last digit is displayed.
The accumulating accuracy of the BER measurement will be according to table 1:

max. amount per symbol	display in %	symbol
3200 bits	xx	.
6400 "	xx.y	.
12800 "	xx.y	.
25600 "	xx.y	.
51200 "	xx.yy +/- 0.004	.
102400 "	xx.yy +/- 0.002	.
204800 "	xx.yy +/- 0.001	.
409600 "	xx.yy +/- 0.0005	.

Table 1. Accuracy and display depending on bits received.

The "symbol" displays a kind of hour-glass, indicates how many bits were read. When the eighth symbol is displayed (a blank character) the final accuracy is reached (at 1200 Bd this takes appr. 3 minutes).

5. PRBS-data Generation

The Pseudo Random Binary Sequence has a period of 2^{20} bits, i.e. the sequence will repeat itself only after 2^{20} bits have been sent. The sequence is generated by using the Linear Congruential Method with the formula:

$$x(n+1) = (13 \cdot x_n + 1) \bmod 2^{16} \quad (x \text{ is 16-bit word})$$

This will lead to a sequence of 16-bit numbers with a period of 2^{16} . By sequentially transmitting the bits of all these numbers a total sequence length of 2^{20} is obtained. At the beginning of each BER-measurement the sequence is restarted.

For BER-calculation a special algorithm is used. This gives no limitation for the amount of test bits. A sudden increase or decrease in the amount of errors will be displayed immediately, even after 15 minutes of continuous testing.

Pager development tools and materials

OM4759 Antenna matching software

SOFTWARE TOOL FOR MATCHING LOOP ANTENNAS TO THE UAA2080 RECEIVER, OM4759

1. Introduction

The program PALOMA helps you to find the elements of a certain matching network for loop antennas for pager applications using the PHILIPS pager receiver chip UAA2080. It is based on approximations for the description of the electrical properties of small loop antennas.

PALOMA runs under DOS (3.3 or higher) and with 80286 machines (or higher). The software package consists of 4 files:

paloma.exe	the executable program and
paloma.col	tree files supporting the
paloma.key	on-line help function and
paloma.hlp	the coloured menu interface.

The PALOMA program may be used on monochrome and colour monitors.

More information about the theory of loop antenna's and matching these to the receiver is available in the chapter on Pager Antenna's.

By following the recommended procedure, one will find the optimum values for a matching network. A few preliminary parameters have to be set at first, e.g. frequency, antenna type and geometry. In a second step the frequency dependend antenna properties are being calculated. The third step includes the optimization of the matching network. The results may be saved on disk as a parameter list for later use when deriving more antenna designs from the same basic set.

2. Designing loop antenna's

PALOMA supports three different types of small loops:

- the single loop, consisting of only one rectangular loop,
- the multi loop made from one wire with a number of turns and
- the special loop, consisting of a number of parallel single loops.

Hints for selecting the optimum antenna structure are given in the chapter as mentioned.

The loop parameters for a rectangular loop are width and height. For non single structures, the distance between the loops becomes a sensitive parameter as well.

The excitation position has an influence on the electrical properties of the loop. Excitation is possible at any position of the rectangular antenna; corner excitation or the longer or shorter side of the rectangular loop.

3. Loop wire types and geometry

3.1 Wire types

PALOMA supports two different types of wire cross sections:

- circular and
- rectangular

When a rectangular cross section is selected, an equivalent diameter for a circular cross section will be calculated as all approximations in PALOMA are valid for a circular cross section only.

3.2 Loop material

It is possible to improve the antenna performance by using high conductive materials (coating). Typical materials to select from, are copper, aluminium, brass and tin. The loop material selection is of secondary influence only; the optimum antenna structure is more important.

4. Antenna feeding

The antenna feeding may have a big influence on the noise matching network parameters because it produces a capacitance parallel to the antenna impedance. PALOMA includes a simple model of two parallel wires with circular cross section in the calculation in order to take the additional capacitor and inductor into account. These added "paracitics" will sometimes be beneficial as this may improve the overall performance of the pager; a capacitor parallel to the antenna is often a good choice

Pager development tools and materials

OM4759 Antenna matching software

for optimizing sensitivity. In any case, either one avoid any feeding or the effect has to be taken into account.

4.1 Setting the noise matching parameters.

PALOMA is using a matching network consisting of four capacitors. This network effectively couples the inductive antenna to the input of the balanced, low-noise amplifier of UAA2080.

The non ideal capacitors are described by means of added (optional), ideal series resistors, which don't vary with the capacitance.

Furthermore it is possible to set the antenna noise temperature; this will describe the influence of the warm earth and cosmic radiation on the system noise figure for the selected frequency. PALOMA calculates this temperature using an approximation; this value may be changed at better information.

For the complete analysis, also the input capacitance of UAA2080T may be taken into account.

5. Optimization procedure

For noise matching purposes, a first target could be to optimize for minimum attenuation of the matching network, e.g. maximum overall gain. PALOMA supports still an other strategy in optimizing for maximum pager sensitivity. This sensitivity is calculated at a 3% BER (bit error rate) when using the decoder PCF5001T.

Different ways lead to the optimum values for the capacitors, depending on the position of the tuning point. To start off, non of the capacitors may be fixed in order to find the right range for further considerations. If a capacitor is found to become lower than 1 pF, this may be omitted.

The next optimization may be found by selecting a set of fixed capacitors, of slightly higher quality, to find the optimum dynamic range for the tuning point.

In a last step, changing to a tunable capacitor may require the other matching capacitors to get slightly different values.

Pager development tools and materials

Support material

Chipsets and support material

The following overview on chipsets and support material will give an impression on the the material available to the designer for paging systems. All material will be available through the local Philips Semiconductors office.

ICs and support material

Type number	Function	remarks
Integrated Circuits		
PCA5000	POCSAG decoder	not for new designs
PCF5001	POCSAG decoder	world standard, on board EEPROM
PCD5002	APOC1 decoder	new pager standard, to licensed customers
PCD5003	POCSAG decoder	New device, higher-end than PCF5001; more EEPROM, 2.5 V programming, I ² C control, message buffer
OM4031	Post-Detection filter	improved sensitivity, when not using Philips decoders (already build-in)
UAA2050	Direct Conversion freq. offset type	not for new designs
UAA2080	Direct Conversion receiver	low system costs, small pagers, also for APOC1
UAA2082	Direct Conversion receiver	UAA2080 optimized for 1-cell, also for APOC1
PCF8586	LCD-driver	flexible pager design, I ² C-bus for numeric pagers
PCF857x	LCD-driver	
PCF83CL782	microcontroller	low voltage, suitable for large display-drive
Support material		
OM4706	PCF5001 test board	quick set-up
OM4716	PCF5001 programming unit and test tool	versatile design-aid
OM4745	UAA2080 test board	optimized for 173 MHz
OM4746	UAA2080 test board	optimized for 288 MHz
OM4747	UAA2080 test board	optimized for 470 MHz
OM4748	UAA2080 test board	blank board
OM4759	Pager antenna matching software	optimizing Pager antennas

Pager development tools and materials

Support material

Technical reports and application notes

The following laboratory reports and technical notes are available on Pager systems, receivers, decoders and support materials. Most of the information in these reports is contained in this Application Book on Pagers.

Pager decoders

- Technical note, Nov. 1989, Start-up conditions for quartz crystals and PXE oscillators in digital clock circuits, by Werner Thommen
- Application note PCALHVCO8903, PCA5000T Paging decoder, features and applications, by Stephan Drude
- Application note ND06/89TC2, The improved POCSAG decoder PCA5000AT, by Stephan Drude, Thomas Rudolph
- Application note ND01/89TC2, Using the POCSAG decoder PCA5000T with data rates other than 512 bps, e.g. 1200 bps, by Thomas Rudolph
- Application note ND32/90TC2, Probability of lost call at PCA5000T and PCA5000AT solved by application, by Thomas Rudolph
- Application note HCO9101, PCF5001T Paging decoder with EEPROM features and applications, by Stephan Drude
- Application note ND52/90TC2, PCF5001T application hints, by Peter Hank

Pager receivers

- Application note AN94083 Pagers loop antennas, by Hans Zelle
- Application note HCO9002, Digital paging VHF/UHF Receivers UAA2050T and UAA2033T by Knud Holtvoeth, Thomas Rudolph
- Application note ETT91003, UAA2080T VHF/UHF paging receiver, by Rishi Mohindra

Pager development tools and materials

- Application note ETT94003, UAA2080H demonstration board, by Andre van Bezooien
- Application note ND29/90TC2, PCA5000 AT, PCF5001T POCSAG decoder demonstration module hardware, by Peter Hank
- Application note ETT92003, OM4718 Pager test and programming unit, hardware description and user's manual, by Hans Zelle, Stephan Drude, Thomas Rudolph
- Leaflets on pager support material, available for OM4706, OM4718

CHAPTER 7

QUESTIONS AND APPLICATION HINTS

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Question and application hints

Introduction

INTRODUCTION

Many questions have been asked at Philips Semiconductors "world" wide local sales offices and application laboratories on pager components and pager design. Many answers concern the same design subjects and trade-offs.

In this chapter we have summarized this information, hoping that the pager designers community can benefit with shorter design time and earlier introduction to the market.

Philips is recognised as a leading company for Direct Conversion Receiver techniques. An early design of a Single Chip receiver in this technology received the Queen's Award for Technology in the United Kingdom in 1989. Also the Export Achievement Award was granted to Philips in the United Kingdom in 1994 for one of its Pager products.

Question and application hints

Pager receiver design

GENERAL

In a radio-receiver, many methods exist for extracting the modulated information from the RF carrier frequency. Two main groups of methods may be distinguished as being of particular interest. In the first method, the incoming RF-signal is directly transformed to a Zero Intermediate Frequency (Zero IF); this type is also known as the Direct Conversion (DC) receiver. In the second method, the incoming signal is converted to a non-zero IF at first, sometimes followed by a conversion to a second non-zero IF; these type are known as the super-heterodyne receiver of double-super at two conversions. Mainly for historic reasons, the second principle has found its way into receiver designs for ease of tuning, reasonable selectivity and sensitivity and well-established design techniques.

Because of modern technology, other receiver principles are becoming feasible now that were not practical before. Also, other design criteria as ease of integration are becoming more important.

Philips has selected the Direct Conversion method as the (pager-) receiver design road to the future by designing the integrated receiver ICs UAA2050 and UAA2080. This choice offers the following advantages:

- Modern technology. This new technology has been developed for high system integration, while maintaining the established specifications. Other architectures, although often performing well, have been developed in the past mainly for other purposes.
- Technical performance of our direct conversion receiver UAA2080 compares well with other architectures. RF sensitivity, dynamic range, power consumption and spurious response are comparable to older system architectures or surpasses these.
- Easy and short design-in, once the new technology is understood. Only the front-end of a Direct Conversion receiver is handling RF signals; rest is low frequency design techniques. The UAA2080 handles a very wide frequency span, ranging from HF, through VHF up to UHF. Even outside the specified frequency range, the performance is remarkably good. This flexibility permits the designer to quickly adapt his system to a different

frequency band, using the same basic design and experience.

The lay-out of the pinning allows for more than one powering scheme. This permits the designer to optimally match the UAA2080 to the power source(s), using local trade-off's between system complexity and power consumption.

- Compliant to various data coding standards. The UAA2080 is compliant to data coding standards, that are two-level FSK with a bandwidth up to 9 kHz. Although designed for the pager POCSAG code, this versatility makes the receiver also suitable for other data systems.
- Very little 'real-estate' required on PCB for complete pager receiver design, as only one crystal and no further resonators or ceramic filtes are used. This feature allows for very small designs and simple logistics for frequency determining components. As an example; various complete pagers in watches have been designed and succesfully brought into the market using our Zero-IF receiver and decoder techniques.

Question and application hints

Pager receiver design

UAA2050 hints

SET-UP AND TUNING

- For good results on tuning accuracy and discriminator range, all specifications (and tolerances to those) should be followed closely. Also, most values in the application diagram in the objective specification sheet have been specified to give optimal results for those applications; deviation from those values should only be considered while observing the effects on the specification.
- In the tuning procedure it is not necessary to measure the oscillator frequency; it suffices to observe the data output DO, pin 14, and the IF output, pin 25.
- To start up, the appropriate set-up voltages are applied, including $V_p - 0.5$ V to the AFC test point, pin 3. Then the RF-signals (initially 1 mV) are applied at exactly the desired frequency, modulated with 600 Hz square wave to mimic a 1200 baud preamble, with a deviation of 4.5 kHz.
- The oscillator is tuned until a clean data waveform, with the correct polarity appears on DO: now the local oscillator is correctly tuned.
- Next, the multiplier tank and the RF-input circuits are tuned for maximum IF level at the IF output. This only serves to optimize the sensitivity.
- Finally, the AFC control voltage is removed from the AFC test point and the voltage is measured while the preamble is received. A value of 0.5 V \pm 20 mV indicates perfect tuning.
Observation of the output data DO, to have a clean wave-form, of the correct polarity, will be helpful.

ANTENNA MATCHING

- The antenna should be properly matched to the input of the circuit. This may be performed, using an RF transformer. Balancing of the input circuitry is important in terms of unwanted signal pick-up and optimizing the noise figure of the input amplifier. Especially while operating the application from an RF generator, the input balancing conditions should be

conserved when measuring performance to specification.

- In the application, the use of ceramic SMD-coils is permitted, except when using a matching coil transformer in the RF input circuit. This must be an air core type for optimum sensitivity.
A high Q (appr. 100) is important here.

DE-TUNING EFFECTS

- Improper tuning of the multiplier tank-circuit may result in occasional failing of the injection locking to the oscillator frequency. The resulting jitter of the multiplier stage, jumping between locked and free running states, may show up as a "noisy" spectrum, degrading the performance of the circuit. Also the temperature stability of the components around the oscillator and multiplier should be taken into account.

AVOIDING SELF RECEPTION AND LF PICK-UP

- Coupling of the VCO frequency with the RF amplifier should be avoided. This degrades the overall performance of the application, will create a DC-offset at the mixer output and will reduce the lock-in range of the AFC. Careful lay-out is important and some form of shielding (integrated in the enclosure) may be considered.
- Low frequency signals to the input circuitry may also impair the receiver's performance. Be aware of magnetic pick-up from a voice-coil type of alerter. The coil should be placed perpendicular to other coils or even be shielded off.

Question and application hints

Pager receiver design

UAA2080 hints on applications

ANTENNA DESIGN AND RF-AMPLIFIER

- For good sensitivity, make sure the impedance matching circuit between the antenna and the input RF-amplifier is of a good quality and the antenna has a low noise figure. Apart from a few hints on pager antennas given below, please also check the application note on pager antenna design.
- The antenna plus matching network should be as loss-less as possible. Due to skin effects the current will flow through a thin layer at the outer surface of the antenna and network conductors. For pure copper, the skin-depth at 170 MHz is 6.6 μm , getting lower for higher frequencies. A pager antenna having a rough surface will exhibit a longer conductive path, hence higher resistance, hence lower system Q and more noise. So it is better to have a clean antenna surface, which is coated against corrosion.
- The pager antenna usually is of a resonant-loop type of design. For best results, the tuning capacitor of this loop should be mounted as close as possible to the antenna and be a high quality. The input coupling (matching) capacitors will then be of lower influence.
- Also consider the input coupling capacitors; low quality, e.g. temperature drift and/or high loss factor will degrade the antenna tuning while contributing to a high overall noise figure. Please consult the application notes on UAA2080 for the input noise characteristics.
- The internal RF amplifier will be quite sufficient for the specified frequency range (up to 512 MHz.). In fact, the combination of RF-amplifier, phase-shifter, and mixer is well optimized for maximum sensitivity (typically -124 dBm. for 3% Bit Error Rate at 288 MHz.) together with good strong-signal behaviour (IP3 typically -28 dBm.).
- In power-saving situations an external RF amplifier might be considered. This external amplifier should exhibit equal or better performance RF performance at less current and/or lower supply voltage.

- To out-perform the internal RF amplifier, the external circuit should exhibit sufficient gain, at a noise figure of better than 3 dB at a current less than 1 mA.
- For optimum performance, the output of the external amplifier should be balanced before feeding the signals to the phase-shifter network.
- If an external RF amplifier will be used, the internal RF stage may be by passed. The bias resistor on pin 10 (H-version) should than be omitted for power saving; for safety reasons, pin 10 should be connected to pin 7 and 8 and the amplifier output pins 12 and 13 should be connected to Vp (e.g. pin 14).

COMPARING RECEIVER SENSITIVITY AND DATA FILTERING

- It is not simple to standardize the relation between the Bit Error Rate (BER) and the input sensitivity. When measuring at the output of UAA2080 (without data filter or decoder), a signal of 3 dB. above "threshold" (e.g. at -121 dBm) corresponds to 0.3% BER. This figure will rise sharply to 3% BER at input levels of -124 dBm (typical at 288 MHz, 1200 baud, 4 kHz deviation, 2.05 V supply; at 1.9 V). Peculiar BER behaviour around these sensitivity levels may point at local oscillator pick-up by the input amplifier.
- When comparing input sensitivity, BER etc. the following points are of interest:
- When looking at absolute sensitivity figures, make sure the measuring equipment is calibrated, as are the conditions at the measuring position. Although this is obvious, considerable differences are found between various types of equipment and between equipment of the same type.
- Also the type of measuring cable should be considered. Standard RG 58 cable exhibits appr. 0.5 dB/m at 450 MHz., some tin-coated types may be 3 - 6 times worse.
- When comparing sensitivities of pager systems including the antenna, care should be taken interpreting the data. Measurements done in a TEM-

Question and application hints

Pager receiver design

cell, may yield very good figures when maximally coupled to the generated RF field. In fact those figures may approach the free-field behaviour of the antenna. Many PTTs require the measurements in a TEM-cell to be done at 45 degrees intervals; the average sensitivity over 8 such intervals (360 degrees) will be compared to the required sensitivity.

Other test sites may simulate more practical operating conditions by measuring on "salt-pillars". The two sensitivity measurement types will yield many dBs difference as a result.

- When comparing sensitivity figures, be sure a measurements are done under equal terms of data filtering. Filtering of the data between the receiver and the decoder will yield extra dBs in sensitivity.
- When these extra dBs of sensitivity make a difference, the Philips Digital Post-Detection Filter for FSK data receivers OM4031T may be used or the Philips POCSAG paging decoder PCF5001; the latter incorporates this filter function.
- An other type of filter may be a second-order Bessel type filter using discrete components and an operational amplifier. Unless the sensitivity of the following decoder stage is high enough, this filter should be followed by a limiting section (in the same housing?). For 1200 baud, at 4 kHz deviation, the optimal filter band-width is appr. 800 Hz and the overall sensitivity gain of the pager system will be appr. 2 dB. Make sure the amplitude of the input signals to this filter will be within the linear range of the amplifier.
An even simpler system is a passive second-order RC-filter, followed by a limiter, under the same conditions. The measured sensitivity gain in this case will be appr. 1.5 dB.

SPURIOUS RESPONSE AND DE-TUNING EFFECTS

- In a direct conversion receiver, there is no image spectrum. This means no need for an input image rejection filter. The channel selectivity is provided by the low-pass IF filter in the UAA2080; the bandwidth may be selected by setting the gyrator current with a resistor between pin 21 and pin 22 (H-version), according to requirements of the application.
- One may find some sensitivity at the receiving frequency plus (or minus) an integer factor times the oscillator frequency. When properly tuned, the spurious rejection is always according to specification, i.e. 60 dB typical. In our demo boards we measure a spurious signal immunity of 65 - 70 dB.
- In many super heterodyne systems, a more likely figure for spurious reception is appr. 55 dB, mainly on the image frequency.
- The UAA2080 is a direct-conversion-receiver. This means that the data-output will still follow the transmitted information when de-tuning to either side of the correct frequency, as opposed to a frequency off-set type of "Zero-IF" system (UAA2033, UAA2050). On de-tuning, a slight data duty-cycle change may be observed on the DO output, but not more than appr. 40-60%. The main effect of this offset is an increase in the flank jitter for the bit, corresponding to the lower IF frequency, especially at low RF-levels.

LOW FREQUENCY PICK-UP

- In some applications, the antenna may pick-up some low frequency components, e.g. from the nearby digital (computer) board and/or pick-up from an (electro-magnetic type) alerter. This pick-up may influence the sensitivity of the pager. By decoupling the pager antenna for LF signals, this influence will be diminished.
- One way of LF decoupling consists of connecting a 10 μ F tantalum capacitor from the centre of the antenna loop to ground. Due to the parasitic series inductance, most tantalum capacitors will display a high enough impedance at the receiving frequency while having a low enough impedance for the unwanted LF component.
- Another method of decoupling the unwanted LF component is by means of a coil. An (SMD) coil of a few hundred nH., from the centre of the loop to ground, may be selected to be self resonant at the receiving frequency, thus creating a high impedance.

Question and application hints

Pager receiver design

AVOIDING SELF-RECEPTION

- As with all direct conversion receivers, coupling of the internal oscillator frequency with the RF amplifier should be avoided. This degrades the overall performance of the application and will create a DC-offset at the mixer output.
- Alternatively, one may check the amount of unwanted coupling, by checking the DC-component: If a weak, unmodulated RF-signal is applied to the receiver input, a sine wave will be present at TPI, pin 5 and TPQ, pin 6 (pinning for H-version). During tuning, the (unwanted!) varying DC term will be added to this sine wave and on an oscilloscope we see the TPI and TPQ signals to jump up and down.
- An other way to check LO pick-up is to measure this signal with a high-ohmic probe at the output of the RF amplifier, pin 12 and pin 13 (H-version), when no external input signal is applied. This pick-up level should be lower than -45 dBm.
- For fully switching of the mixer stages inside the UAA2080, a drive level of -18 dBm at the mixer input, pin 24 and pin 25 (H-version) will suffice. Make sure this level is not (very-much) higher. A high level at this position will only contribute to unwanted LO pick-up and spurious reception.
- Careful PCB lay-out is important as is the design and positioning of the antenna. We recommend a loop-type of antenna at 90 degrees to the PCB. In body-worn pager applications, with the PCB parallel to the body, this loop configuration also optimally exploits the "body-effect" for high receiver sensitivity. From experience we know, that with a well designed lay-out self-reception can be sufficiently minimised. Please refer to the application note on UAA2080 for further recommendations.

OPERATING UAA2080 OUTSIDE THE SPECIFIED FREQUENCY RANGE

- The minimum frequency of UAA2080 is specified at 25 MHz. The real minimum is determined by internal coupling capacitors around the multiplier. With a current level through the multiplier at 350 μ A, the

minimum operating frequency would be appr. 7 MHz. This could mean extended applications of the UAA-2080 (double conversion systems) at e.g. 10.7 MHz.

- The maximum frequency of UAA2080 is specified at 512 MHz. It is reported, that the circuit will also operate at (much) higher frequencies. For those design's a few hints will be given:
- When operating at 930 MHz., the local oscillator injection level at the input of the mixer stages, pin 24 and pin 25 (H-version) may become somewhat low. This L.O. level can be increased to around -20 dBm by means of two cross-coupled transistors (BFG 505) biased with a 2.7 k Ω resistor at appr. 400 μ A.
- At 930 MHz. a typical sensitivity of appr. -116 dBm. is measured (512 baud, 4 kHz, 2.05 V supply, data filter included). An extra RF pre-amplifier at appr. 1 mA. with only a few components will make-up for the sensitivity loss of the internal RF pre-amplifier. (a cascoded transistor stage with BFR 505, BC 858 plus additional R's and C's)
- A different approach is using the SA620 as a front-end down-converter to frequencies, acceptable to UAA2080. The SA620 exhibits a comforting 1.6 dB noise figure at 930 MHz. and a gain of 11.5 dB. Due to this gain, the UAA2080 has to handle relatively large signals, which may influence the IP3 figure of the back-end. An attenuator between UAA2080 and SA620 may be optimized for a better compromise between large signal handling capability and sensitivity while relaxing the matching requirements. The IP3 specifications of SA620 are more than adequate for pager applications, so a trade-off may be made. As an alternative, the SA601 with even lower noise and an external oscillator may be considered.
- As with all designs at these frequencies, care should be taken to the lay-out of the PCB. Track lengths are very important, especially when radiation of LO signals are considered and unwanted self-reception. In general, strip-line design techniques are recommended. Apart from short conductor lengths and low "enclosed radiation area" some form of shielding may be necessary for the oscillator and multiplier circuit parts.

Question and application hints

Pager receiver design

TRADE-OFF'S FOR COMPONENT COUNT AND TUNING COSTS.

- Trade-off's may be made between component/tuning costs versus performance. The following points will be of interest:
- The loaded-Q of the antenna input network in the application is high, therefore tuning is absolutely necessary. For optimum pager sensitivity, losses in this input network should be kept as small as possible. This means that the Q-factor of the trimmer capacitor (and other C's) must be sufficiently high (>300) at the working frequency. The trimmer quality at this position will be traded-off against the requirements for sensitivity.
- The RF-amplifier output tank circuit is a high-Q network and provides RF selectivity. The sensitivity reduces rapidly when the resonance circuit is not on frequency. Spreads in L2, L3, C7, C8, and C9 (please refer to the application diagram) have to be compensated by trimmer C6. We advise to use a trimmer at this position.
In principle the loaded Q of this resonance circuit can be reduced by changing the values of C7, C8 and C9. If the loaded Q is made sufficiently low then tuning the tank will not be necessary any more.
The trade-off here is reduced selectivity and therefore stronger spurious reception. Also the sensitivity will be influenced.
- The trimmer C15, tuning the oscillator output tank circuit may be used to minimize the spurious reception of the receiver, by optimizing the injection level to the frequency multiplier circuit.
The trade-off here is higher spurious response.
- The trimmer C12, tuning the frequency multiplier tank circuit, is determining the injection level to the mixers. A low-Q tank circuit means reduced spurious rejection, where a high-Q tank means reduced sensitivity if not properly tuned on frequency. This is not a critical setting, as long as the mixers are being fully switched. Again, spurious response is being influenced as a trade-off.

- In many applications, one or more of the trimming capacitors are being replaced by fixed capacitors after proto-typing, except for the crystal tuning. It appears that for those systems the specifications of UAA2080 allow for trade-offs when compared to the local requirements.
- A simplified application diagram may be worked out, with non-balanced tank circuits in both the RF amplifier and the frequency multiplier output. This will save two SMD coils and two SMD capacitors. The trade-off here, is reduced "common mode" rejection, caused by even order distortion. Although not recommended, this solution is subject to local considerations.
- Trimmer C17 is used to tune the crystal oscillator on frequency. A frequency offset of 2.1 kHz, at 1200 baud will cause a sensitivity degradation of appr. 3 dB. An oscillator crystal, having an overall temperature drift of ± 10 ppm (equals ± 1.7 kHz at 170 MHz) and an accuracy of 2.3 ppm nominal (equals ± 391 Hz at 170 MHz), already will be the cause of this 3 dB sensitivity loss.
At higher frequencies, the crystal requirements will be more stringent, so the trade-off for replacing C17 will be higher crystal costs.
- The oscillator circuit has been designed for optimum performance under low current conditions. A trade-off may be made between a higher motional resistance of the oscillator crystal (usually at a lower price) and somewhat more current through the oscillator circuit, by decreasing R5. For more background on the oscillator circuit, please refer to the application note of UAA2080.

BAUDRATES

- The UAA2080 may be used at many different baud rates; some points of attention may be worth noting:
- Make sure the slope of the modulating signal is chosen in accordance with the baudrate as this will reduce the required bandwidth on transmission and reception, e.g. 250 μ s at 512 baud and 1200 baud, 125 μ s at 2400 baud and 62 μ s (or 31 μ s) at 4800 baud.

Pager decoder design

Pager receiver design

- Running the UAA2080 at different baud rates will not affect the supply current consumption. Also changing the supply voltage within the specified range has virtually no effect on the supply current.
- The higher energy-bandwidth for the higher baudrate (at the same deviation of 4 kHz) will result in a reduced offset tolerance to the receiving frequency. Reported offset tolerance for 3 dB sensitivity reduction (4.0 kHz deviation at 470 MHz using a digital data filter), was: 2.0 kHz at 1200 baud, 1.6 kHz at 2400 baud and 1.6 kHz at 4800 baud.
- The input sensitivity may be affected when using different baud rates. The reported sensitivity at 3% Bit Error Rate, at 4.0 kHz deviation at 470 MHz using a digital data filter, was -125.8 dB at 1200 baud, -123.6 dB at 2400 baud and -119.7 dB at 4800 baud. The IF bandwidth of UAA2080 should be optimized for the energy spectrum at every baud rate in relation to the in-band noise.
- Using 4 kHz deviation, a baudrate of 1200 bps results in 3.5 periods per bit where 2400 baud only yields 1.7. The demodulator updates its logic outputs at every zero-crossing of the IF signal, either I or Q signal. As the number of zero-crossings is reduced at 2400 baud, the relative jitter of the edges increases. The post-processing circuits should accommodate for this behaviour.
- Loading the output DO, pin 3 (H-version), with a capacitor will add an extra low-pass filter between the output of UAA2080 and the decoder. Care should be taken with this extra filter. Degrading the slope of the outputted data will influence the overall Bit Error Rate, especially when using data sampling techniques at the input of the following data decoder. Also, extra noise could be added to the TPI and TPQ terminals if DO is capacitively loaded. A resistor of 47 K. to the DO output will solve this problem.

Question and application hints

Pager decoder design

GENERAL

More than one method exists for decoding the pager transmission message. The first, and most obvious selection is in the decision to do the decoding in hardware stand-alone circuit, or in software in a micro processor.

Philips has selected the hardware decoding method by designing the decoding ICs PCA5000A and PCF5001. This choice is offering the following advantages:

- low power consumption; (17 μ A for PCA5000A and 60 μ A for PCF5001). A microcomputer, accomplishing the decoding in software, will have to complete a decoding task before the next information arrives. This will require a high clock speed for a "standard" μ C (high power), or a dedicated μ C (high price).
- lower development cost and risk for the pager manufacturer. Since all data filtering, synchronisation, decoding, POCSAG protocol functions and error correction systems are catered for, the pager designer can concentrate on the (pager)user interface design, in many cases a more familiar task.
- real-time signal processing, including digital data filtering.
No extra storage required for input buffering of new information while signal processing is still in progress in the software.
- dedicated error correction for low software load. See lower development costs/risks
- higher software and μ C flexibility. Since most software/memory space consuming decoder functions have been catered for, the controlling μ C may be simpler, perform extra tasks, be of simpler, less time critical design and so may consume less power.
- two chip complete, beep-only pager solution. The high functionality of the Philips decoder ICs is permitting a pager design, using a receiver and decoder IC only. The power-saving, receiver controlling functions are inside the decoder together with (simple) user-interface functions. This permits the design of a simple, alert only pager allowing four different

cadences (messages) to be send to the owner; the user address and pager configuration information is stored in SRAM (PCA5000A) or EEPROM (PCF5001). The PCF5001 can recognise up to four different user addresses in two different frames. The decoder also takes care of some pager-status messages to the owner like: call alert, repeat alert, battery low, power up and out-of-range. Further features are silent call storage, programable call-termination conditions, duplicate call suppression, programmable hold-off time on duplicate call suppression and out-of-range indication.

Question and application hints

Pager decoder design

PCA5000A hints

PROGRAMMING

- A good way of checking, if the decoder has left the programming mode, is in looking at the receiver enable output pin (RE, pin 10). This output should enable the receiver to perform sampling of the synchronization code word position and the programmed code word positions in the respective frames.
- If the decoder is not sampling at all, the system may still be in the program mode.
- If the decoder is sampling at the synchronisation word positions only (and not at the proper program code-word positions), the clock frequency may be outside the normal range. The deviation of the clock frequency should not exceed 20 ppm from its nominal value, for the clock recovery algorithm to resume synchronization.
- In all cases, the rise and fall times of the power supply transients should not be excessive. A series resistor of 22 Ohm in series with the supply should damp transients efficiently when the decoder is decoupled with a capacitor of minimum 10 μ F. Switching transients may interfere with the decoder to resume its decoding functions after programming is finished. See also the application note on PCA5000T.
- In the "display pager" mode, the ON, OFF and SK pins do not have internal pull-down resistors, as the following circuitry will provide for the correct logic levels. If left unconnected to the micro-processor, ON (pin 18) should be connected to Vdd (pin 28) and OFF (pin 17) to Vss (pin 13). By modifying the level on SK (pin 16) the system is switched between SILENT and ON state. Also, the test input TS (pin 7) should not be left floating, but must be pulled low to Vss. When switching the power to Vss, (the supply terminal is negative, Vdd is substrate, is ground) this terminal may be left floating when not connected. Care should be taken, that the voltage on Vss will not rise to more than 0.9 V above Vdd. A resistor of 2.2 MOhm between Vb (pin 1) and Vss (pin 13) should take care of this situation.

PCF5001 hints on applications

PCF5001 AT DIFFERENT BAUD-RATES

- When using the PCF5001 at 2400 baud, the following points should be considered:
- The clock frequency (or connected crystal) should be 153.6 kHz.
- Minimum supply voltage is 1.8 V; supply current will be somewhat higher than at 1200 baud.
- The programming (via the SPF bits) should be for 1200 baud.
- All timings will be halved w.r.t. 1200 baud: alerts are one octave higher, data output rate will be 4096 i.s.o. 2048 baud, time-outs are halved, receiver establishment times halved etc.
Some PTTs may have problems with changed alert durations and frequencies, although the POCSAG standard itself only mentions the number of bleeps per call type and not the duration or the frequency.

INTERFACING PCF5001 TO A RECEIVER

- The versatile PCF5001 is designed to operate as a stand-alone pager controller or as a decoder interface between a pager receiver and a microcontroller. In most cases, PCF5001 will determine the on/off periods of the receiver via the receiver enable output RE (pin 14).
- When the receiver is switched off, RE = 0, the data input to the decoder DI (pin 5), is loaded with a pull-down current of 7 - 20 μ A (at an input voltage of Vdd). This will prevent random noise signals, mistaken for data input, to cause the decoder to respond.

Question and application hints

Pager decoder design

COMMUNICATION BETWEEN PCF5001 AND A MICRO CONTROLLER

- In display-pager mode, the internal pull-ups and pull-downs to the micro-processor interface are disabled, except for pin SR. This will reduce the supply current slightly.

Battery-low indication

- When using the battery-low indication as an input to a pager micro-controller, the following should be taken into account:
- Battery-sense input BS (pin 6) is not sensed during the "preamble receive state". Also, battery-low output BL (pin 24) is interrupted for 62.5 msec. when switching from SILENT to ON status. Further, battery-low alert and BL signal are reset as soon as an incoming call is alerted (in the ON status); they will not re-appear automatically after the 16 s. call alert time-out.
- When a call alert is cancelled by a pulse on SR (pin 21), the Battery Low alert and BL signal are restarted. They also re-appear when switching from ON to SILENT status.
- On using the PCF5001 - microcontroller combination, the μC can detect a call and cancel the alert by pulsing SR before the call alert has started, so preventing the battery-low detection switch-off condition. This is possible because the call alerts are started after a 52 ms delay (t_{ALD}) from a call data-transfer via DO/DS to the μC . (see also the specification of PCF5001)

Alphanumeric data transfer

- When transferring alpha-numeric data to a micro-controller via the DO (pin 26) and DS (pin 27) outputs of PCF5001, the following might be of interest:
- The consecutive byte delay t_{BYD} , when transferring message data to the micro-processor via DO/DS, is dependant on the crystal frequency: $t_{\text{BYD}} = 1454 \mu\text{s}$ at 32.768 kHz and 1210 μs at 76.800 kHz.

- Care should be taken handling the error flag bit: The 20th message byte of a message is not transferred after the 7th, but after the 8th codeword. The error flag bit, attached to the 20th byte is being determined by the 7th OR 8th codeword. These two conditions may lead to the situation, where the 20th codeword has been received correctly, but the 8th codeword, not correctly received, has set the error flag. This situation may lead to interpretation problems. To prevent misleading information, the software should check every 20th and 19th data byte; when the 19th byte had no error flag, the 20th byte was alright too. See also PCF5001 Application Hints.
- In case the entire message is correctly received and finished, but no "next-address" or "idle" codeword is generated after the last message codeword, a termination error will occur; this also hold for numeric pagers. Interpretation of this termination error should not lead to an incorrectly-received-message error.
- In the programming area of PCF5001, the bits SPF 18 and SPF 20-30 are available for general purpose storage. They do not influence the decoder operation in any way. Programming and reading must be done in the normal way. Make sure, the other SPF bits are not changed when using these spare bits, by re-programming them with their unchanged values. Also, unused addressing space (RIC) may be reused for other purposes, except for each enable bit. In this situation, the enable bit must be programmed to "1" (= OFF) to ensure that the info in the RIC location is not used to compare incoming address codewords with. One way of using these spare bits, is to store operational pager characteristics, that will not change during the pager's lifetime. Other, more ingenious ways are left to the designer. In total, 102 EEPROM bits have to be programmed for RICs and configuration management and 12 bits (minimum) are spare for the user.
- The microcontroller should use an asynchronous interface protocol when reading the EEPROM contents via data-out DO (pin 26) and data strobe DS (pin 27); the output clock rate is not constant due to internal timing and may vary considerably during transfer.

Question and application hints

Pager decoder design

Reading the EEPROM values by the μC is possible via the DO/DS serial interface in the "display-pager mode" (SPF01=1), by selecting the status on the ON (low), SK (high) and IE (high) pins. The "normal" pager modes (ON, OFF, SILENT) are not active now.

A rising edge on status request SR (pin 21), enters the EEPROM read-back mode, and a falling edge starts the EEPROM contents output via DS/DO after delay t_{SDD} .

During an EEPROM read operation, the reference clock output FL (pin 28), and LED indication output OL (pin 13), are undefined. This means that the FL reference clock signal cannot be used as a clock signal to a microprocessor during EEPROM read-back.

After EEPROM read-back has finished, the pager status is restored and pin FL and OL will resume normal operation.

- The out-of-range indication is interrupted when the call alert timer is active during an incoming call. If this is a problem to the μC , at least one of the following measures could be taken:
the Duplicate Call suppression should be enabled, Call Alert should be cancelled with one batch duration, the OR (out-of-range) hold-off time should be disabled.
The OR output, pin 25, will now immediately show the OR condition, regardless of the ongoing alert. If a hold-off time is required, this may be realised in software in the μC .

START-UP CONDITIONS

- The PCF5001 is "reset" by the internal power-on reset circuit as soon as the supply voltage rises past 1.2 V. The internal circuitry then waits for a clock signal for further activation of the decoder; without this clock signal, the decoder will not respond to key-presses or interface signals from a microcontroller. The decoder is intended to be powered-on continuously to act as a pager controller, at a typical operating current of 60 μA (at 1200 baud at 76.8 kHz. clock).
- As the PCF5001 is a fully static device, no further start-up delays will be encountered when using an external clock.
- On using the internal crystal oscillator, some start-up delay will be noticed. This delay is depending on the type of resonator; rather long start-up times have been observed.
- In a display-pager situation, the micro-controller should make the decoder insensitive to random signals on the interface lines by keeping the interface enable IE (pin 19) low at start-up. The decoder will enter the OFF status at power-up and no start-up alert will be generated.
- The contents of the EEPROM have to be programmed at first operation after delivery, no guarantees can be made to the initial contents. If one selects the EEPROM contents to be all zero, e.g. in a test set-up, this means to the decoder, that all RICs are enabled, the pager is in alert-only configuration at 512 baud (32.768 kHz crystal). See also "Synchronization".

SYNCHRONIZATION

- The PCF5001 is containing an algorithm for keeping track of the incoming information and synchronization to the POCSAG transmission protocol. Under design conditions, address codewords containing all zero's or ones may be transmitted as part of a test set-up. Such codewords make it difficult for the decoder to maintain synchronization, because there are no bit-transitions to be detected. Such a test set-up should be avoided, as it may lead to erroneous conclusions about the pager's sensitivity or sensitivity differences for information in different frames.
- The decoder always checks a group of 32 bits for a preamble, sync. word address or message codeword.
- The length of a standard preamble is 1 batch + 1 code word (544 + 32 bits). This ensures that a pager in Carrier Off state, activating itself one codeword per batch-duration, will always notice the start of a transmission.
- Before the preamble is deemed detected, at least 28 out of 32 bits must match a preamble pattern. This is equivalent to a tolerance of 4 random errors per 32 bits.

Question and application hints

Pager decoder design

A synchronization word is deemed detected, when at least 30 out of 32 bits are correctly matched to the sync. word pattern; this corresponds to a tolerance to 2 random errors.

ERROR CORRECTION

- The POCSAG code permits transmission errors to be corrected at the receiver (decoder) side. Transmission errors may occur in many forms; some are more likely to happen than others.
Two main error correction schemes are adopted; correction of one or two bit errors at random positions or four bit burst errors.

The POCSAG Standard does not specify a particular correction method, but leaves the choice to the designer. In any case, the method to be selected will have to exhibit a good call success rate and a low false alarm rate.

For the PCF5001 the 4 bit burst method has been selected for the address decoding and a single bit random method for the message contents.

Comparison of a two bit random error method against the four bit burst in the address word under laboratory test circumstances, shows that 90% call success rate is achieved at 2.7% Bit Error Rate for two bit random method against 1.7% at 4 bit burst. At this level, the 1% BER difference corresponds to approximately 0.5 dB sensitivity difference.

Using bit error patterns from radio channels in field tests, this difference reduces to 0.25 dB, on or below the edge of measuring accuracy.

PRIVATE AND GROUP CALLS

- The PCF5001 supports up to four different user addresses (RIC) in two different frames (two per batch). This means, that the same pager may be used for private messages, (selected) group calls and general (news) services.
- In PCF5001, all four RICS can be separately enabled or disabled by EEPROM programming. Of the 21 bits of a full user address, the first 18 bits are actually being transmitted, while the last three bits are determined by position of this transmission within the

batch (eight frames in a batch). The pager will only look for information in the frame, it is programmed for. When two frames (in one batch) are enabled, the pager will be active during the sync. word plus 2 frames. This will affect the power consumption of the pager somewhat; the trade-off between ease of multiple pager address operation vs shorter battery life should be made by the manufacturer (customer).

OVERRIDE SILENT CALLS

- The PCF5001 may be used in the ON, OFF and SILENT state. In the SILENT state, the alert generation is normally non acoustic.
The address positions (RIC) C and D can be programmed to enable a SILENT OVERRIDE call to reach the acoustic alarm (on the AL output, pin 15 and AH output, pin 12); this facility permits urgent calls to reach the immediate attention of the user even though the pager is in SILENT state.

NEGATIVE SUPPLY VOLTAGE

- The PCF5001 is produced in an IC process, having the substrate connected to the positive supply pin Vdd. The circuit's supply current is drawn from the negative supply pin Vss; power switching should therefore preferably be done via this terminal.
- Usually, all circuit references are made with respect to a common "plane". In PCF5001, this common plane is advised to be connected to the circuit's substrate; the positive supply pin. All voltages in the data sheet are referenced to substrate and will therefore appear as a negative value.
- All decoupling for this circuit should also be done to this "ground-plane", that should be electrically separated from "ground-planes" referencing to a negative supply.
- It also follows, that the voltage , convertor produces a doubled voltage (on pin V_{REF}) referenced to the positive supply pin, V_{dd} so a voltage that is more negative than the negative supply pin. This voltage also shifts the level of the interface lines to the microprocessor.

Question and application hints

Pager decoder design

VOLTAGE DOUBLER

- The voltage doubler is designed to operate with a capacitor of 100 nF between CP, pin 3 and CN, pin 2. Changing this capacitor hardly changes the value of Vref, but will change the ripple form as rise and fall-times are affected.
A reservoir capacitor of 10 µF should be connected between Vref and Vdd. The value of this capacitor largely determines the ripple on Vref: the larger the capacitor, the lower the ripple and the higher the convertor efficiency.
The ripple voltage is also proportional to the output current.
In general the doubler is capable of delivering 600 µA at 2.7 V output on a 2 V supply and 900 µA at 4.5 V output on a 3 V supply. Using the internal voltage doubler, automatically takes care of the logical voltage levels of the interface to the microprocessor.

PROGRAMMING THE EEPROM

- At programming, the supply voltage for the decoder should be typical -5.0 V, minimum -4.5 V; according to the data sheet.
Some pager designers have reported, that programming is possible above 3.3 V. Although this is not guaranteed, sample testing has shown minimum programming voltage to be between 2.7 and 3.1 V at 25 °C.
- Care should be taken during programming to ensure that the voltage on the reference pin Vref (pin 1), does not exceed the maximum value specified when using the voltage doubler. With respect to Vdd, the voltage on Vref should not exceed Vss - 0.8 V.
- A better way is to always start programming by first disabling the voltage doubler, then programming the addresses and finally enabling the voltage doubler again as a last programming action.
- When connected to the UAA2080 receiver, the programming voltage may also reach the receiver. Make sure, the receiver is disabled during programming by setting RE, pin 14 at low level. This is achieved by selecting the OFF status on the PCF5001.
- Although the UAA2080 is specified at an operational voltage range of 1.9 V - 3.5 V, the limiting value on Vp is 8 V (all ground pins connected together). The programming voltage for the decoder at 4.5 - 5 V appears not to harm the receiver when switched off at RE = 0 V.
- In the application diagrams a diode is used to disconnect all other pager circuits (receiver, microprocessor) during programming at or above 4.5 V. This precaution is connected to these particular circuits and may be omitted when not necessary. When using a receiver type UAA2033 or UAA2050, this safety precaution is a must; it may be better to also check the µC.
- Care should be taken with the decoder crystals, connected to X1 (pin 9) and X2 (pin 10) of the decoder. At "normal" pager operation, the supply voltage is low enough to have the crystal run within the specified power limits, usually around 1 µW. At the programming voltage level of 5.0 V, the crystal dissipation may go up to 2 µW. The manufacturer should be consulted for the effects on the crystal lifetime under these conditions.
- EEPROM programming/verifying is possible at high clock rates.
Although usually clock rates of 32.768 kHz or 76.800 kHz will be used, a clock frequency of 153.6 kHz is also permitted. It is reported, that clock frequencies at least up to 500 kHz may be used with good result.

Question and application hints

Development tools and materials

AVAILABLE OPTIONS

- The Test and Programming Unit OM4718 is designed as a development tool for the decoders PCA5000ATD and PCF5001. Although being a flexible tool, not all functions inside the decoders may be reached:
- The Duplicate Call Suppression option cannot be disabled, this is fixed to the "enabled" position.
- The Repeat Alert option is also permanently enabled. This option is intended to make the user aware of the fact that a call alert was not cancelled and is still in memory.
The Alert time can be reduced to 2 seconds, by selecting the "Pager Test Mode"; the alert level then is "low", which is normal for the first 4 seconds of an alert.
- There is no option for High Level Alert testing through the TPU; a High Level Alert may be measured directly at the alert output AL (pin 23), preferably through a buffer stage.
- For further information on the OM4718 please refer to the "Pager development tools and material" OM4718.

LOW VOLTAGE TESTING

- When connecting the OM4718 to the PCF5001T demonstration board, OM4706, be aware of testing the decoder under low voltage conditions.
In the TPU, a series diode is placed in the Vbat. line to prevent dis-charging of the batteries during EEPROM programming. This diode accounts for 0.6 - 0.7 V drop of the supply voltage. Replacing this diode for a Schottky-type (e.g. a Philips BAT 85) will reduce this voltage drop.
When operating the OM4706 in a stand-alone position (with a link between connector pins 14 and 15), or together with a receiver board, there is no problem and the decoder will work well down to 1.5 V.

BAUD RATES

- The decoder may be programmed through the TPU, OM 4718, to run at different baud rates. This baud rate programming in the decoder is accomplished by means of the control bits SPF 02 and SPF 03. The crystal has to be selected accordingly.
- Using the TPU, SPF 03 will be programmed at a logic 0 and SPF 02 may be selected through the dip switch DIP 3 at OM4718. Through this set-up the following settings may be accomplished:
512 baud at 32.768 kHz, SPF 02 = 0
1200 baud at 76.800 kHz, SPF 02 = 1
2400 baud at 153.600 kHz, SPF 02 = 1

Other settings for SPF 02 and SPF 03 are blocked when using the TPU. For testing through the TPU, only the options for 512 baud and 1200 baud may be selected.
- The decoder board OM4706 is equipped with crystals for 32.768 kHz and 76.800 kHz. Modification to 153.600 kHz should be done by the user.

ALERter ENHANCEMENTS

- To enhance the output capability of the alerter, it may be useful to select an alerter of lower impedance than is on the decoder board OM4706 at present. The (electro-magnetic) alerter impedance on the board is 50 Ohms.
The efficiency of the alerter is important. Apart from a high efficiency alerter device, a proper acoustic transformer from the transducer to free air (encasing, acoustic horn) will enhance the efficiency.

Question and application hints

Crystal and PXE oscillator considerations

INTRODUCTION

Quartz crystals and ceramic resonators (PXE resonators) are widely used as timing elements in integrated circuits. For many applications the important question is not the accurate oscillation frequency, but a guaranteed start-up. Typical questions are:

- Which circuit elements are important for the oscillator's operation?
- How must the resonator and the oscillator circuit be specified to ensure operation under worst-case conditions?
- Can a quartz crystal in a given circuit be replaced by a lower-cost PXE resonator?
- Why does the circuit no longer oscillate if a 4 MHz crystal is replaced by a 32 kHz crystal?

After a short oscillator circuit review, the start-up situation is explained graphically in the impedance plane. Simplified analytical expressions are then derived which describe the safe start-up range and allow the influence of the important circuit parameters to be calculated. Special emphasis is placed on CMOS circuits. The accurate frequency calculation and the tuning range, which are well documented in other publications [1,2] are not discussed in this paper.

In the second part of this chapter the frequency pulling of quartz resonators is discussed. It will be explained that the pulling range is coupled to the overtone of the particular crystal vibration mode. Also the influence of the material resistance will be considered.

Question and application hints

Crystal and PXE oscillator considerations

START-UP CONDITIONS FOR X-TAL AND PXE OSCILLATORS

1. OSCILLATOR EQUIVALENT CIRCUIT

1.1 Basic circuit

The standard oscillator circuit is the so-called Pierce oscillator. The amplifier is an inverter with a phase shift of 180° . The resonator is in the feedback path and provides, together with the capacitors at the input and output, the additional 180° phase shift. Oscillation will start if the loop gain at 360° phase shift is higher than one. The oscillator amplitude increases until the over-all loop gain is reduced to one through non-linear effects of the amplifier.

Because the oscillation amplitude is small initially, small signal equivalent circuits can be used to describe the start-up conditions.

1.2 Amplifier equivalent circuit

The inverting amplifier may be realized through many different circuits. Bipolar or MOS transistors can be used as active elements with various feedback schemes to bias the inverter in the active region. All these circuits can be described by an equivalent circuit (Fig.2), which contains as an active part a current source, which is controlled by the input voltage and RC components between all three terminals.

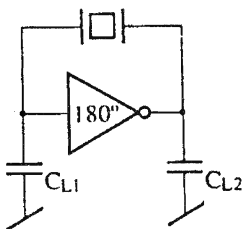


Fig. 1 Pierce oscillator

Referring to the equivalent circuit, the transconductance g_m is the most important parameter of the amplifier. C_{A1} , C_{A2} and C_F are only partially determined by the transistor capacitances, the main part is due to the elements protecting the circuit against static discharge, the bond

pads and wiring capacitance (bonding wires, lead frame, socket capacitance).

C_{A1} and C_{A2} present no problem, as they appear in parallel with the load capacitors C_{L1} and C_{L2} which can be

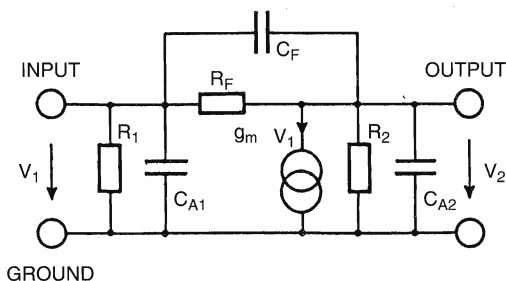


Fig. 2 Equivalent circuit of the inverter amplifier

adjusted accordingly. However the feedback capacitor C_F , which may have a value of several picofarads (input and output pins are usually adjacent), cannot be directly compensated for. As will be seen later, the resistors R_1 and R_2 cause unwanted phase shifts. Therefore their resistances should be as high as possible. The feedback resistor R_F further attenuates the oscillator. Its influence dominates in low frequency oscillators.

Fig.3 shows the typical performance of two CMOS inverters. The transconductance is the sum of the N- and the P-side. For a conventional inverter, the transconductance (and also the current consumption) is strongly dependent on the supply voltage. Source feedback resistors can be used to reduce this effect.

Independent of the degree of the feedback there exists a strong correlation between the transconductance and the output impedance: the small signal output conductance $G_2 = 1/R_2$ is in a first order approximation proportional to the transconductance g_m .

For CMOS circuits the elements of the equivalent circuit remain constant up to the frequencies of interest. This means that the values for g_m and R_2 can be measured at DC or at low frequencies and need not to be determined at the oscillating frequency.

Question and application hints

Crystal and PXE oscillator considerations

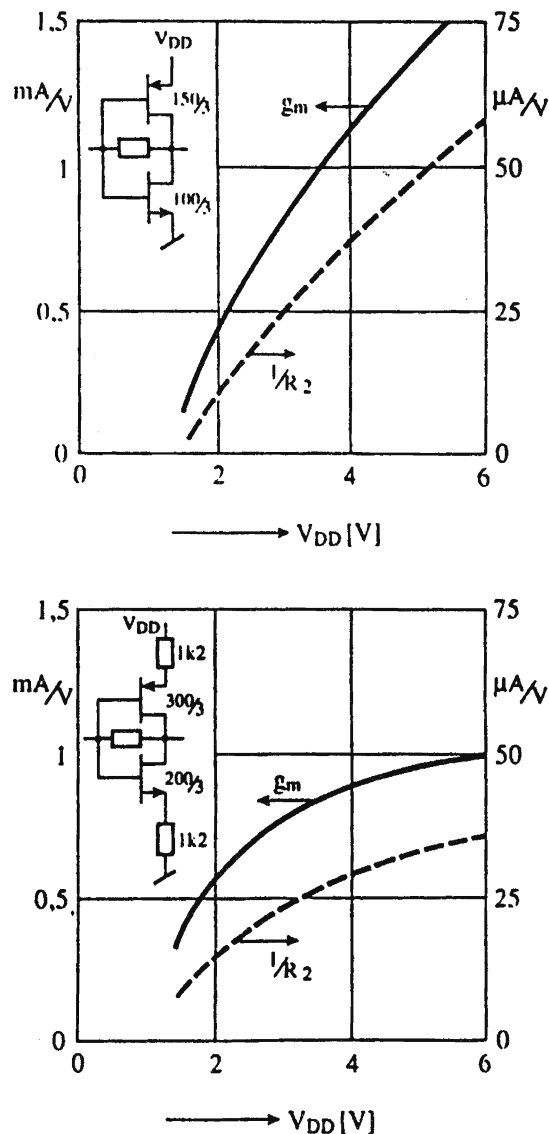


Fig. 3 Transconductance and output impedance of a CMOS inverter without and with source feedback resistors

1.3 Resonator equivalent circuit

It is well known from the literature that an electro mechanical resonator can be represented in the neighbourhood of the resonance frequency by a series connection of a large inductance L_x , a small capacitance C_{x1} and a damping resistance R_{x1} in parallel with the static capacitance C_{x0} (see Fig.4). The equivalent circuit of a ceramic resonator sometimes contains an additional parallel resistor R_{x0} . If such a resistor is specified it can be combined with the feedback resistor R_f of the amplifier for the purpose of calculation.

The series resonance frequency f_s is defined as the resonance of the series branch:

$$f_s = \frac{1}{2\pi\sqrt{L_x C_{x1}}}$$

The somewhat higher "parallel resonance" frequency f_p is given by the resonance of the series branch in parallel with the static capacitance C_{x0} (which results in a series connection of the two capacitors C_{x1} and C_{x0} whereby C_{x0} is always much larger than C_{x1}).

$$f_p = \frac{1}{2\pi\sqrt{L_x \frac{C_{x0} C_{x1}}{C_{x0} + C_{x1}}}} \approx f_s \left(1 + \frac{C_{x1}}{2C_{x0}}\right)$$

The oscillator frequency always lies between f_s and f_p . Table 1 shows typical values for 5 different resonators. Compared to the ceramic resonator, the quartz crystal has a much higher effective inductance and a lower dynamic capacitance C_{x1} which results in a significantly smaller range between f_s and f_p . Another important difference is the much larger static capacitance C_{x0} of the ceramic resonator.

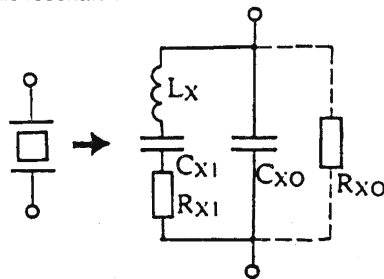


Fig. 4 Resonator equivalent

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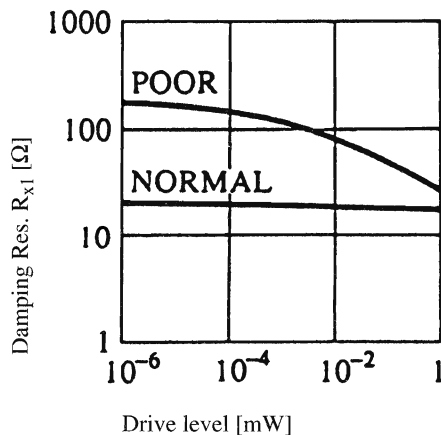
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Material	Quartz	Ceramic	Quartz	Ceramic	Quartz	
f_{os}	0.0328	0.455	3.6	3.6	16	MHz
L_x	$7.8 \cdot 10^6$	8.2	130	0.54	5	mH
C_{x1}	0.003	15	0.015	3.6	0.02	pF
C_{x0}	1.5	250	4.5	35	4.5	pF
R_{x1}	20k	10	50	15	10	Ω
f_p/f_s	1.001	1.038	1.0017	1.05	1.002	

Tab. 1 Typical circuit parameters for 5 different resonators

The damping resistor R_{x1} is not constant; it depends somewhat on the vibration amplitude and unfortunately increases for low power levels. Since oscillation starts from zero (i.e. noise) we have the worst case condition for R_{x1} at start-up. This "drive-level dependency" effect is not very large for quartz crystals of a standard quality, but cheap, low-quality crystals can show a significant increase (see Fig.5). Such an excessive damping is often hard to detect, because it can show a large hysteresis. This means it can disappear for a long time after the crystal has been excited with a certain power level.

Tab. 1 Typical circuit parameters for 5 different resonators

Fig. 5 Damping resistance R_{x1} as circuit a function of the drive level(3)

2. OSCILLATION EQUATION

Fig.6 shows the equivalent circuit of the complete oscillator. The feedback elements of the amplifier are combined with the resonator. The resulting impedances are:

$$Z_1 = \frac{1}{j\omega C_1} \parallel R_1$$

$$Z_2 = \frac{1}{j\omega C_2} \parallel R_2$$

$$Z_3 = \left(R_{x1} + j\omega L_x + \frac{1}{j\omega C_{x1}} \right) \parallel \frac{1}{j\omega(C_{x0} + C_F)} \parallel R_F \quad (1)$$

The basic oscillation equation is derived from the equivalent circuit of Fig.6B. The output voltage v_2 is:

$$v_2 = -g_m v_1 [Z_2 \parallel (Z_1 + Z_3)] \quad (2)$$

The loop gain is one, if the voltage fed back to the input is equal to the initial input voltage v_1 .

$$v_1 = v_2 \frac{Z_1}{Z_1 + Z_3} \quad (3)$$

Equation (3) together with (2) gives the steady state oscillation condition:

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$$g_m = -\frac{Z_1 + Z_2 + Z_3}{Z_1 Z_2} \quad (4)$$

The circuit elements (1) are now inserted into (4), which gives an equation with ω as a variable. Since g_m is a real number the imaginary part of (4) has to be zero. This leads to a quadratic equation with two solutions for ω and therefore also for g_m . As will be seen later, these two solutions for g_m give the maximum value for which an oscillation is possible. It has already been shown in previous publications (4,5) that start-up conditions are only fulfilled if the trans-conductance is in a certain range, but the derived equations are either too complicated (computer solution) or too much simplified (no resistive components other than R_{x1}).

Equation (4) together with (1) can of course be accurately solved with a short computer program, but at the same time the relation between the circuit parameters is lost. An exact analytical solution is also possible, but yields long expressions so that the overview is also lost. A good understanding of the circuit behaviour can be obtained from a vector diagram in the impedance plane. Equation (4) is rewritten in the form:

$$-g_m Z_1 Z_2 = Z_1 + Z_2 + Z_3 \quad (5)$$

Since the frequency range of interest is very small (between f_s and f_p , see table 1), we can make the following simplification: Z_1 and Z_2 are considered constant (ω is replaced by ω_s), the only important impedance variation as a function of the frequency results from the series branch of the resonator, where the imaginary part is given by the difference of two very large numbers ($\omega L_x - 1/\omega C_{x1}$). The two sides of (5) are now plotted as a locus in the impedance plane (Fig. 7). The left side of the equation is a straight line with g_m as a variable (the negative sign is due to the 180° phase shift of the inverter). The right side is a very large circle with ω as a variable. The important properties of the circle $Z_3(\omega)$ are derived in Appendix A. It has to be pointed out, that for all 5 oscillators given in table 2, the radius r_z of the impedance curve $Z_3(\omega)$ is very much larger than Z_1 , Z_2 , and X_{x3} , so that Fig. 6 is not to scale. The intersection of the line $-g_m Z_1 Z_2$ with the locus of the impedance ($Z_1 + Z_2 + Z_3(\omega)$) give the two solutions for g_m . Oscillation is only possible, if g_m is in the range between $g_{m \min}$ and $g_{m \max}$. This can be explained as follows: in the

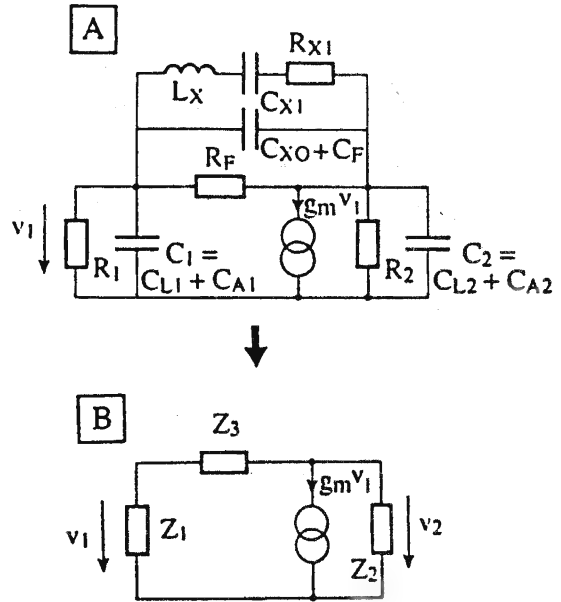


Fig. 6 Equivalent circuit of the complete amplifier

start-up situation we have no steady state condition, which means that equation (5) is not fulfilled. The oscillation start with a small amplitude and increases. During this phase, electrical energy is pumped into the storage elements L and C of the circuit. This is a loading effect which can be represented by an increase of the damping resistor R_{x1} and an increase of the real part of Z_1 and Z_2 .

The increased damping resistor leads to a smaller diameter of the impedance circle (see equation 16), the increased real part of Z_1 and Z_2 causes a counter clockwise rotation of the line $-g_m Z_1 Z_2$. Both effects move a point which does not lie between $g_{m \min}$ and $g_{m \max}$ even further away from an intersection with the locus ($Z_1 + Z_2 + Z_3$), so that the loop gain equation can never be fulfilled. For a transconductance between $g_{m \min}$ and $g_{m \max}$, the oscillation amplitude increases, the inverter enters nonlinear regions, and the average transconductance output impedance decrease (angle δ in Fig.7 increases) until a steady state condition is reached.

The start-up time depends strongly on the quality factor

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of the resonator and on the DC-conditions at $t = 0$. The calculation of the start-up time is thoroughly treated in the paper of A. Rusznyak [5].

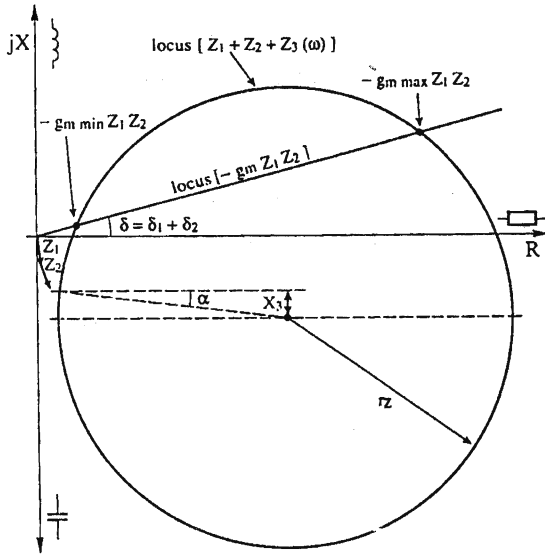


Fig. 7 Equation (5) plotted in the impedance plane. The left hand side is a straight line with g_m as a variable, the right hand side is a large circle with ω as a variable. The two solutions of the equation are given by the intersections.

3. APPROXIMATION FORMULAE

3.1 Conditions

With a few assumptions, it is possible to get manageable analytical expressions for the minimum and the maximum transconductance.

These assumptions are:

a) The real parts of Z_1 and Z_2 are small compared to the imaginary parts.

$$\tan \delta_1 = \frac{\operatorname{Re} Z_1}{\operatorname{Im} Z_1} = \frac{1}{\omega R_1 C_1} \ll 1$$

$$\tan \delta_2 = \frac{\operatorname{Re} Z_2}{\operatorname{Im} Z_2} = \frac{1}{\omega R_2 C_2} \ll 1$$

The real and imaginary parts are approximated by:

$$\operatorname{Im} Z_1 \approx |Z_1| \approx \frac{1}{\omega C_1} \quad (6)$$

$$\operatorname{Re} Z_1 = \operatorname{Im} Z_1 \cdot \tan \delta_1 \approx \frac{1}{R_1 (\omega C_1)^2} \quad (7)$$

$$\operatorname{Im} Z_2 \approx |Z_2| \approx \frac{1}{\omega C_2} \quad (8)$$

$$\operatorname{Re} Z_2 = \operatorname{Im} Z_2 \cdot \tan \delta_2 \approx \frac{1}{R_2 (\omega C_2)^2} \quad (9)$$

b) Angle α is small (see Fig.7). This means:

$$(C_{x0} + C_i) \ll 17 R_{x1}$$

c) Z_1 and Z_2 are much smaller than the diameter of the locus $Z_3(\omega)$.

d) The feedback resistor R_i is very much larger than the damping resistor R_{x1} of the resonator.

When looking at the numerical values of a specific circuit, one sees that conditions b), c) and d) are always fulfilled; only condition a) can cause some problems. From Fig.7 it is obvious that oscillation is impossible if the sum δ of the two loss angles δ_1 and δ_2 approaches 90° . For a stable design it is important therefore to keep the value δ as small as possible. The error of the approximation formulae does not exceed ten percent, provided that the angle δ stays below 30° .

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3.2 Maximum transconductance

From Fig.7 we get directly:

$$g_{m \max} Z_1 Z_2 \approx 2 r_z$$

The radius r_z of the impedance circle is derived in Appendix A, equation (16). Together with equations (6) and (8) $g_{m \max}$ becomes:

$$g_{m \max} = \frac{C_1 C_2}{R_{X1} (C_{X0} + C_F)^2 + 1 / (\omega R_F)^2} \quad (10)$$

For oscillators in the Megahertz range, the first term of the denominator dominates and the influence of the feedback resistor is negligible. However for oscillators under about 100 kHz the second term becomes the dominating part and the maximum allowed transconductance is strongly reduced by the feedback resistor R_f (See Fig.9).

3.3 Minimum transconductance

The minimum transconductance is usually of much more interest than g_m max. The derivation which takes a bit more space is done in Appendix B. The result is:

$$g_{\min} = \left(2 + \frac{C_1}{C_2} + \frac{C_2}{C_1} \right) \left[R_{X1} \omega^2 (C_{X0} + C_F + C_L)^2 + \frac{1}{R_F} \right] + \frac{C_2}{R_1 C_1} + \frac{C_1}{R_2 C_2} \quad (11)$$

Where C_L is the series connection of C_1 and C_2 :

$$C_L = C_1 C_2 / (C_1 + C_2)$$

The first term of equation (11) is usually the dominating part. For a given load capacitance C_L it is proportional to the function $(2 + C_1/C_2 + C_2/C_1)$ which is shown in Fig.8. It has a minimum for $C_1 = C_2$. In circuits where no frequency tuning is required, it is therefore recommended to use more or less symmetrical load capacitors.

For $C_1 = C_2$ equation (11) simplifies to

$$g_{\min} = 4 R_{X1} \omega^2 (C_{X0} + C_F + C_L)^2 + \frac{4}{R_F} + \frac{1}{R_1} + \frac{1}{R_2} \quad (12)$$

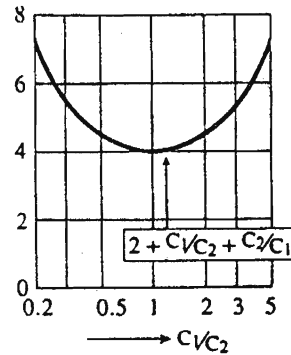


Fig. 8 The necessary transconductance increases if the capacitive loading of the resonator is not symmetrical. See formula (11).

3.4 CMOS circuits

For CMOS inverters a further simplification is possible. The input impedance is usually a pure capacitance ($R_1 = \infty$). The output conductance $1/R_2$ is more or less proportional to the transconductance g_m (see Fig. 3). A safe value is:

$$R_2 \approx 20 / g_m$$

Equation (11) becomes therefore:

$$g_{\min} = \frac{(2 + C_1/C_2 + C_2/C_1)}{1 - C_1/20C_2} \left[R_{X1} \omega^2 (C_{X0} + C_F + C_L)^2 + \frac{1}{R_F} \right]$$

For the condition $C_1 = C_2$ the minimum transconductance is:

$$g_{\min} = 4.2 \left[R_{X1} \omega^2 (C_{X0} + C_F + C_L)^2 + \frac{1}{R_F} \right] \quad (14)$$

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Material	Quartz	Ceramic	Quartz	Ceramic	Quartz	
f_{os}	0.0328	0.455	3.6	3.6	16	MHz
$R_{x1\ max}$	40 k	25	120	40	20	-
$C_{x0\ max}$	3	350	7	50	7	pF
$C_1 = C_2$	15	100	20	50	20	pF
C_f	3	3	3	3	3	pF
R_f	10	2	1	1	0.5	MΩ
$g_{m\ min}$	1.7	141	107	527	348	μA/V
$g_{m\ max}$	0.06	3.15	28.7	21.9	182	mA/V
$g_{m\ max}/g_{m\ min}$	34	22	267	41.5	523	-

Tab. 2 Allowed transconductance range for the 5 resonators of Table 1. Calculations are done according to equations (10) and (14) with worst case values for R_{x1} and C_{x0} .

4. DISCUSSION AND GUIDELINES FOR DESIGN

Table 2 shows the range of transconductance for the 5 resonators of Table 1 in a typical oscillator circuit. The calculations are done with worst case values for R_{x1} and C_{x0} , which are usually two to three times higher than the specified typical values.

There are several interesting points to be noted:

- a) The necessary transconductance does not depend on the dynamic elements L_x and C_{x1} of the resonator. L_x and C_{x1} determine the oscillating frequency. For specifying the frequency of the quartz crystal it has to be kept in mind, that the effective load capacitance seen by the crystal is not only C_L but $(C_L + C_f)$.
- b) The large static capacitance C_{x0} of ceramic resonators results in a rather high $g_{m\ min}$ and in a strongly reduced $g_{m\ max}/g_{m\ min}$ range.
- c) For Megahertz quartz oscillators, $g_{m\ min}$ is mainly determined by R_{x1} and the load capacitance; the influence of the feedback resistor can usually be neglected. The maximum allowed transconductance $g_{m\ max}$ is very large and usually causes no practical problems.

- d) For low frequency oscillators (which are not specially designed for low current consumption), start-up is often a problem because the inverter exceeds the maximum allowed transconductance. If a 32 kHz oscillator has to be built with a given inverter of $g_m = 1\text{ mA/V}$ and $R_2 = 20\text{ kΩ}$, it will not work if the crystal and the capacitors are connected directly to the inverter because the transconductance is too large and the phase shift ($90^\circ - \delta$) at the output is much too small.
A solution is to connect a large resistor R_s in series with the output (Fig. 9). This resistor reduces g_m by the factor $R_2/(R_2 + R_s)$ and increases the output impedance to $(R_2 + R_s)$ so that an acceptable phase shift is reached at the output. Without this series resistor the circuit will not work at all, or it will oscillate at a harmonic frequency of the crystal, where the oscillation conditions are fulfilled.

- e) The transconductance range of a low frequency quartz oscillator is strongly determined by the feedback resistor R_f (see Fig. 10). The feedback resistor has to be at least several Megohm to ensure an adequately safe operating range. Very high feedback resistors on the other hand lead to the danger that leakage currents on the circuit board can cause a shift of the input DC-voltage and the oscillator will never start.

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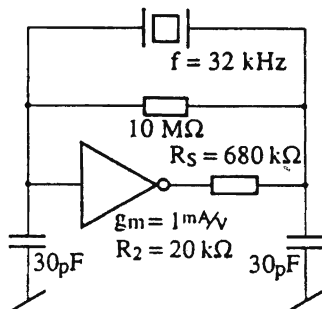


Fig. 9 A resistor in series with the output of the inverter is often necessary for low frequency oscillator to achieve safe operating conditions.

5. CONCLUSIONS

The start-up conditions for resonator oscillators are explained graphically in the impedance plane. This representation directly shows that oscillation is only possible if the transconductance of the amplifier exceeds a minimum value, but that there is also a maximum allowable transconductance. Approximation formulae which include all resistive components are derived so that the allowed transconductance range can be easily calculated. Looking at the results of typical oscillator circuits, it may be seen that for frequencies above 1 MHz, start-up problems are usually caused by an amplifier transconductance which is too low. The start-up problems for oscillators below 100 kHz are mostly caused by a transconductance which is too high, and by the feedback resistor, which significantly reduces the allowed transconductance range.

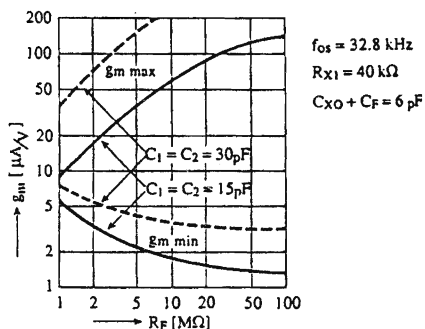


Fig. 10 Allowed transconductance range for a 32 kHz oscillator as a function of the feedback resistor.

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APPENDICES

Resonator Impedance

To get the locus of the impedance $Z_3(\omega)$ we start with the series branch $(R_{x1} + j\omega L_x + j\omega C_{x1})$ of the resonator. In the Z-plane this is a straight line (Fig. 11A) with ω as parameter. This line is transformed into the admittance plane ($Y = 1/Z$, Fig. 11B), where it becomes a circle with $1/R_{x1}$ as diameter (Moebius transform). In the Y-plane, the admittance of the parallel branches R_i and $(C_{x0} + C_i)$ can be added directly. This gives a small shift of the admittance circle (Fig. 11C) by the value $1/R_i + j\omega(C_{x0} + C_i)$. The locus $Y_3(\omega)$ is transformed back to the impedance plane ($Z_3 = 1/Y_3$). This results in a circle again, but mirrored at the real axis. The points on the real axis are called the "resonance point" and "anti-resonance point". Since α is very small (usually less than 5 degrees), the diameter $2r_z$ of the circle in the Z-plane is approximately equal to the resistance at the anti-resonance point.

$$2r_z \approx \frac{1}{G_C + G_F} = \frac{1}{G_C + 1/R_F} \quad (15)$$

G_C is derived from Fig. 11C:

$$G_C = \frac{1}{2R_{x1}} - \sqrt{\left(\frac{1}{2R_{x1}}\right)^2 - \omega^2(C_{x0} + C_F)^2} \approx R_{x1} \omega^2(C_{x0} + C_F)^2$$

Inserted into (15) we obtain for the diameter of the circle

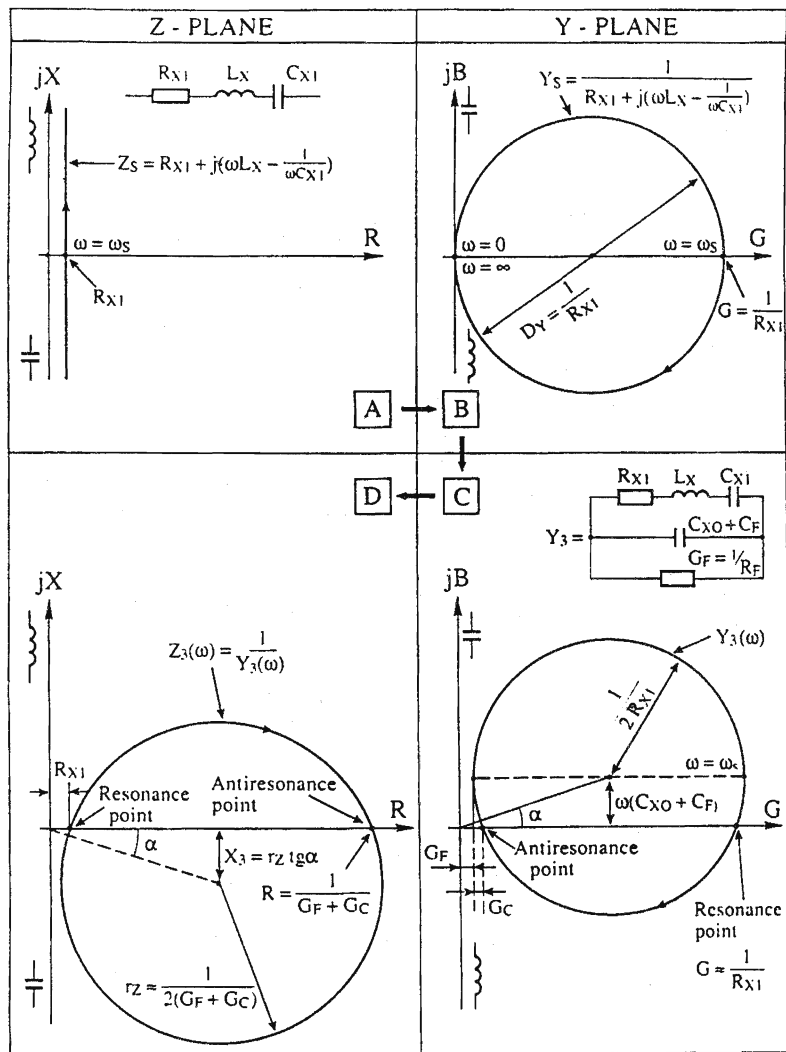
$$2r_z = \frac{1}{R_{x1} \omega^2(C_{x0} + C_F)^2 + 1/R_F} \quad (16)$$

The distance of the centre from the real axis is:

$$X_3 = r_z \tan \alpha = 2r_z R_{x1} \omega (C_{x0} + C_i) \quad (17)$$

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Fig. 11 A Impedance locus of the series branch of the resonator (with ω as variable)

B transformed into the admittance plane

C parallel branches ($C_{X0} + C_F$) and R_F added

D Transformed back into the impedance plane

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Minimum Transconductance

The calculation of $g_{m \min}$ is done with the diagram of Fig.7 which is partially redrawn in Fig.12. To get the right proportions, one has to keep in mind, that the difference between the parameters is much larger than shown here. Typical values for a 10 MHz oscillator are:

$$\begin{aligned} R_{X1} &= 20 \, \Omega \\ Z_1 &= Z_2 = 1 \, \text{k}\Omega \\ X_3 &= 2 \, \text{k}\Omega \\ r_z &= 100 \, \text{k}\Omega \end{aligned}$$

In the region of interest, the impedance curve $Z_3(\omega)$ is therefore almost parallel to the imaginary axis.

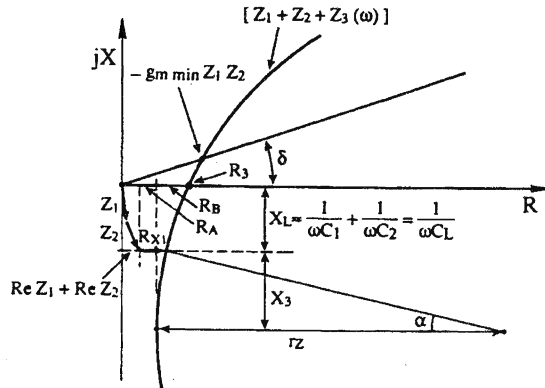


Fig. 12 Impedance plane of Fig.7 with expanded details around the origin

For small angles δ , we have

$$g_{m \min} |Z_1 // Z_2| \approx R_3$$

inserting equations (6) and (8), we get:

$$g_{m \min} = R_3 \omega^2 C_1 C_2 \quad (18)$$

This simplification is no longer valid, if δ exceeds about 30° , as $g_{m \min}$ will then increase. The value R_3 consists of 4 parts:

$$R_3 = \text{Re} Z_1 + \text{Re} Z_2 + R_a + R_b \quad (19)$$

$\text{Re} Z_1$ and $\text{Re} Z_2$ are given in eqs (7,9). The values for R_a and R_b are:

$$R_A = R_{X1} - \left(\sqrt{r_z^2 + X_3^2} - r_z \right)$$

$$R_B = \sqrt{r_z^2 + (X_3 + X_L)^2} - r_z$$

Taking only the first term of the series expansion of the square roots, we get:

$$R_A + R_B = R_{X1} + \frac{(X_3 + X_L)^2 - X_3^2}{2r_z} = R_{X1} + \frac{X_L(2X_3 + X_L)}{2r_z}$$

Inserting equations (16) and (17) into eq.(20) and rearranging gives a rather simple expression:

$$R_A + R_B = R_{X1} \left[1 + \omega(C_{X0} + C_F)X_L \right]^2 + \frac{X_L^2}{R_F}$$

Together with (see Fig.12)

$$X_L = \frac{1}{\omega C_1} + \frac{1}{\omega C_2} \approx \frac{1}{\omega C_L}$$

Equation (19) becomes:

$$R_3 = \frac{1}{R_1(\omega C_1)^2} + \frac{1}{R_2(\omega C_2)^2} + R_{X1} \left(1 + \frac{C_{X0} + C_F}{C_L} \right)^2 + \frac{1}{(\omega C_L)^2 R_F}$$

Inserted into eq. (18) we eventually get:

$$g_{m \min} = \left(2 + \frac{C_1}{C_2} + \frac{C_2}{C_1} \right) \left[R_{X1} \omega^2 (C_{X0} + C_F + C_L)^2 + \frac{1}{R_F} \right] + \frac{C_2}{R_1 C_1} + \frac{C_1}{R_2 C_2}$$

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FREQUENCY PULLING OF QUARTZ RESONATORS

1. Introduction

Quartz resonators, "Crystals", are used as stable frequency determining elements in oscillator applications. The quartz resonator frequency, as made by the manufacturer, will show some deviation from the target value due to the production process tolerances. A tight frequency tolerance requires a more expensive production process and often also yield loss, resulting in a higher price. The oscillator circuit also modifies the operating frequency of the quartz resonator. The most practical solution is an oscillator circuit design in which the frequency can be adjusted by a variable element, in general a trimmer capacitor. The natural series resonance of the quartz resonator is pulled to the target frequency by modifying the oscillation conditions with the trimmer capacitor. This note explains the limitations of frequency pulling of quartz resonators and some elements of the oscillator circuit design with respect to pulling.

2. Pager quartz resonator requirements

Pager systems require accurate frequency adjustment of the paging receiver because of the narrow frequency bands (channels) in which they operate. Pager system characteristics require maximum deviation from the channel centre frequency of about 15 ppm for 150 MHz, down to 2.5 ppm for centre frequencies in the 930 MHz band. This level of accuracy can only be obtained with high performance quartz resonators and dedicated oscillator circuits.

But even then the pager receiver manufacturer needs to adjust the oscillator at the exact centre frequency to guarantee that the frequency stays within the maximum limits due to temperature and aging effects. Unfortunately a large pulling range, although desirable from manufacturing point of view, conflicts with the quartz resonator characteristics and high stability requirements for pagers, so a compromise is required.

2.1 The Quartz resonator

A quartz resonator utilizes the piezoelectric properties of quartz in a mechanical vibration mode. AT-cut quartz plates are used in the thickness shear-mode, when high frequency resonance with good temperature characteristics and stability is needed.

AT-cut is referring to the orientation of the thin plates with respect to the axes of the mono-crystalline material.

The thin plates are cut from a quartz bar in a parallel sawing process. Determining and maintaining the AT-cut with a very tight cutting-angle tolerance during the production process is a challenge for quartz crystal manufacturers. For this type of crystals, one arc minute tolerance variation represents about three parts-per-million shift in the temperature compensation factor.

AT-cut plates are optimum regarding the temperature coefficient of the resonator with respect to piezoelectric activity, elasticity and mass.

When thin metal electrodes are deposited on the quartz plate, the resonator can be represented by an electric LCR series-circuit with a parallel capacitance (C_0). The series resonance frequency is determined by the thickness, for AT-cut plates:

$$F_s \text{ (MHz)} = 1.661/\text{thickness (mm)}$$

In the past, the electrical characteristics of the quartz resonator were empirically determined and the "activity" (R_1) was a matter of fortune. Today, the theoretical calculation of the so called motional parameters C_1 , L_1 , and R_1 of the resonator is also possible.

The complex calculation is based on the physical characteristics of quartz, involving: elasticity, mass, piezoelectric coupling, trapping, dielectric constant, dimensions and thickness of the quartz and electrode material.

The capacitance C_0 caused by the metal electrode, with area "A", opposite to each other at distance "d", is:

$$C_0 = \epsilon_0 * \epsilon_r * A/d$$

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The substitution diagram of the crystal parameters follow from figure 1.

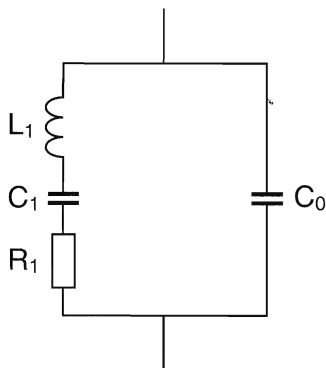


Fig. 1 Substitution diagram of a quartz crystal

By convention between quartz crystal manufacturers, the equivalent electrical, motional circuit parameters are always stated as L_1 , C_1 , R_1 ; this also holds for overtone units.

The equivalent electric circuit shows two resonance frequencies,

- F_s the lower series-resonance frequency determined by L_1 , C_1 , R_1 ,
- and F_p determined by the parallel circuit of L_1 , C_1 , R_1 with C_0 .

2.2 The coupling factor

The ratio between F_p and F_r is given by the equation:

$$F_p / F_r = \sqrt{(C_0 + C_1) / C_0}$$

The ratio C_0/C_1 is in principle a fixed quantity:

$$C_0/C_1 = r = \pi^2 * \{(1 - k^2) / k^2\} / 8$$

where k is the electromechanical coupling factor.

For AT-cut quartz crystals, $k = 0.088$, resulting in a ratio:

$$C_0/C_1 = r = 159$$

For flat quartz plates this "ideal" ratio cannot be obtained in a practical resonator due to trapping of contaminating atoms and non ideal plane-parallel surface the k factor is much lower. Practical values of r are in the range 190 - 500 for the quartz plate; the holder capacitance, most often a metal can, increases this ratio to even higher values.

2.3 Overtone crystals

All mentioned results are for fundamental mode resonators. The highest frequency which can be obtained for fundamental crystals by using a standard production process is about 35 MHz.

For higher frequencies, as needed in most pagers, quartz plates are vibrating in odd overtone modes (3, 5, 7,...). On analyzing the motional parameters of quartz plates vibrating in overtones, one finds the equivalent capacity in the series branch to decrease with the inverted square of the overtone mode;

$$C_3 = C_1/9, C_5 = C_1/25, C_7 = C_1/49$$

In most cases we are interested in the relative frequency difference between series and parallel frequency. For quartz resonators with high Q factor and high C_0/C_1 ratio we can use the simple formula:

$$(F_p - F_s) / F_s = C_1 / (\tilde{2} * C_0)$$

As an example, assuming C_0/C_1 is 210, we find:

Fundamental mode	$1/2 * 210$	= 2400 ppm
Third Harmonic mode	$1/2 * 210 * 9$	= 265 ppm
Fifth Harmonic mode	$1/2 * 210 * 25$	= 95 ppm

For small practical shielded fundamental and overtone quartz resonators a typical C_0 value is 6 pF, including the shield capacitance.

With the motional capacitance C_1 of fundamental quartz units to be 10 - 50 fF for a frequency range of 10 - 30 MHz, the third overtone units show a typical C_3 value of 1.5 fF for the 30 - 100 MHz range, and the fifth overtone C_5 is typical 0.5 fF for 70 - 150 MHz.

Questions and application hints

Crystal and PXE oscillator considerations

Where the motional series resistance R_1 practically is about 10 ohms, the overtone units show higher values due to the frequency dependent losses of the quartz resonator. These losses generally also increase with decreasing resonator size.

For more information on quartz crystal resonators, one should always consult the manufacturer; the parameters for any specific unit may vary by more than an order of magnitude.

The chapter Pager Receivers, UAA2080 VHF/UHF Paging receiver; 2. Design of crystal oscillator, is dealing with further particulars of oscillator design and calculation examples.

3. The complete oscillator.

3.1 Load resistance

From a practical point of view, a small tunable capacitor C_{load} in series with the quartz unit, is most easy to implement.

When the series-capacitance is tuned to a very small value, the oscillator will probably not start, or jump to a non desired mode of operation.

This can be explained because the loss resistance of the crystal is transformed according to;

$$R_{load} = R_0 * (1 + C_0/C_{load})^2$$

This means when $C_{load} = C_0$, the result is $R_{load} = 4 R_1$; when $C_{load} = 1/10 C_0$, this results in $R_{load} = 121 R_1$; a practical oscillator will not operate properly at such high resistance values.

3.2 The tuning range (pull-ability)

Using the same approximation as above we can now express "pull-ability" to be the relative frequency difference;

$$(F_p - F_s)/F_s = C_1 / \{2 * (C_0 + C_{load})\}$$

In practical oscillator circuits, C_{load} values should not be smaller than C_0 .

In an example circuit, using a third overtone crystal, we find C_0 is 6 pF and C_1 is 1.5 fF. When using the load capacity C_{load} (6 - 30 pF) for tuning the oscillator, we calculate the highest frequency to be 62 ppm above series-resonance and the lowest frequency to be 21 ppm. This example circuit now shows a total pulling range of 62 - 21 ppm with respect to the series resistance, or about +/- 20 ppm around a centre frequency.

For the example circuit, the crystal unit will be ordered at a calibration frequency of 42 ppm above series resonance (mean value) at C_{load} is 12 pF.

Quartz crystal unit manufacturers prefer standardized C_{load} values with values of 8, 12, 15, 20, 30, and 50 pF. Standardised load capacitors decrease the measurement uncertainty at the manufacturers calibration service.

CHAPTER 8

NEW DEVELOPMENTS

New developments

page

VIII-1

New Developments

NEW DEVELOPMENTS

In this chapter, some of the more recent developments on Pager ICs will be looked at. Although these developments have not yet resulted in new application reports, the information in this chapter may still be valuable for the designer.

1. UAA2082

The well-known UAA2080 has been around for some time now, resulting in a host of application information (see chapter: Pager Receivers) and responses from the market and OEM Pager designers (see chapter: Questions and Application Hints). Based on the above information and requests, it was decided to design a derivative of the UAA2080, incorporating features, that make this design even more "application friendly".

1.1 Battery-low detection

In the UAA2080, the battery-low detection threshold is specified at a fixed voltage of 2.05 V (+/- 0.1 V over temperature).

In the UAA2082, the battery monitoring circuit has an external sense input and a 1.1 V (+/- 0.07 V over temperature) detection threshold for easy operation in a single-cell supply concept.

When the voltage on the SENSE input drops below the threshold voltage, the output of this monitoring circuit is available as a logical HIGH, at the BLI-output. This operation is equivalent to the UAA2080 situation. The designer now has freedom over the low voltage alarm situation in various Pager powering schemes, as the SENSE input may be divided down from any convenient voltage level. Also the tighter voltage tolerance over temperature on the detection threshold of the UAA2082 makes this new feature a useful addition.

1.2 Power saving

The oscillator circuit is revised, allowing for power saving possibilities under various conditions. In the UAA2080, the oscillator circuit is internally biased, leaving the designer the freedom of selecting the transconductance of the active element to suit his choice

of oscillator crystal by means of the external emitter resistor R5, that is in parallel to an internal resistor of 1.8 k Ω (see diagrams at chapter: Pager Receivers). In the UAA2082, the oscillator is to be biased externally at the crystal oscillator input terminal while the internal emitter resistor of 1.8 k Ω has been omitted. The optimal external biasing is using a reference voltage of 1.22 V (+/- 20 mV) and a series resistor of 22 k Ω . The emitter resistor now becomes 1.5 k Ω .

The external bias scheme allows for various new design options.

1.2.1 External oscillator.

When using an external oscillator circuit design, the internal oscillator circuit may be switched-off completely by connecting the two oscillator terminals to ground. This option will save about 65 micro amp. as compared to the same situation, using UAA2080.

In the external oscillator case, the new situation offers the designer a larger freedom in selecting the bias current, when using the receiver's oscillator stage as an input buffer for the oscillator frequency.

1.2.2 Internal oscillator.

As is well known to any circuit designer; a design, operating with a high-Q tuned circuit will need some time to establish the desired operating condition. This time is longer at very-high-Q designs, e.g. when using quartz crystals.

In pager applications, power saving is very important. For this reason, the pager receiver is switched on only, when the system is expecting information and switched off for the rest of the time. When the receiver is switched on, it will take some time before the receiver has reached a stable operating condition, mainly due to the oscillator "establishment time". During this period, all of the receiver circuits are active, draining power from the supply.

In the new situation, using the UAA2082, it is possible to switch on the oscillator circuit through the external bias path, while leaving the rest of the receiver circuit switched off. At the end of the oscillator establishment time, the rest of the receiver is switched-on for normal

New Developments

operation, using the receiver enable input, which controls the internal band-gap reference.

This two-step switch on scheme may be accomplished with a simple receiver enable delay scheme using PCF5001, or with the two dedicated switch lines using PCD5003 (see also the comparison table PCF5001/PCD5003 and the appropriate data sheets).

As the established oscillator consumes approximately 10% of the total receiver current, power savings are very feasible using such a switching scheme.

1.3 Packaging

At this moment, the UAA2082 is available as UAA2082H, in TQFP32 package, this is the thin, plastic, quad flat package with 32 leads, version SOT358-2, UAA2082U, as naked die, 28 pads.

1.4 Electrical and mechanical specifications

All other electrical and mechanical specifications of the UAA2082 are identical to the UAA2080. This means, that all the information as mentioned in chapters: Pager receivers, Development tools and materials and Questions and application hints also hold for this new receiver.

For more information on UAA2082, please refer to the latest data sheet.

2. PCD5003

In our series of decoders for the POCSAG Paging standard, the new PCD5003 is a major step forward. When compared to the popular PFC5001, many new features and utilities have been included, power has been lowered and the versatility enhanced. The following description from the preliminary data sheet gives an impression of this powerful device.

2.1 General description

The PCD5003 is a very low power Decoder and Pager Controller specifically designed for use in new generation radiopagers. The architecture of the PCD5003 allows for flexible application in a wide variety of radio pager designs.

The PCD5003 is fully compatible with CCIR Radiopaging Code No.1 (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

In addition to the standard POCSAG synch word the PCD5003 is also capable of recognizing up to 4 user-programmable Sync Words (UPSW's). This permits the reception of both private services and POCSAG transmissions via the same radio channel.

Used together with the Philips UAA2080 Paging Receiver, the PCD5003 offers a highly sophisticated, miniature solution for the radiopaging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs), which eliminate the need for external storage devices and interconnections. The low EEPROM programming voltage makes the PCD5003 well-suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5003 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

Via external bipolar transistors the PCD5003 can also produce a high-level acoustic alert as well as drive an L.E.D. indicator and a vibrator motor.

The PCD5003 contains a low power, high efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5003.

Interface to such an external device is provided by an I²C-bus. This bus allows transferring of received call identity, message data, data for the programming of the internal EEPROM, alert control and pager status information between the decoder and other pager components. Pager status includes features provided by the PCD5003 such as Battery Low and Out-of-Range indications.

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A selectable low frequency timing reference is provided for use in Real Time Clock functions.

Data Synchronization is achieved by the Philips patented ACCESS algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption.

Random and (optional) Burst Error correction techniques are applied to the received data to optimize on call success rate without deteriorating falsing rate beyond specified POCSAG levels.

When the PCD5003 is used in combination with a microcontroller, communication takes place via an I²C-bus interface. A dedicated interrupt line minimizes the required microcontroller activity.

2.2 Comparison table

When compared to the popular PCF5001 POCSAG decoder, it will become clear, that the PCD5003 may be regarded as a high-end device.

Feature	PCF5001	PCD5003
Voltage range	1.5 V - 6.0 V	1.5 V - 6.0 V
Supply current	60 µA typ.	50 µA on, 25 µA off
Temp. range	-40 °C to +85 °C (restricted supply range -40 °C to -10 °C)	-25 °C to +70 °C
Radio paging code	POCSAG	POCSAG
Baudrates	512, 1200 bit/s using 76.8 kHz crystal, 2400 bit/s using a 153.6 kHz. crystal	512, 1200, 2400 bit/s using 76.8 kHz crystal
Data filter	built-in	built-in
ACCESS algorithm	built-in	built-in
Alert -support	beeper, vibrator, LED	beeper, vibrator, LED
-control	auto (POCSAG), alarm input	auto (POCSAG), cadence register, alarm input
-cadence	fixed - 4 patterns	fixed - 4 patterns, progr. via 8 bit reg.
-acoustic	2-level	2-level
-repeat mode	optional	no
Call-termination condition	programmable	fixed, or externally programmable from call termination register
-duplicate suppression	optional	no
Error correction	4 bit burst (address) 1 bit random (message)	2 bit random plus 4 bit burst (optional) (address and message)

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Feature	PCF5001	PCD5003
User-addr. (RIC)	4	6
-frames	2	6
-sync. word	fixed (POCSAG)	fixed (POCSAG) plus programmable (max. 4)
μC wake-up INT	no	yes (prog. polarity)
Real time clock reference	32768 or 16384 Hz	32768 or 50 Hz 2 or 1/60 Hz
Data inversion	no	yes (optional)
Pager system cntl	dedicated lines	dedicated lines, I ² C (including PCD5003 wake-up)
Receiver -control	one level	two level (separate rec. oscil/rec. pwr; see UAA2082)
-enable monitoring	no	yes
Synthesizer cntl	no	3-line serial interf.
Battery low input	yes	yes
Out-of-Range ind.	yes	yes
On-chip voltage doubler	yes	yes
EEPROM -width	3 * 38 bits	48 * 8 bits
-programming	5.0 Volt 2-prog. lines	2.5 Volt (over air!) I ² C (up to 400 kbit/s)
-content	user address (4-RIC), pager configuration	user address (6-RIC), pager configuration, synthesizer data
Message storage	1 (display pager) or 8 different silent calls (alert only)	96 bytes of call data in two batches
Packaging	(T), 28 pin minipack, plastic, SOT136A (H), 32 pin QFP, plastic SOT358AA1	(U/10), 32 pads naked die, film frame carr. (H), 32 pin QFP, plastic SOT358-1

For more information, please refer to the data sheets:

PCF5001, POCSAG Paging Decoder, June 1993 or Philips Semiconductor Data Handbook IC03, 1993

PCD5003, Advanced POCSAG Paging Decoder, November 1994

New Developments

3. PCD5002

The PCD5002 is a very low power decoder and pager controller specifically designed for use in new-generation radio pagers. It is fully compatible with the POCSAG standard, but also complies with the basic version of the new APOC standard (APOC-1), which offers much improved battery economy. The PCD5002 operates at speeds of 512, 1200 and 2400 baud using a single 76.8 kHz crystal and has advanced ACCESS synchronization.

Documentation and the APOC licence are available from Philips Telecom (Private Mobile Radio), Cambridge (UK).

4. OM4031T

The OM4031T is a digital post detection filter for FSK Data receivers. The basic filter circuit is an integral part of the Philips Pager Decoder ICs PCF5001, PCD5002 and PCD5003 and enhances the sensitivity of a pager-system, build around these decoders. It was decided to also have the filter available as a discrete circuit building block to the pager designer, allowing for greater flexibility and enhanced performance of his design. The following description was taken from the data sheet of OM4031.

4.1 General description

The OM4031T is intended for performance enhancement of FSK data receivers that do not have a built-in post-detection filter.

It contains a digital moving average filter to remove noise from the demodulated data. When operated from a 38.4 kHz external clock it can handle data rates of 600, 1200 and 2400 bits/s at an oversampling rate of 16. The filter bandwidth can be doubled to ease the search for bit synchronization on the output data.

To allow for jitter in the input data, a 12-bit sample is taken for the majority decision. Doubling the filter bandwidth is realized by taking the majority out of 6 samples (2400 bits/s) or by doubling the sampling rate (600 and 1200 bits/s).

An input data rate of 4800 bits/s is supported at 8 times oversampling and normal bandwidth.

All inputs are Schmitt-triggered to ensure reliable operation even at signals with long rise/fall times.

4.2 Functional description

The OM4031T Digital Post-Detection Filter oversamples the noisy binary data stream at the input, and outputs a noise-reduced data stream via an open drain output. The filter bandwidth can be doubled to ease the search for bit synchronization on the data output signal.

Although designed for a clock frequency of 38.4 kHz typical, the clock frequency is not very critical for the noise filtering performance: a clock frequency of 32.768 kHz could be used at 512, 1200 and 2400 bits/s without loss of performance.

Since no on-chip oscillator is available, an external clock signal is required at the clock input, with a frequency between 30 - 80 kHz. Two control inputs are used for selection of the data rate and the filter bandwidth.

The OM4031T filter output will produce bit rates equal to the clock frequency divided by 64, 32 or 16. When the clock frequency is not an integer multiple of the data rate some edge jitter will be introduced in the output data.

Noise reduction is realized by applying a moving average filter on N samples of the input data signal. In principle N can be odd or even, but in the OM4031T an even number is used (N=12). When there is no absolute majority (equal number of ones and zeroes) the previous majority output is maintained.

Using 12 out of 16 samples for the majority decision produces a filter which combines good noise reduction with a large tolerance for data jitter (max. 1/8 bit duration).

The moving average filter is implemented using a 13-bit shift register and two state machines for the majority decision. The first stage of the shift register is used for input synchronization.

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The first state machine generates the internal clock signal and the bandwidth selection signal, according to the logic levels on three control lines.

The majority decision is taken by the second state machine based upon the contents of the input shift register and the previous decision in the output latch. To obtain an impression of the performance of the filter, the OM4031T was tested in a POCSAG pager application using software decoding, together with the UAA2080H receiver. For 12-digit numeric messages at 1200 bits/s the typical sensitivity for 80% call success rate improved by 2.8 dB.

4.3 Applications

The OM4031T is specifically valuable in cases where maximum sensitivity of an FSK-based transmission system is required and/or optimum data integrity. These requirements may be found in a host of applications, e.g. telemetry data receivers, RF security systems, low bit rate wireless data links and, of course, Paging applications of UAA2080 and UAA2082 with software decoding.

4.4 Packaging

The OM4031T is available in an 8 pin, plastic SO8 package, SOT96A.

For more information on OM4031T, please refer to the data sheet

OM4031T Digital Post-Detection Filter for FSK Data Receivers, August 1994.

CHAPTER 9

PACKAGE OUTLINES

page

Package outlines

IX-1

Package outlines

- NOTES**
- 1. Controlling dimension: inches. Metric are shown in parentheses.
 - 2. Package dimensions conform to JEDEC Specification MS-001-AB for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 8 leads (Issue B, 7/85).
 - 3. Dimension and tolerancing per ANSI Y14, 5M - 1982.
 - 4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
 - 5. These dimensions measured with the leads constrained to be perpendicular to plane T.
 - 6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.

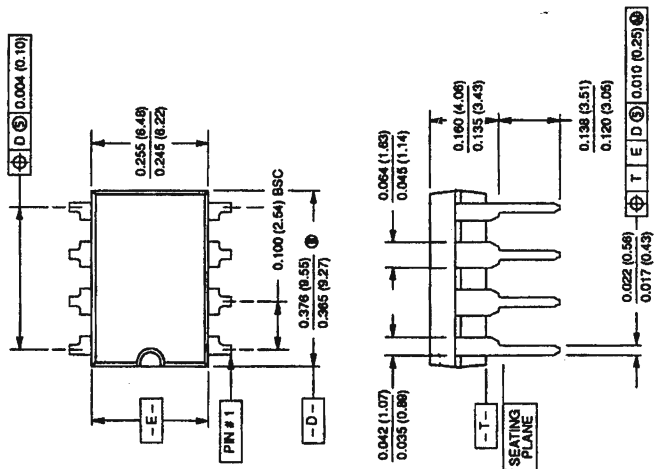
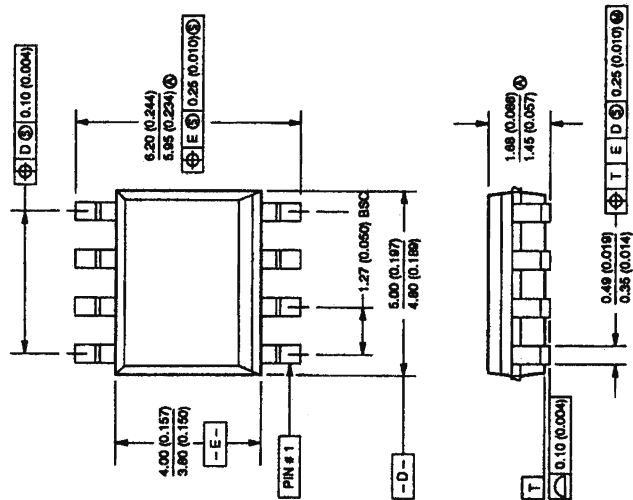


Fig.1 8-pin (300 mils wide) plastic dual in-line (N) package (DWG 0404B).

Package outlines



NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AA for standard Small Outline (SO) package, 8 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

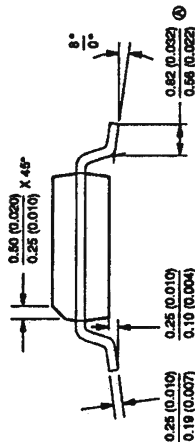


Fig.2 8-pin (157 mils wide) plastic SO (Small Outline) dual in-line (D) package (DWG 0174C).

Package outlines

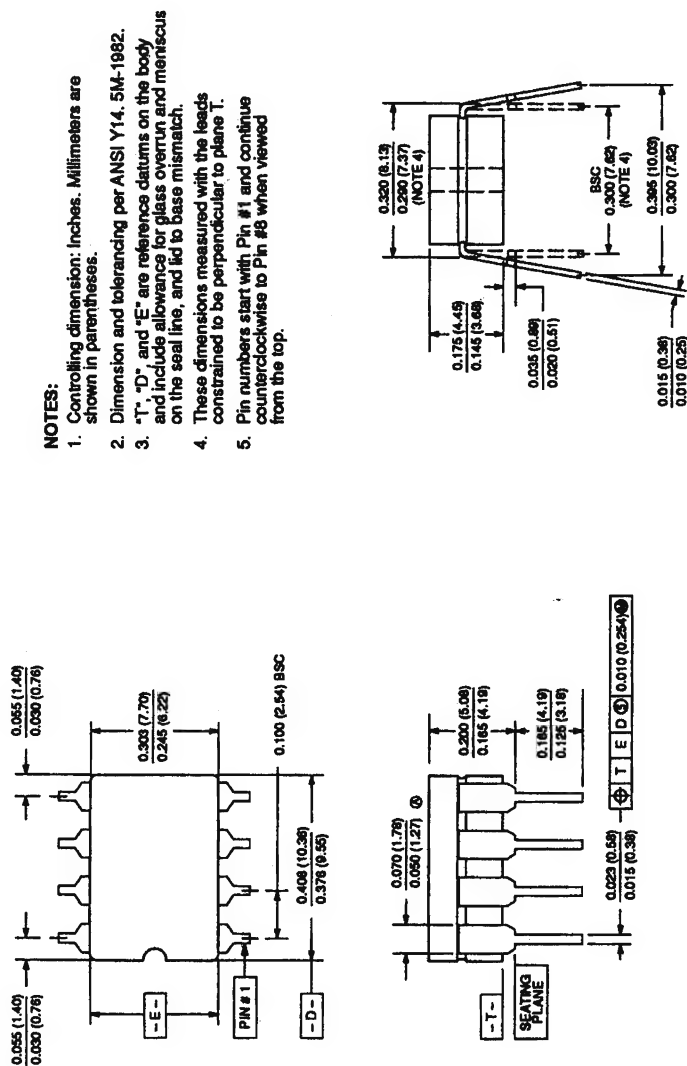


Fig.3 8-pin (300 mils wide) ceramic dual in-line (F) package (DWG 0580A).

Package outlines

NOTES

1. Controlling dimension: Inches. Metric in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AC for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 14 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M - 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.

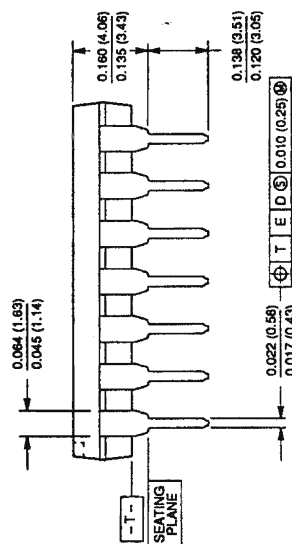
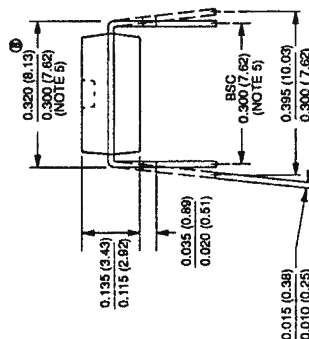
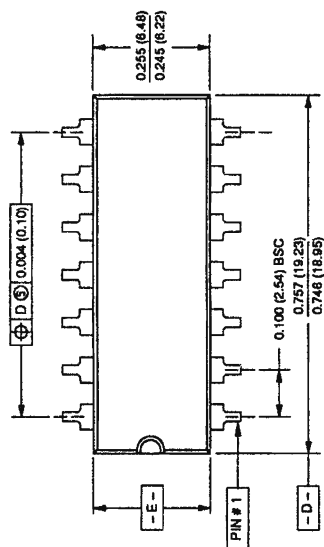
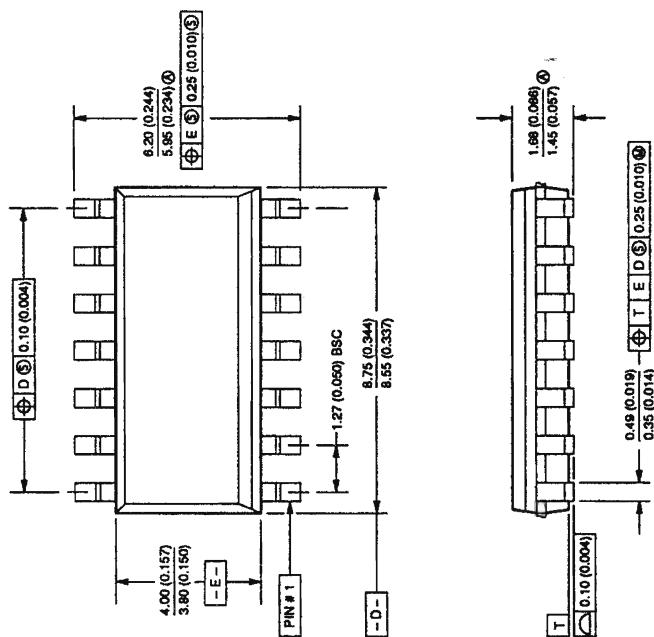


Fig.4 14-pin (300 mils wide) plastic dual in-line (N) package (DWG 0405B).

Package outlines



NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AB, for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

Fig.5 14-pin (157 mils wide) plastic SO (Small Outline) dual in-line (D) package (DWG 0175D).

Package outlines

NOTES:

1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimension and tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with Pin #1 and continue counterclockwise to Pin #14 when viewed from the top.

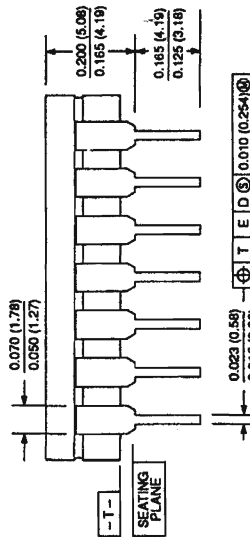
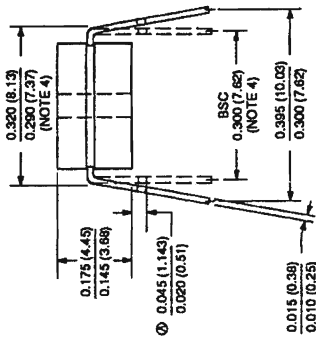
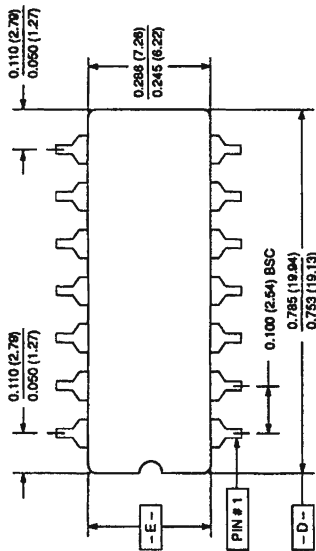


Fig.6 14-pin (300 mils wide) ceramic dual in-line (F) package (DWG 0581B).

853-0581B 06688

Package outlines

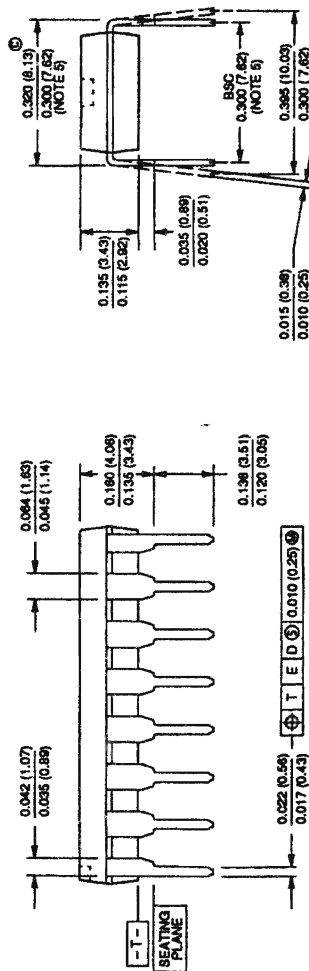
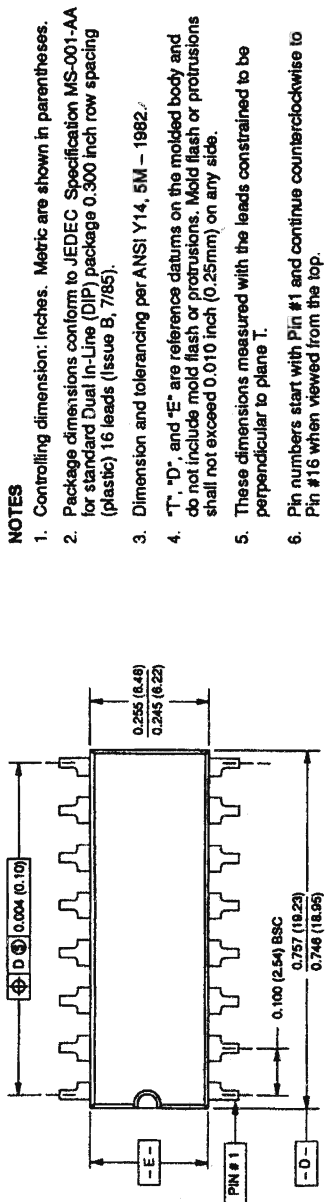
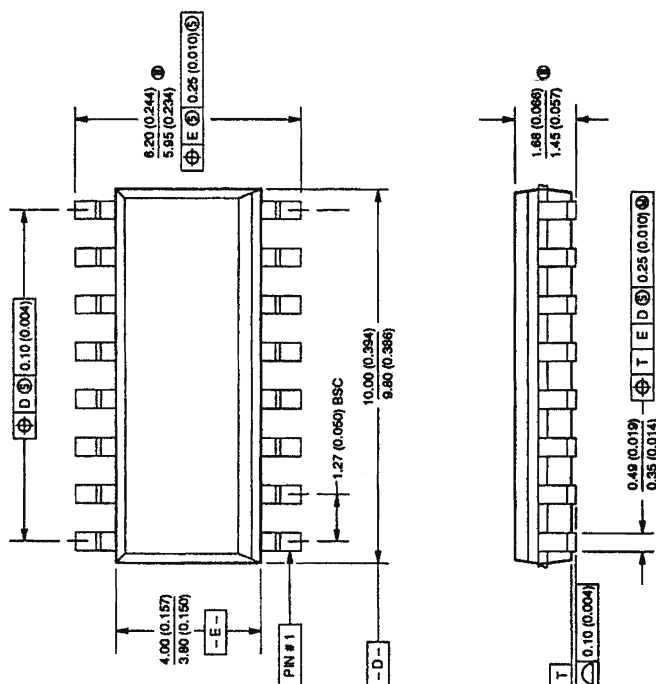


Fig.7 16-pin (300 mils wide) plastic dual in-line (N) package (DWG 0406C).

Package outlines



NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AC for standard Small Outline (SO) package, 14 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

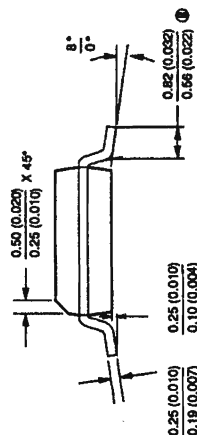
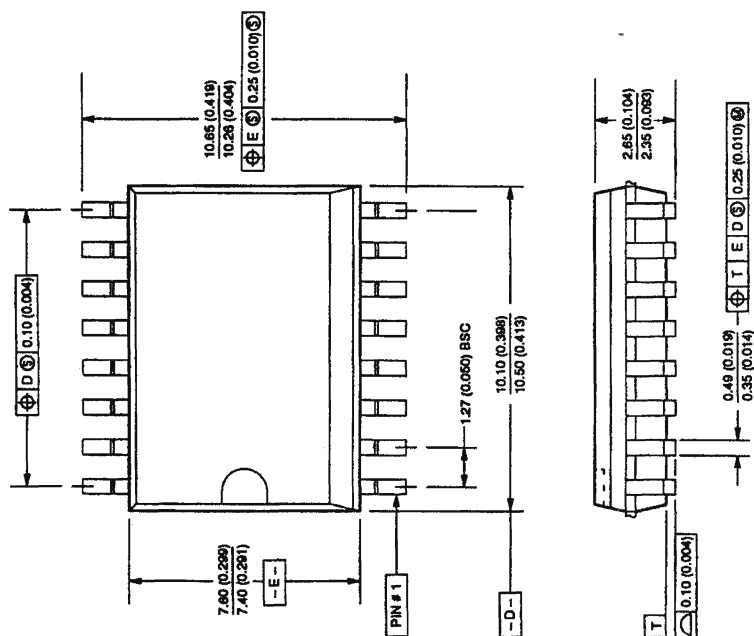


Fig.8 16-pin (157 mils wide) plastic SO (Small Outline) dual in-line package (DWG 0005D).

Package outlines

853-0171B 04697



NOTES

1. Package dimensions conform to JEDEC Specification MS-013-AA for standard Small Outline (SO) package, 16 leads, 7.50mm (0.300") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from top.
7. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.

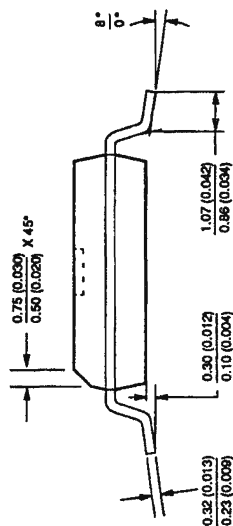


Fig.9 16-pin (300 mils wide) plastic SOL (Small Outline Large) dual in-line (D) package (DWG 0171B).

Package outlines

853-0582B 09888

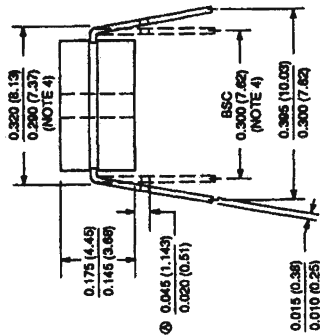
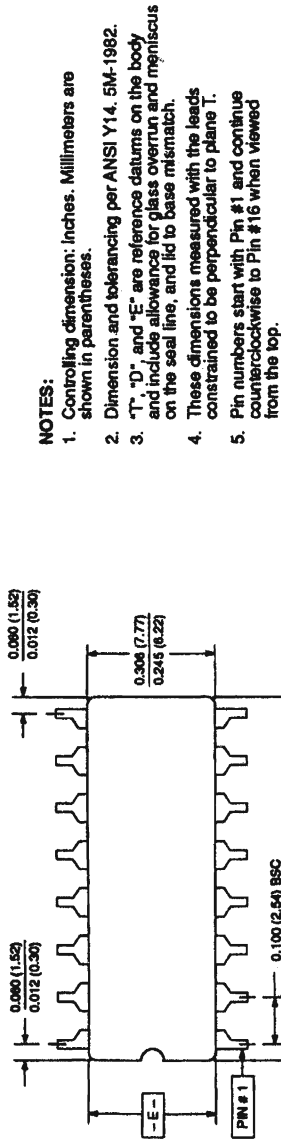


Fig.10 16-pin (300 mils wide) ceramic dual in-line (F) package (DWG 0582B).

Package outlines

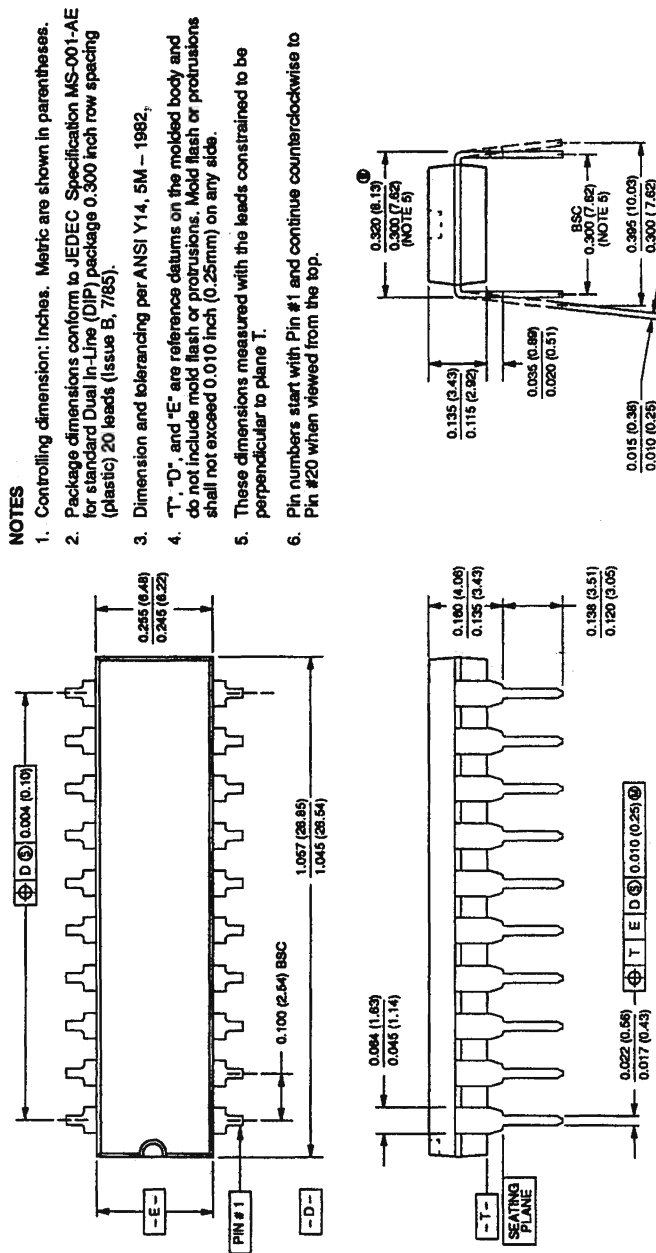


Fig.11 20-pin plastic dual in-line (N) package (DWG 0408B).

Package outlines

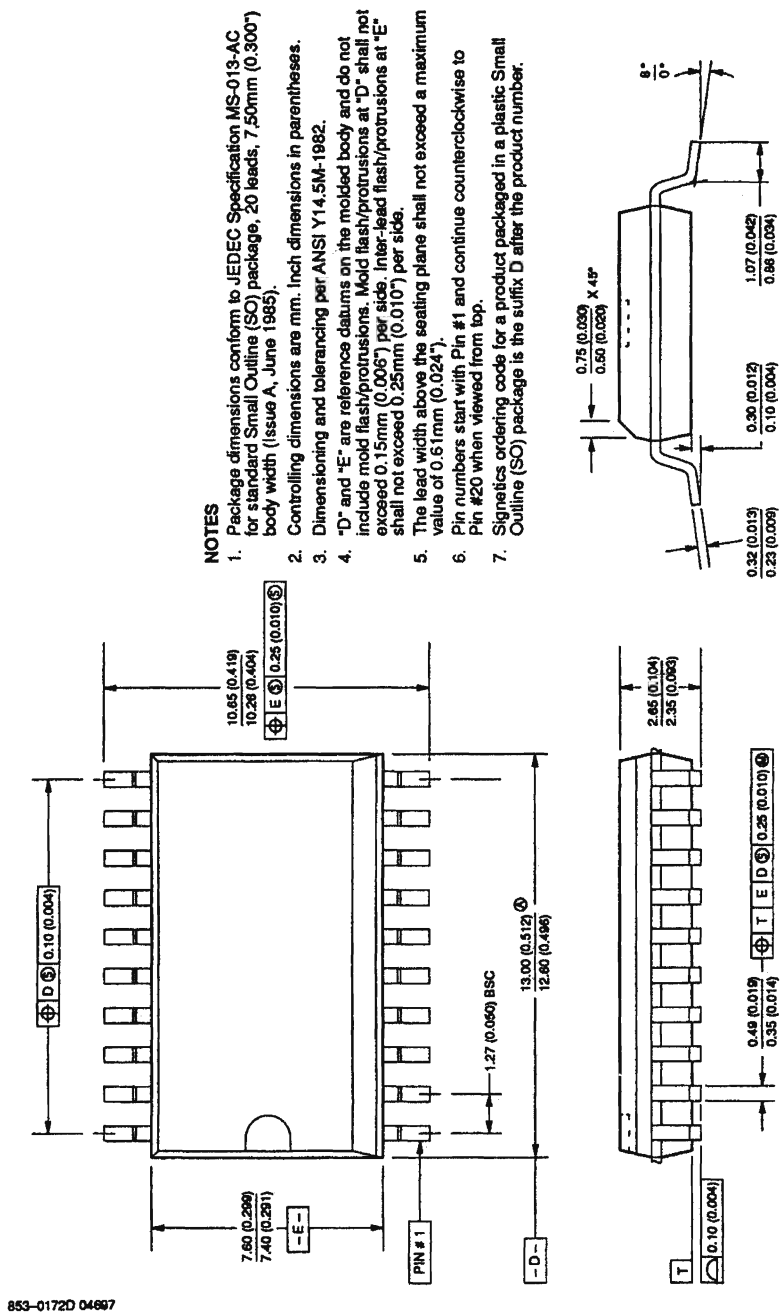
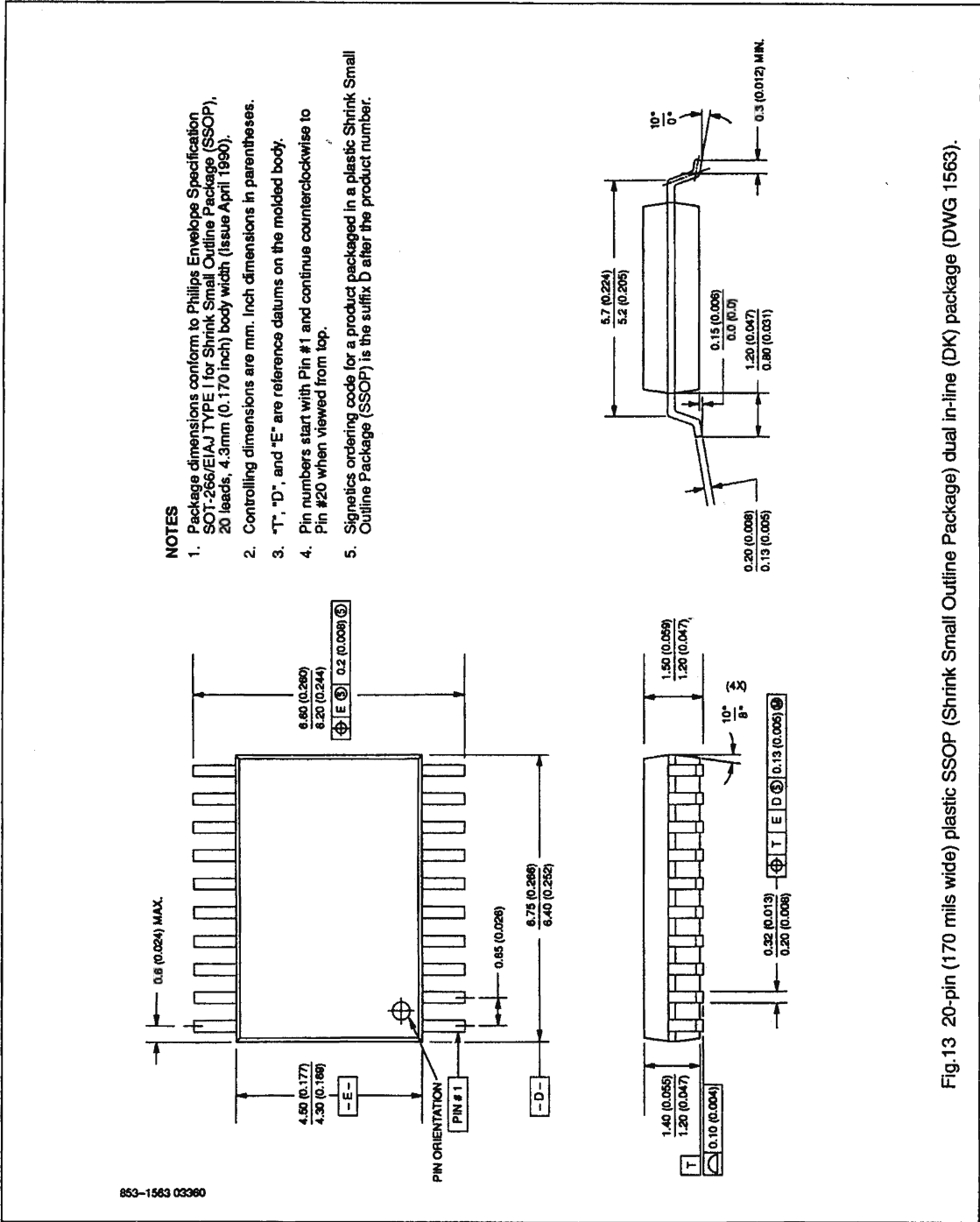


Fig. 12 20-pin (300 mils wide) plastic SOL (Small Outline Large) dual in-line (D) package (DWG 0172D).

Package outlines



Package outlines

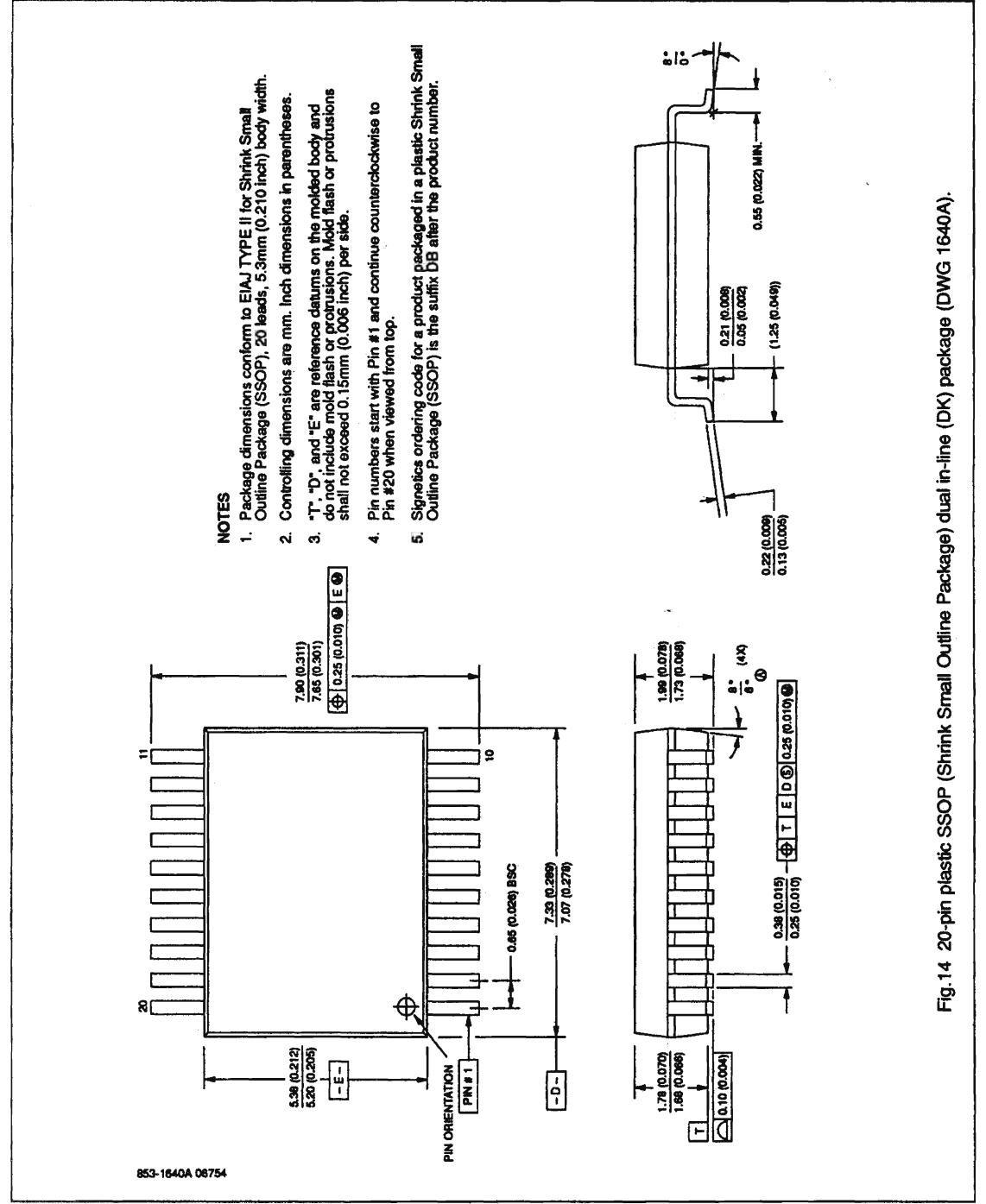


Fig.14 20-pin plastic SSOP (Shrink Small Outline Package) dual in-line (DK) package (DWG 1640A).

Package outlines

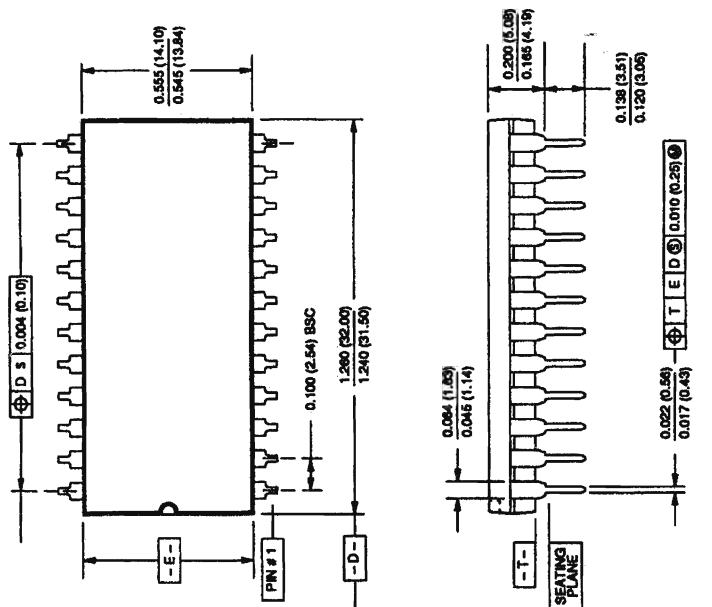


Fig. 15 24-pin (600 mils wide) plastic dual in-line (N) package (DWG 0412A).

NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AA for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 24 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14.5M - 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from the top.

Package outlines

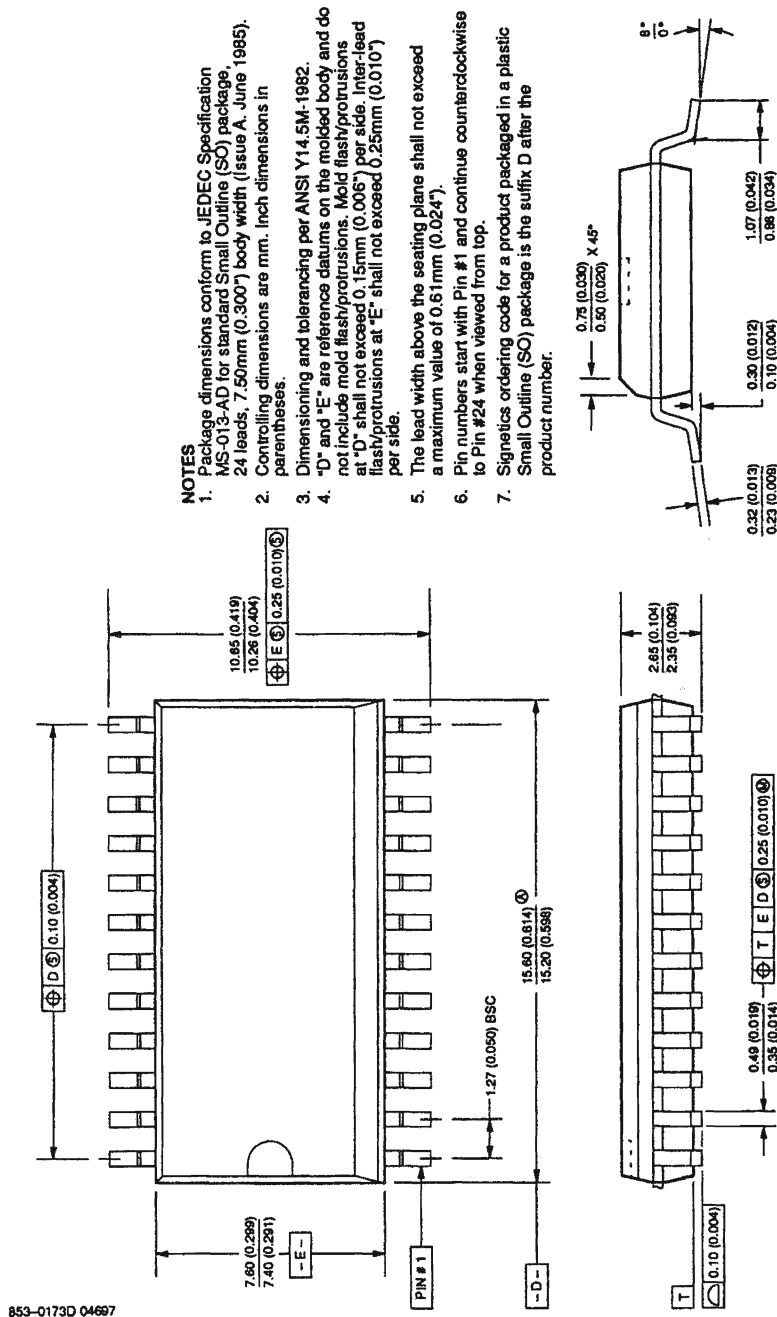


Fig. 16 24-pin (300 mils wide) plastic SOL (Small Outline Large) dual in-line (D) package (DWG 0173D).

Package outlines

853-0006C 04697

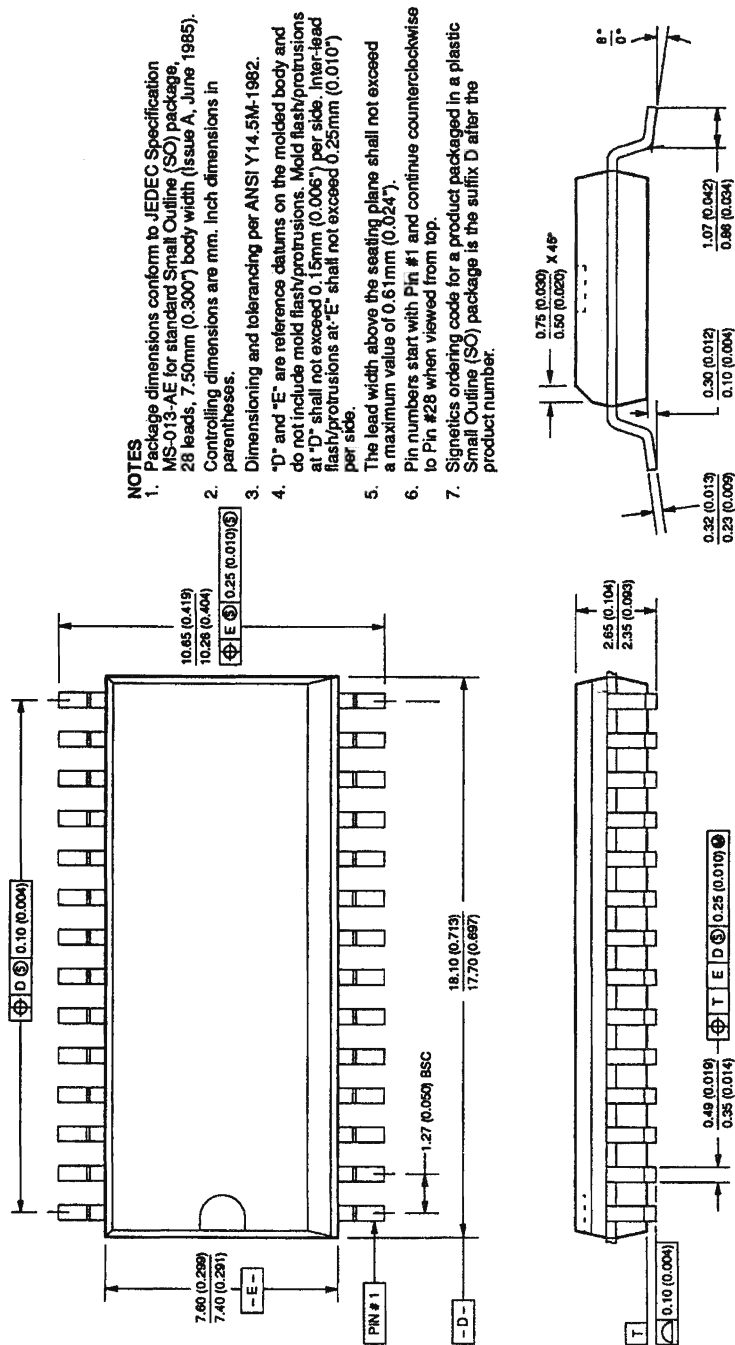
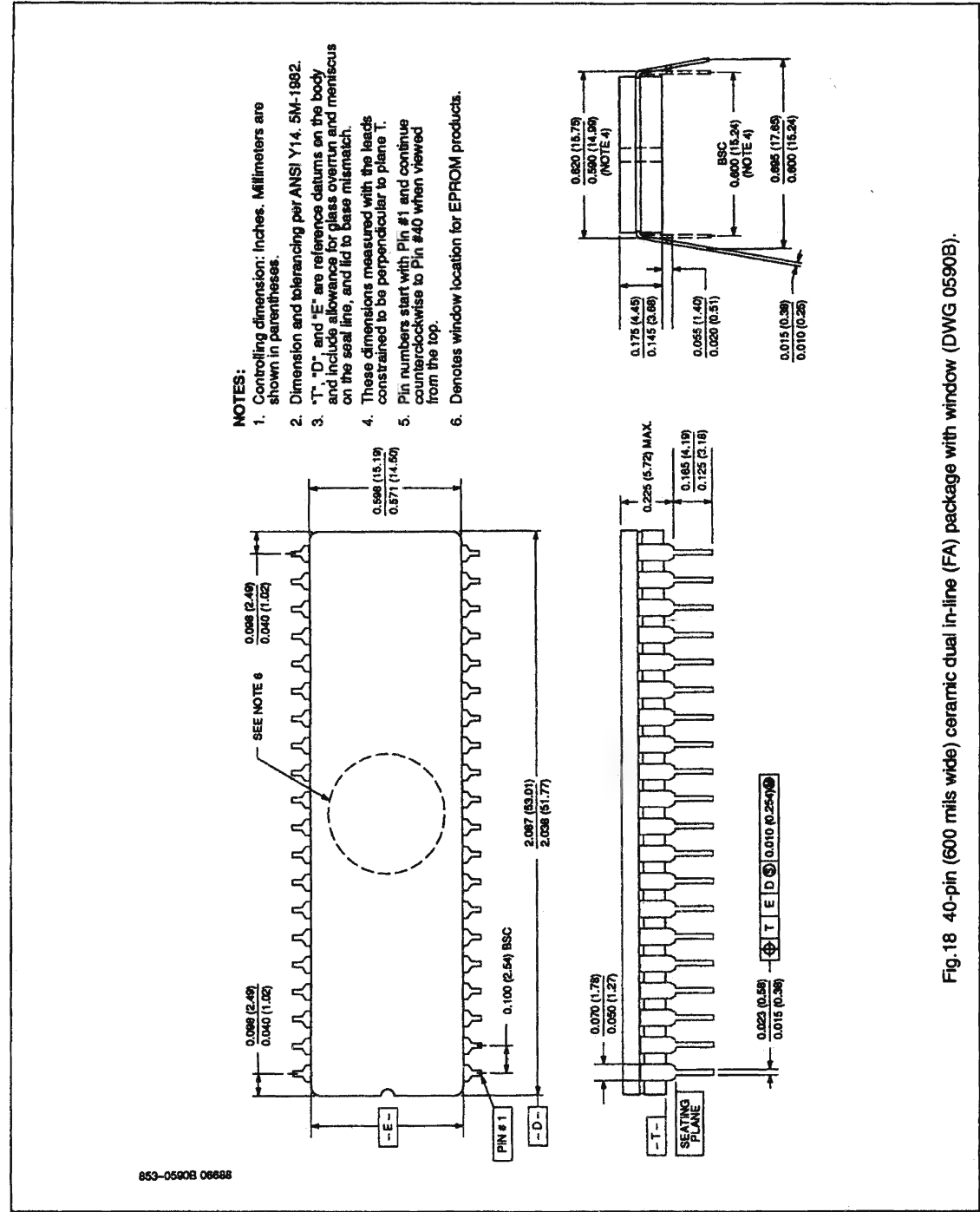


Fig. 17 28-pin (300 mills wide) plastic SOL (Small Outline Large) (D) package (DWG 0006C).

Package outlines



Package outlines

853-1472A 05854

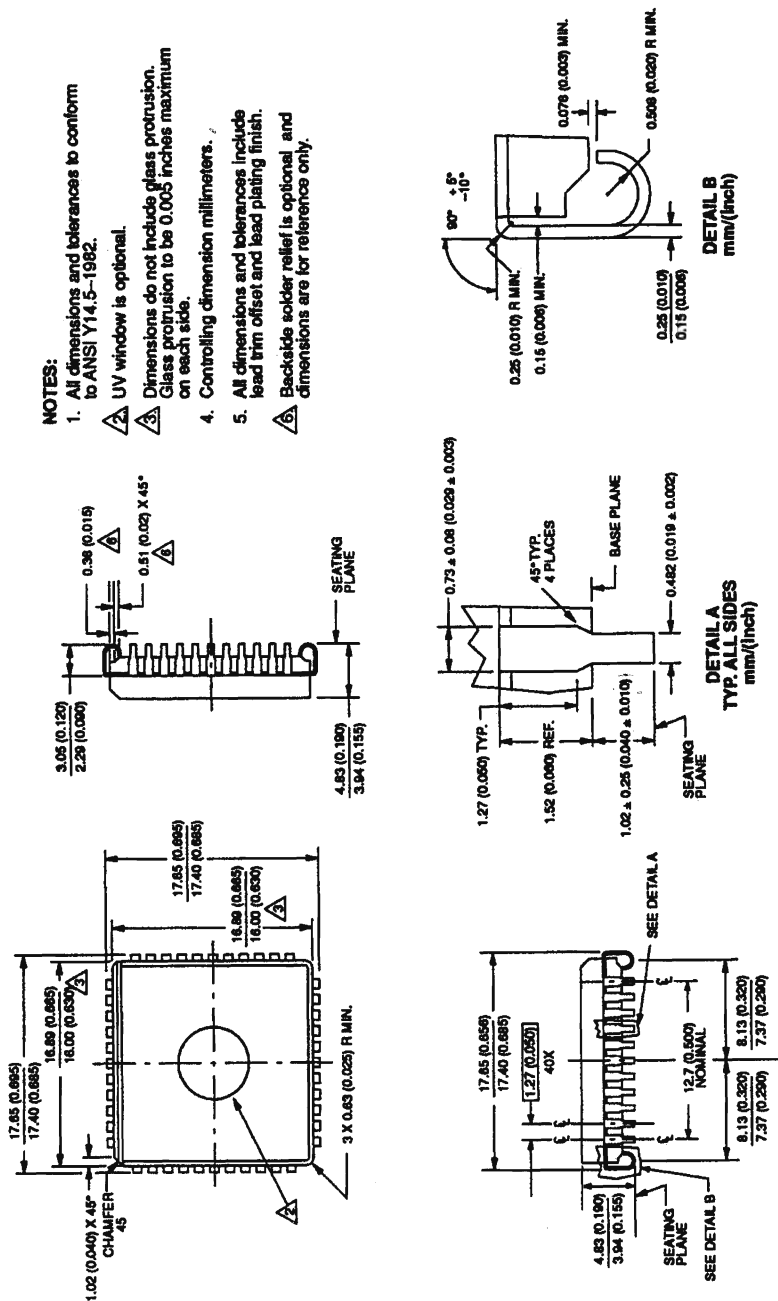
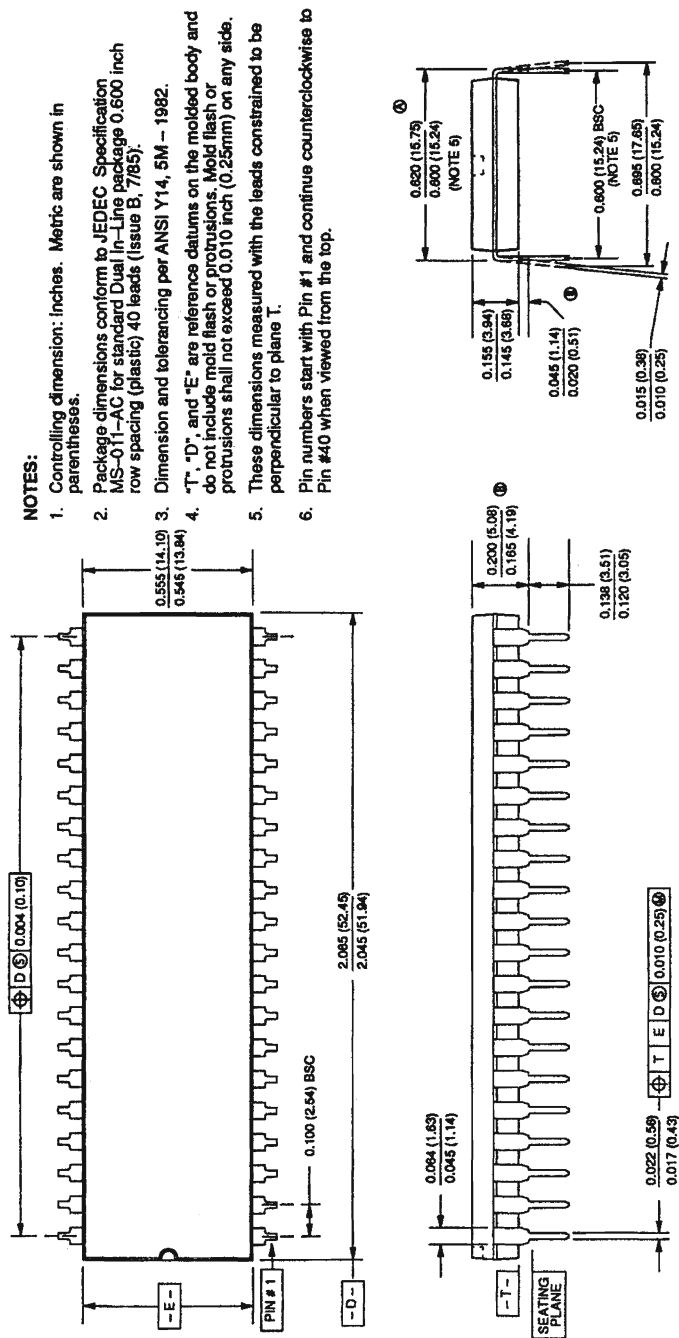


Fig.19 44-lead CERQUAD J-bend (K) package (DWG 1472A).

Package outlines



853-0415C 05390

Fig.20 40-pin (600 mils wide) plastic dual in-line (N) package (DWG 0415C).

NOTES

1. Package dimensions conform to JEDEC Specification MO-047-AE for Plastic Leaded Chip Carrier 68 leads, 0.050 inch lead spacing, square, (Issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H-" located at the top of mold parting line and coincident with top of lead, where leads exits plastic body.
5. Location to datum "A-" and "B-" to be determined at plane "H-". These datums do not include mold flash. Mold flash protrusion shall not exceed 0.010" (0.25mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H-".
7. Pin numbers continue counterclockwise to Pin 68 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.
10. Location of Pin #1 mark is optional. Mark on chamfered side is preferred.

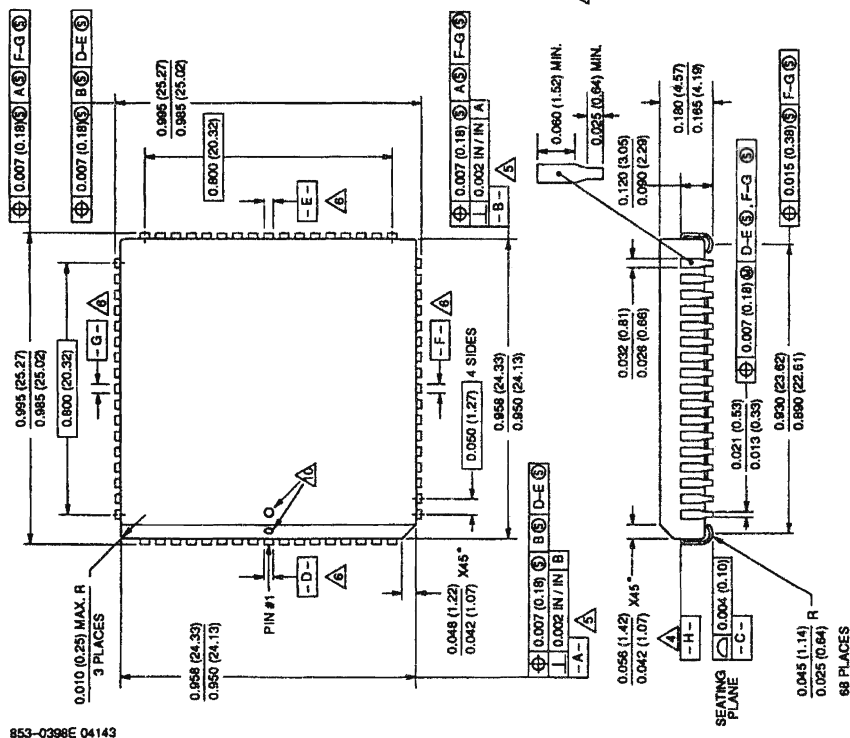


Fig.21 68-pin square plastic leaded chip carrier (A) package (DWG 0398E).

Package outlines

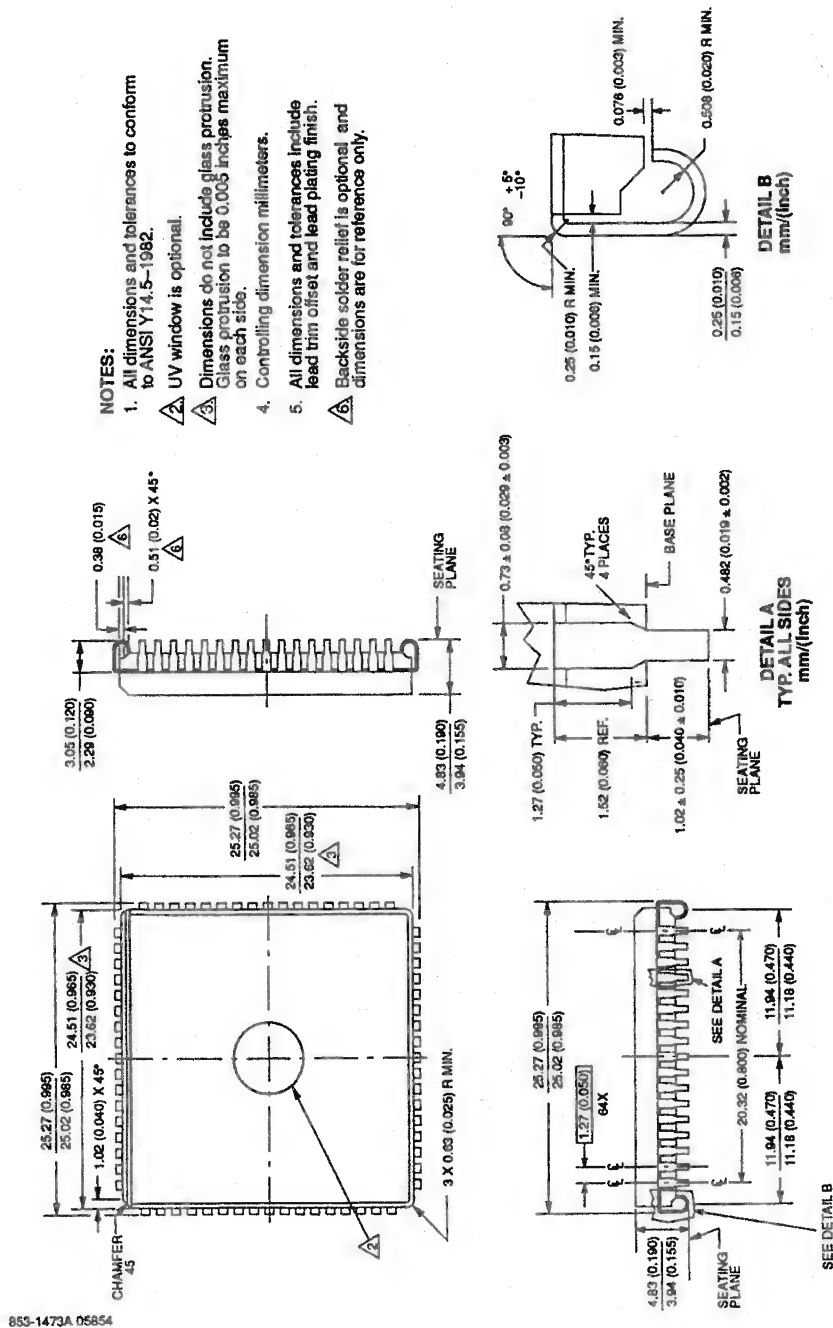
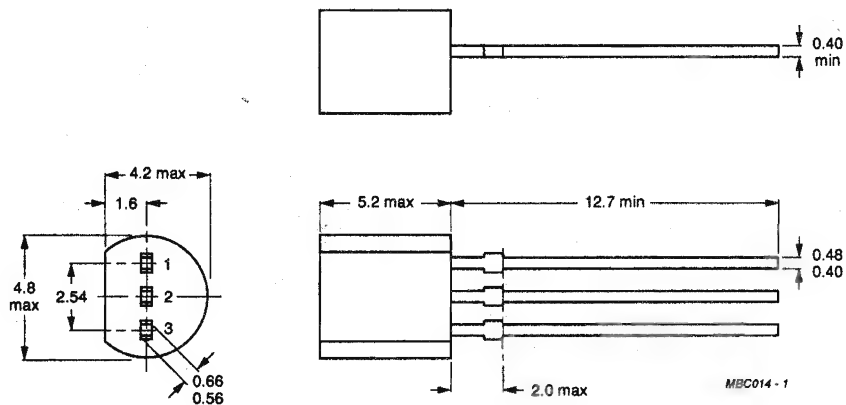


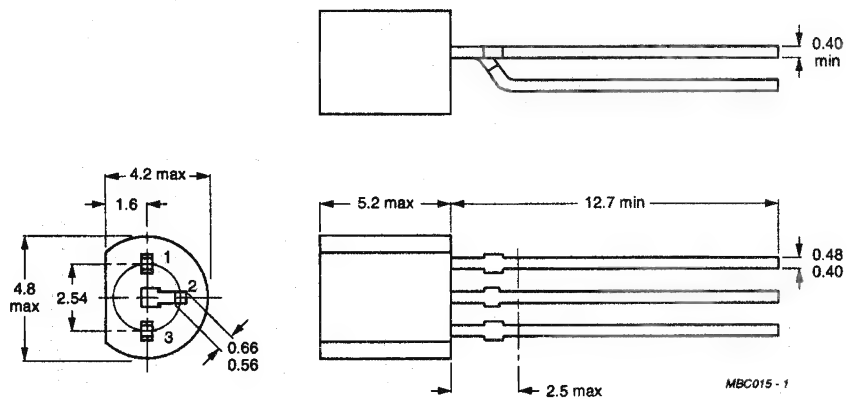
Fig.22 68-lead CERQUAD J-bend (K) package (DWG 1473A).

Package outlines



Dimensions in mm.

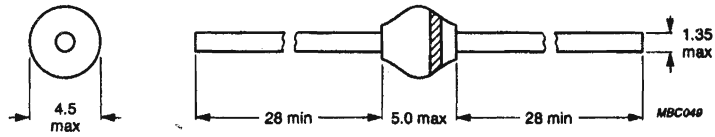
Fig.23 TO-92 VARIANT (VN2406L series).



Dimensions in mm.

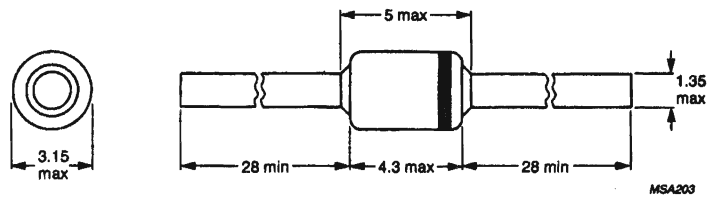
Fig.24 TO-92 VARIANT (BS107 BS108 BS170 BSN254/A BSP254/A BSS89 BSS92 BST74A BST76A series).

Package outlines



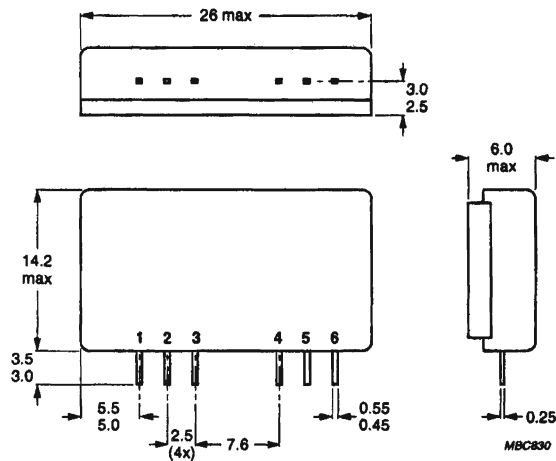
Dimensions in mm.

Fig.25 BZW03 and BZW14 series (SOD64).



Dimensions in mm.

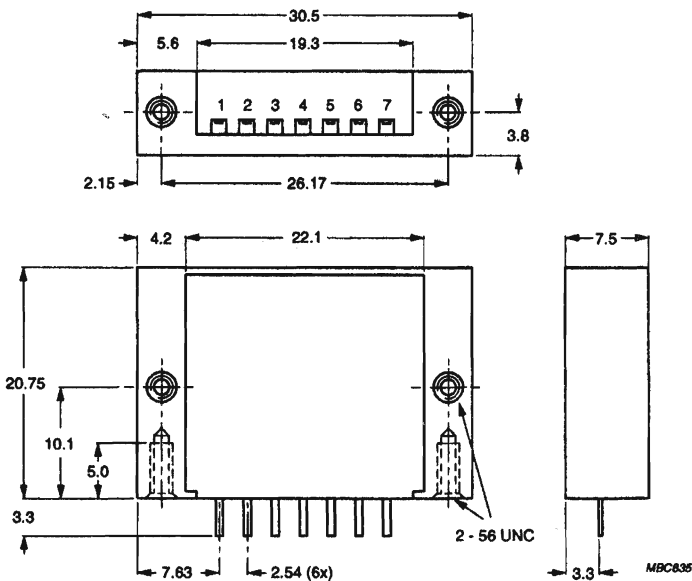
Fig.26 BR211 series (SOD84).



Dimensions in mm.

Fig.27 BGY46A BGY46B BGY47A series (SOT181).

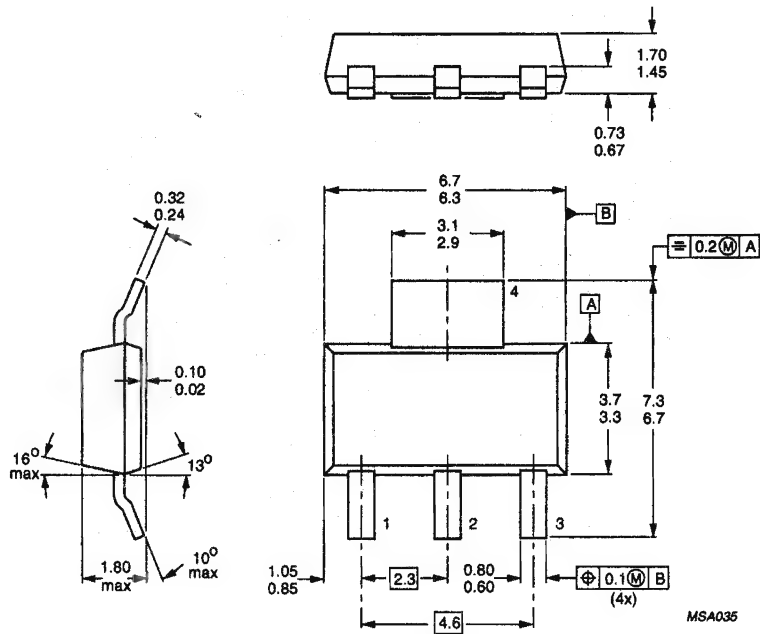
Package outlines



Dimensions in mm.

Fig.28 BGY95A/B BGY96A/B series (SOT200).

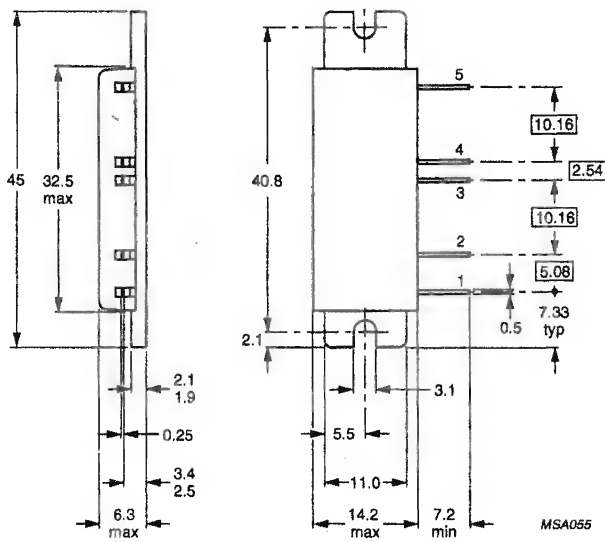
Package outlines



Dimensions in mm.

Fig.29 BSP126 BSP225 BSP89 BSP92 series (SOT223).

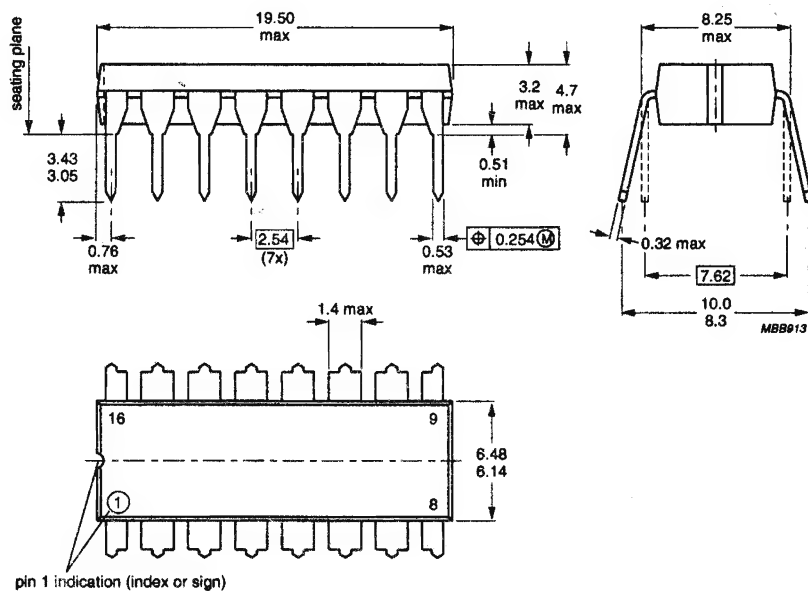
Package outlines



Dimensions in mm.

Fig.30 BGY110D/E/F/G series (SOT246).

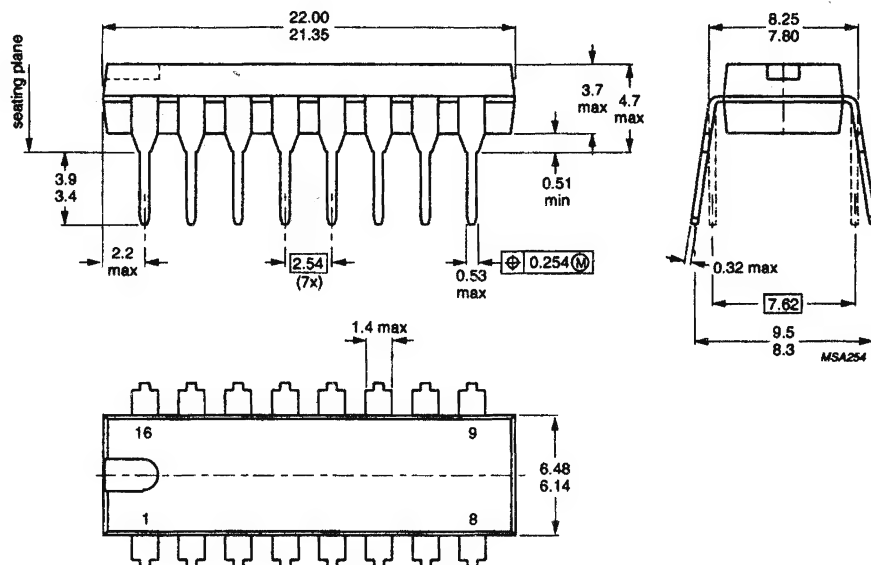
Package outlines



Dimensions in mm.

Fig.31 16-lead dual in-line; plastic (SOT38Z).

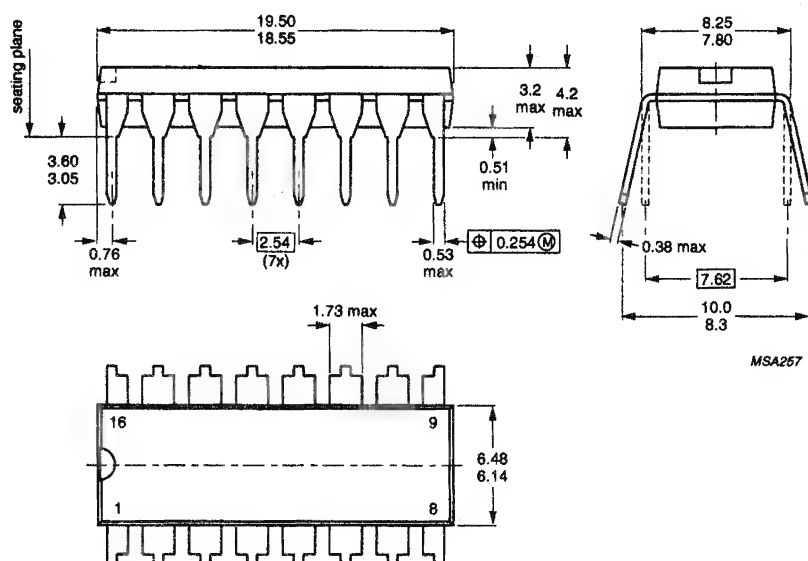
Package outlines



Dimensions in mm.

Fig.32 16-lead dual in-line; plastic (SOT38 GE GG).

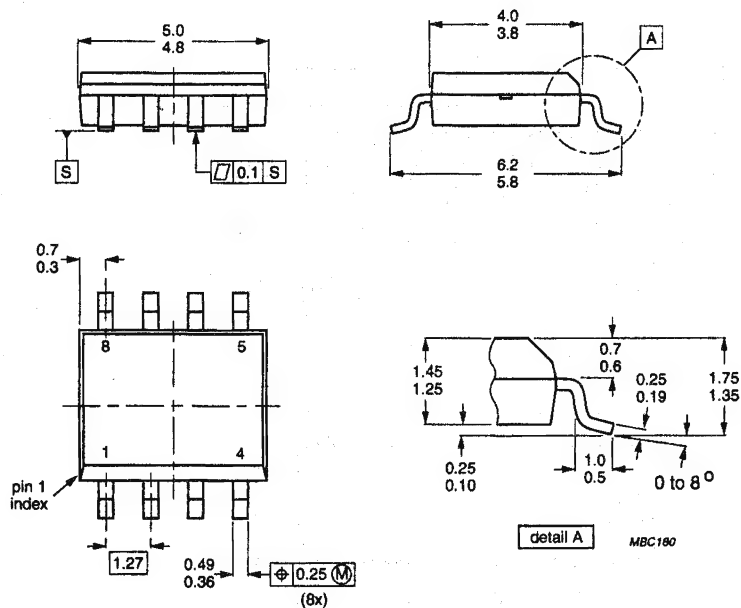
Package outlines



Dimensions in mm.

Fig.33 16-lead dual in-line; plastic (SOT38 DF).

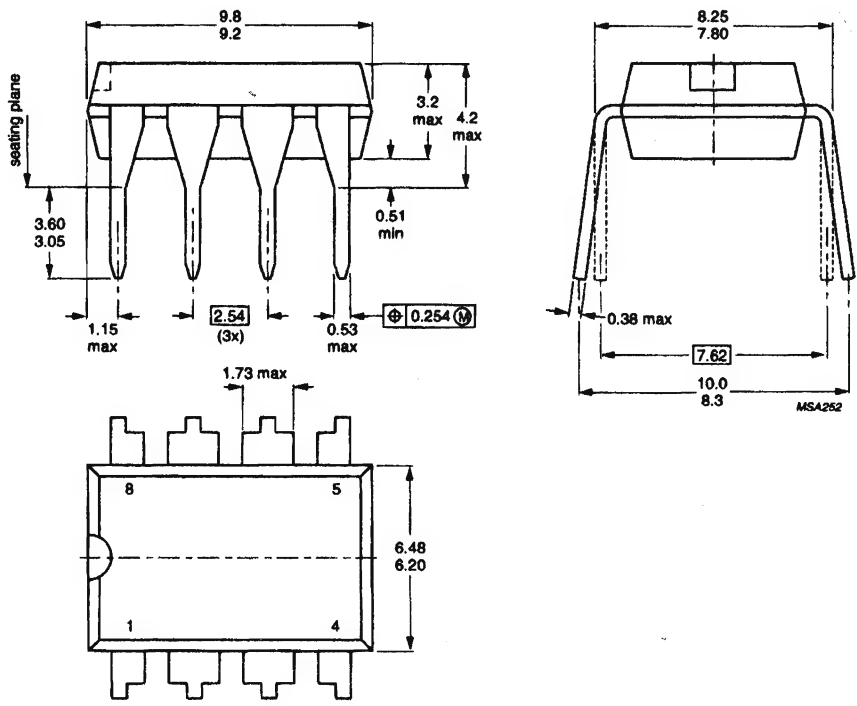
Package outlines



Dimensions in mm.

Fig.34 8-lead mini-pack; plastic (SO8; SOT96A).

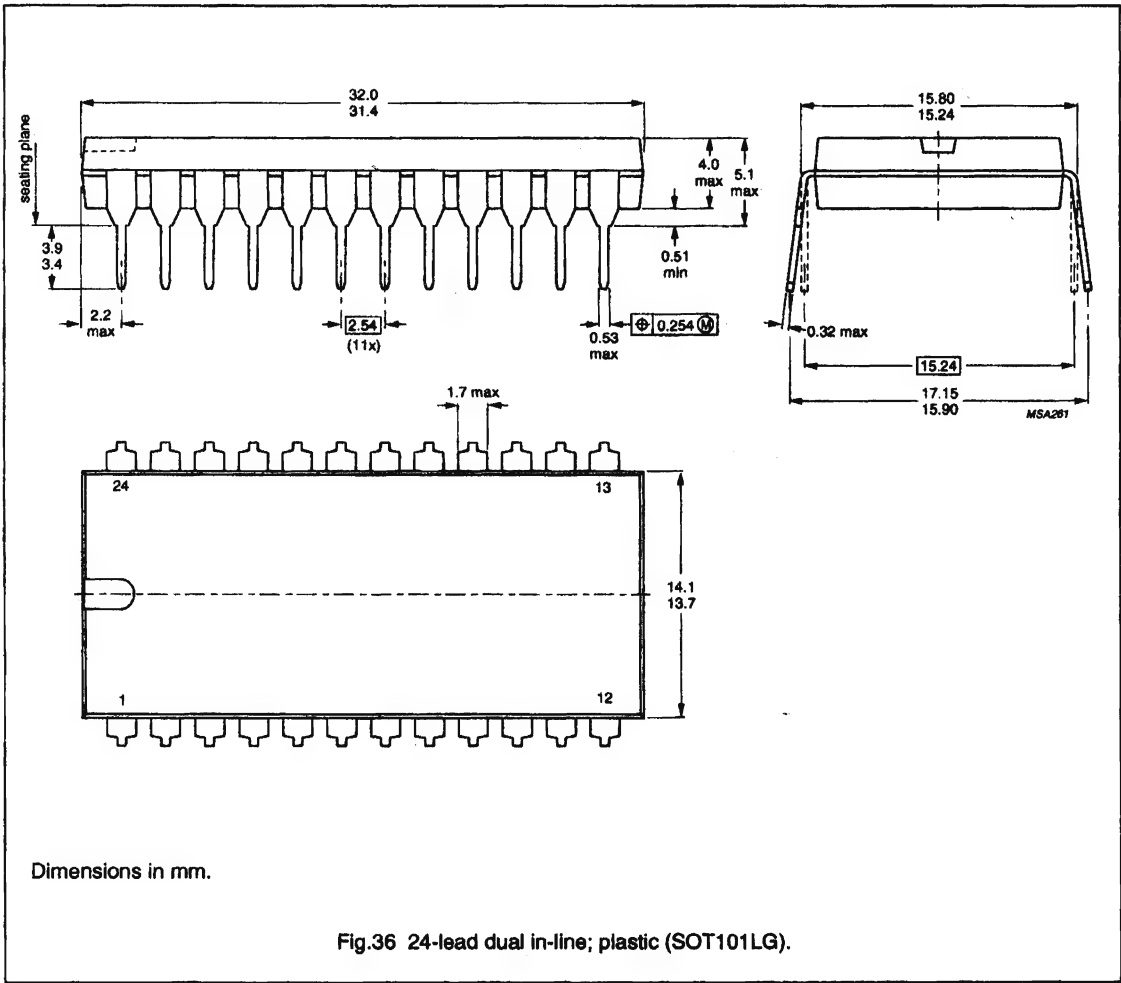
Package outlines



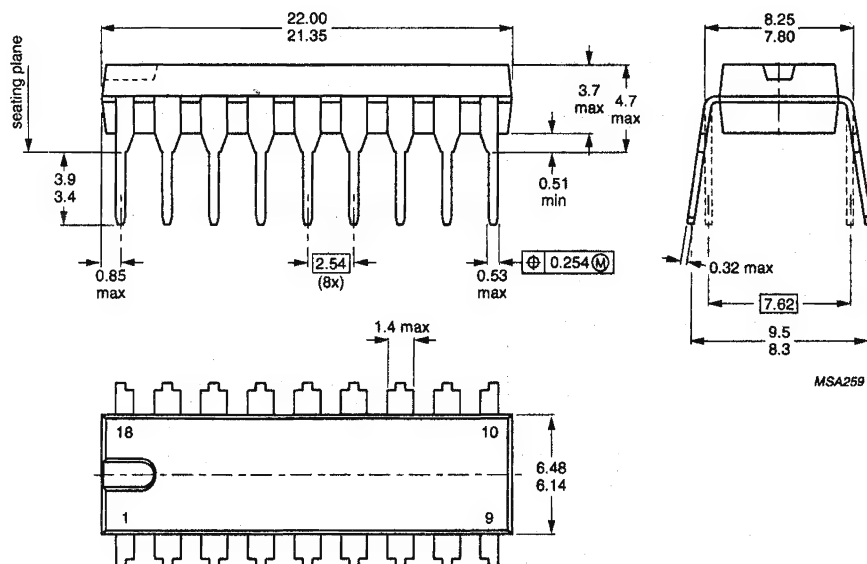
Dimensions in mm.

Fig.35 8-lead dual in-line; plastic (SOT97).

Package outlines



Package outlines



Dimensions in mm.

Fig.37 18-lead dual in-line; plastic (SOT102G).

Package outlines

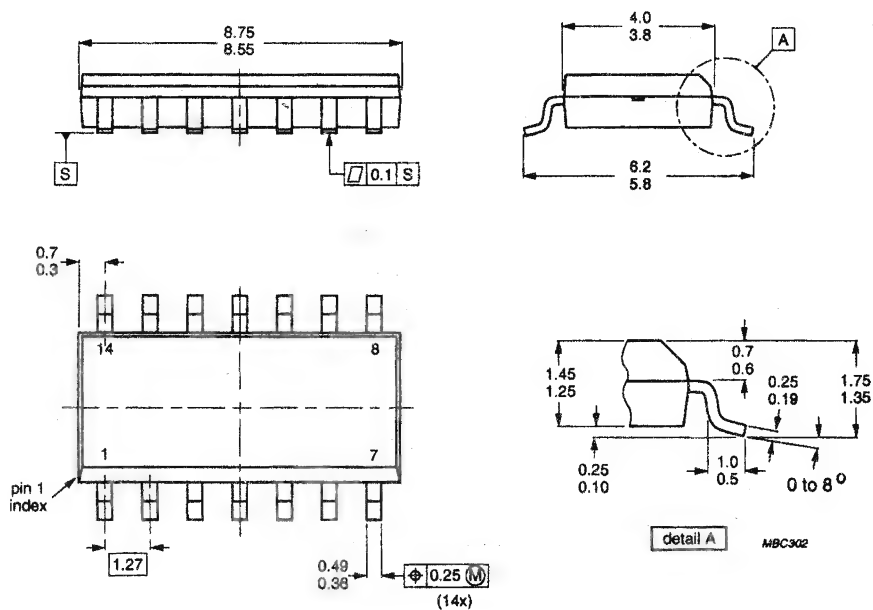
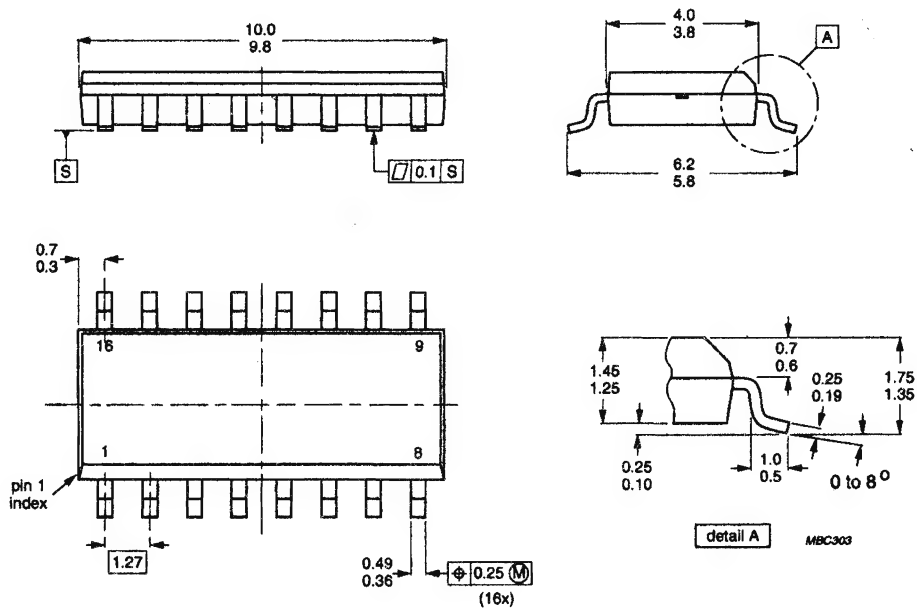


Fig.38 14-lead mini-pack; plastic (SO14; SOT108A).

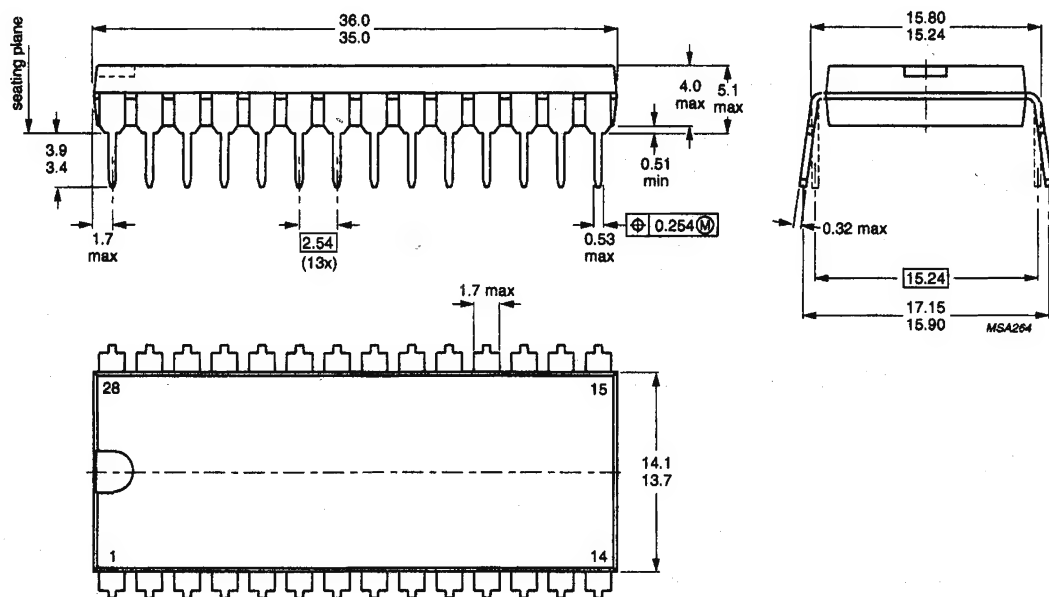
Package outlines



Dimensions in mm.

Fig.39 16-lead mini-pack; plastic (SO16; SOT109A).

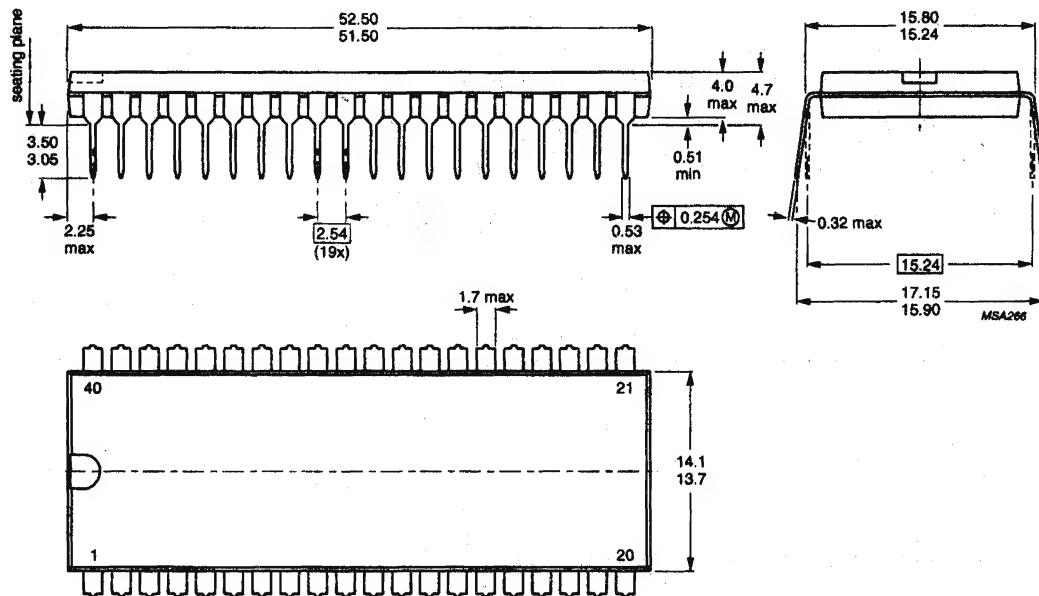
Package outlines



Dimensions in mm.

Fig.41 28-lead dual in-line; plastic (SOT117N).

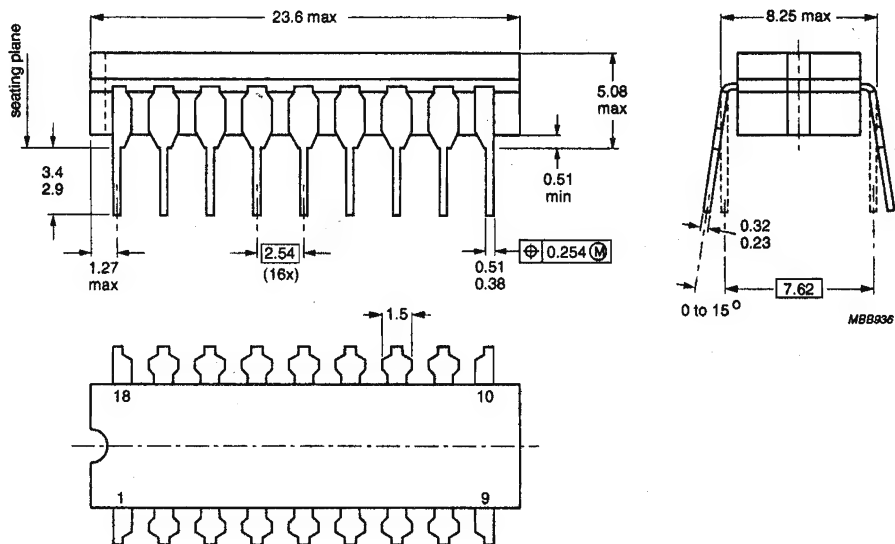
Package outlines



Dimensions in mm.

Fig.42 40-lead dual in-line; plastic (SOT129).

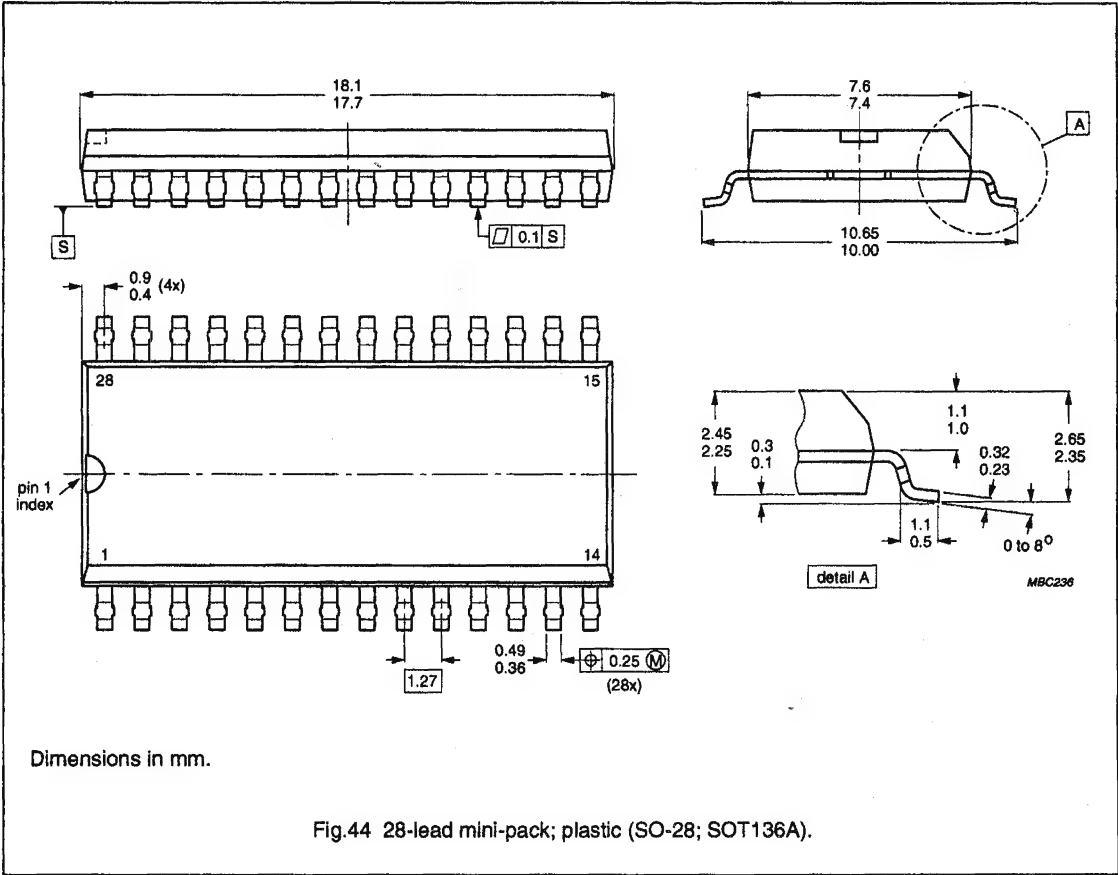
Package outlines



Dimensions in mm.

Fig.43 18-lead dual in-line; ceramic (cerdip) (SOT133B).

Package outlines



Package outlines

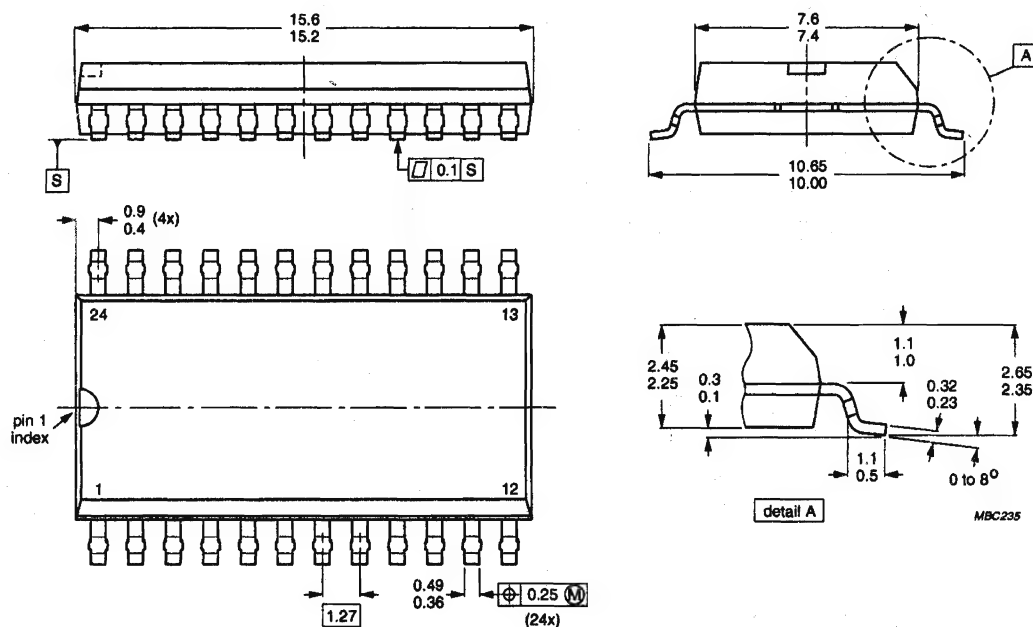


Fig.45 24-lead mini-pack; plastic (SO-24; SOT137A).

Package outlines

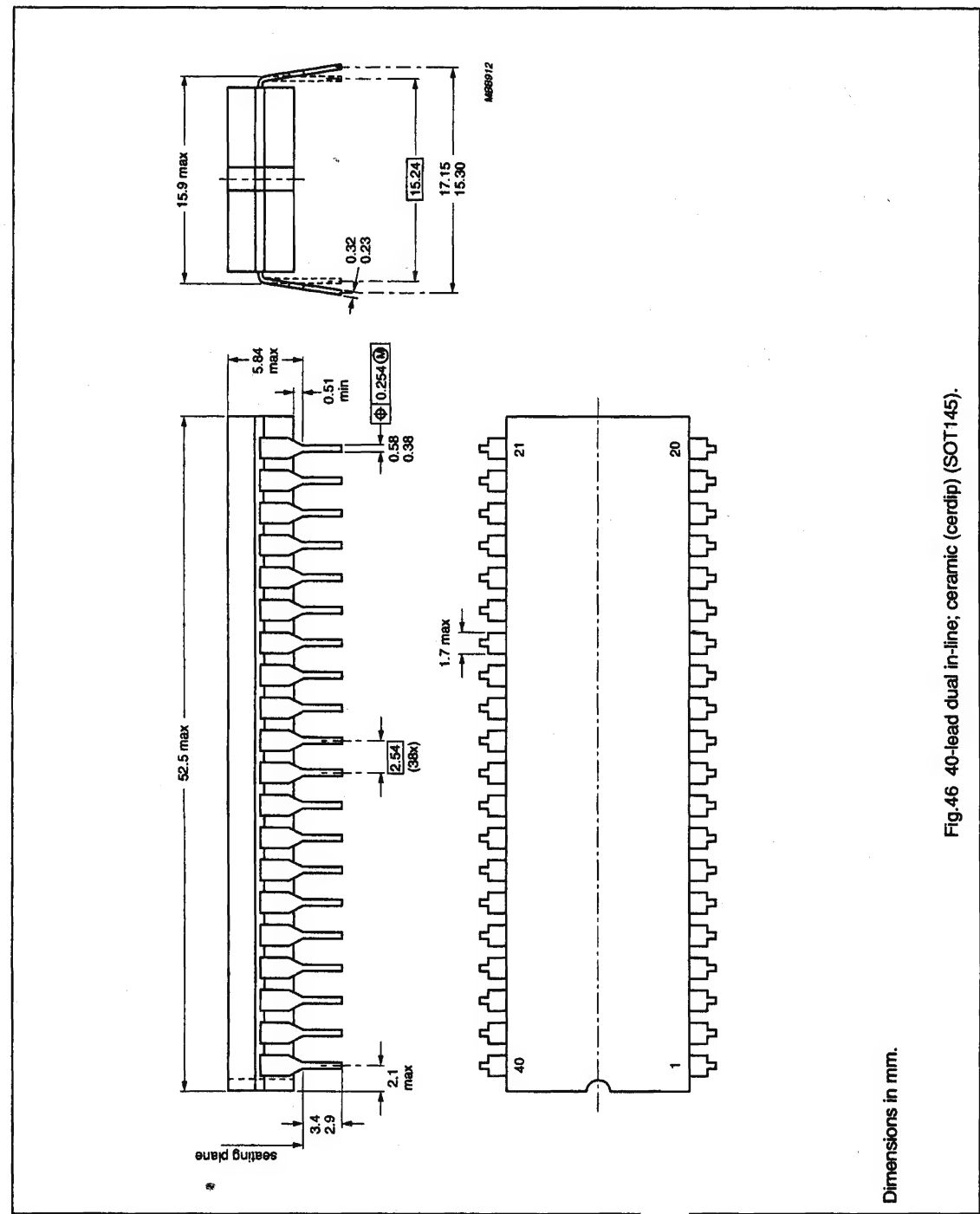
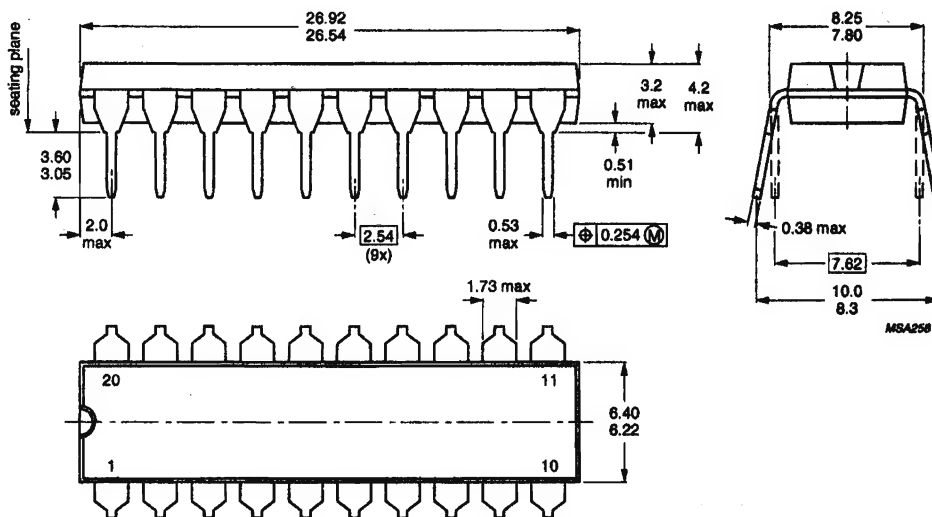


Fig.46 40-lead dual in-line; ceramic (cerdip) (SOT145).

Package outlines



Dimensions in mm.

Fig.47 20-lead dual in-line; plastic (SOT146).

Package outlines

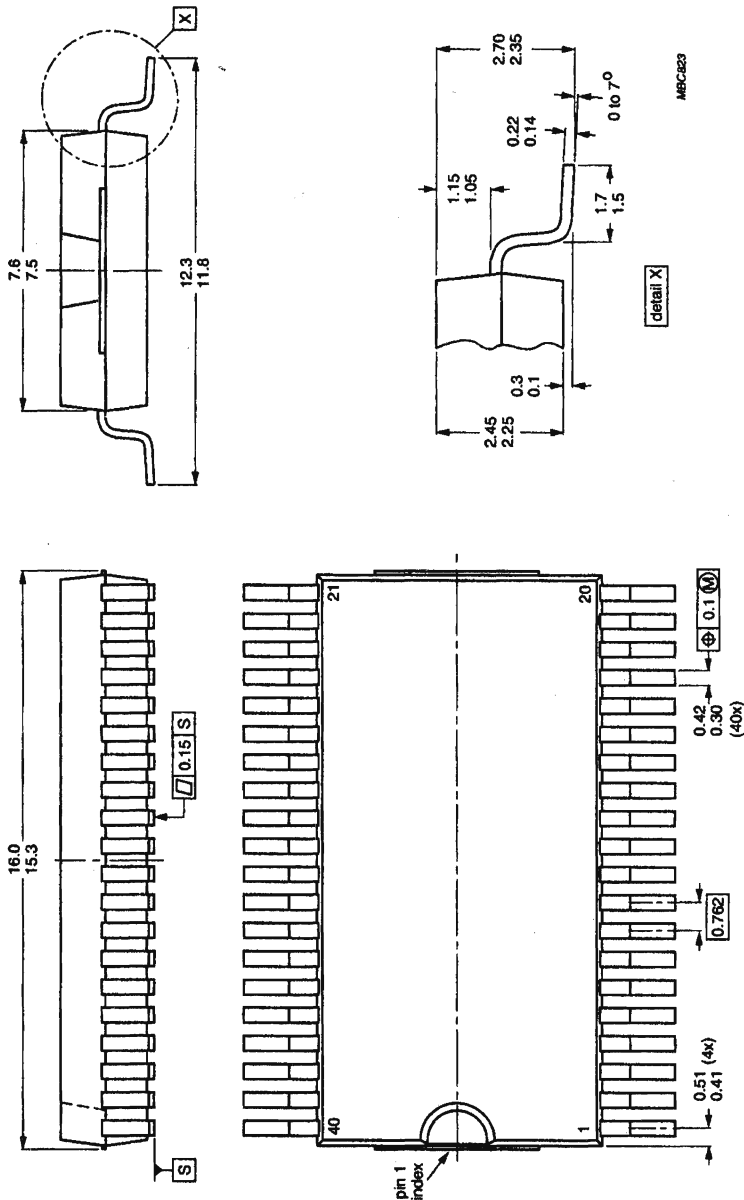
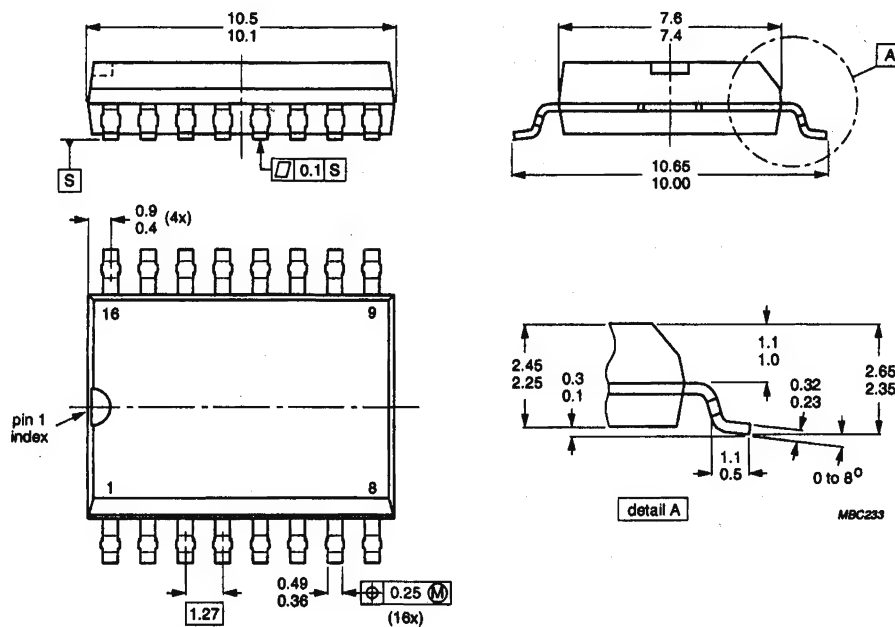


Fig.48 40-lead mini-pack; plastic (VSO40; SOT158A).

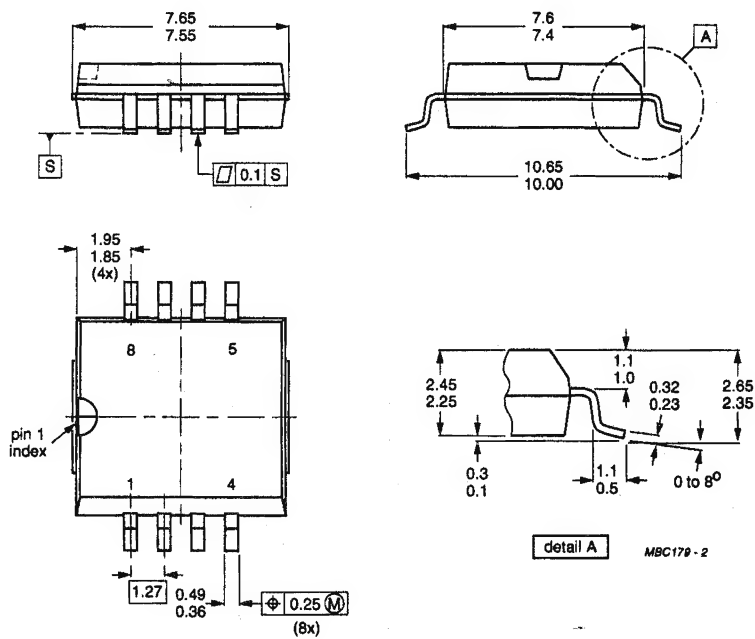
Package outlines



Dimensions in mm.

Fig.49 16-lead mini-pack; (SO16L; SOT162A).

Package outlines



Dimensions in mm.

Fig.51 8-lead mini-pack; plastic (SO8L; SOT176C).

Technical drawing of a metal spring clip, showing three views: top, side, and detail A.

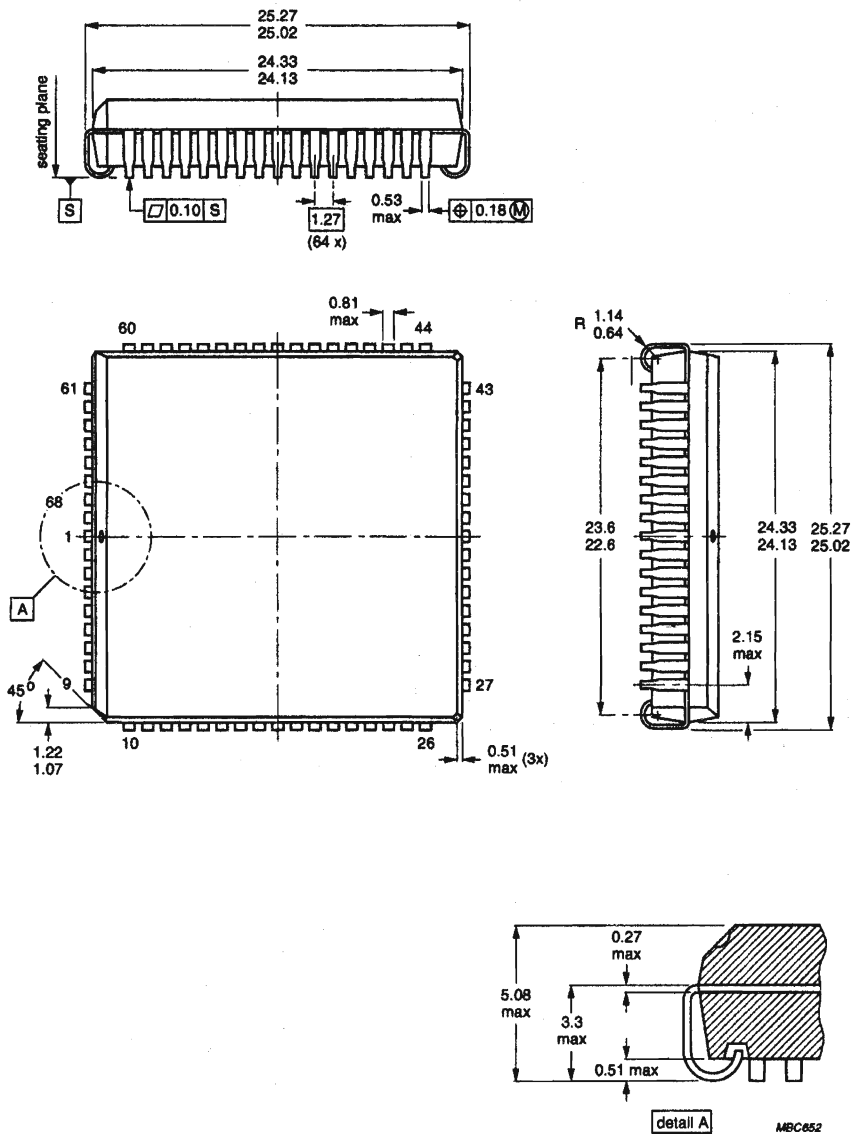
Top View: The clip is rectangular with a central slot. Dimensions include overall width of 17.85 and 17.40, and inner width of 16.66 and 16.51. A central slot width is 1.27 (40 x). A seating plane is indicated on the left. Surface finish symbols are present: S, 0.10 S, 0.53 max, and 0.18 (M).

Side View: Shows the profile of the clip. Dimensions include overall height of 16.00 and 14.99, and inner height of 16.66 and 16.51. A central slot width is 1.27 (40 x). A seating plane is indicated on the left. Surface finish symbols are present: S, 0.10 S, 0.53 max, and 0.18 (M).

Detail A: A close-up of the clip's end, showing a hook and a spring. Dimensions include overall height of 4.57 max, inner height of 3.04 max, and a minimum gap of 0.51 min. A surface finish symbol of 0.32 max is shown.

Fig.52 44-lead plastic leaded chip carrier (PLCC) (SOT187CG).

Package outlines



Dimensions in mm.

Fig.53 68-lead plastic leaded chip carrier (PLCC) (SOT188CG).

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Package outlines

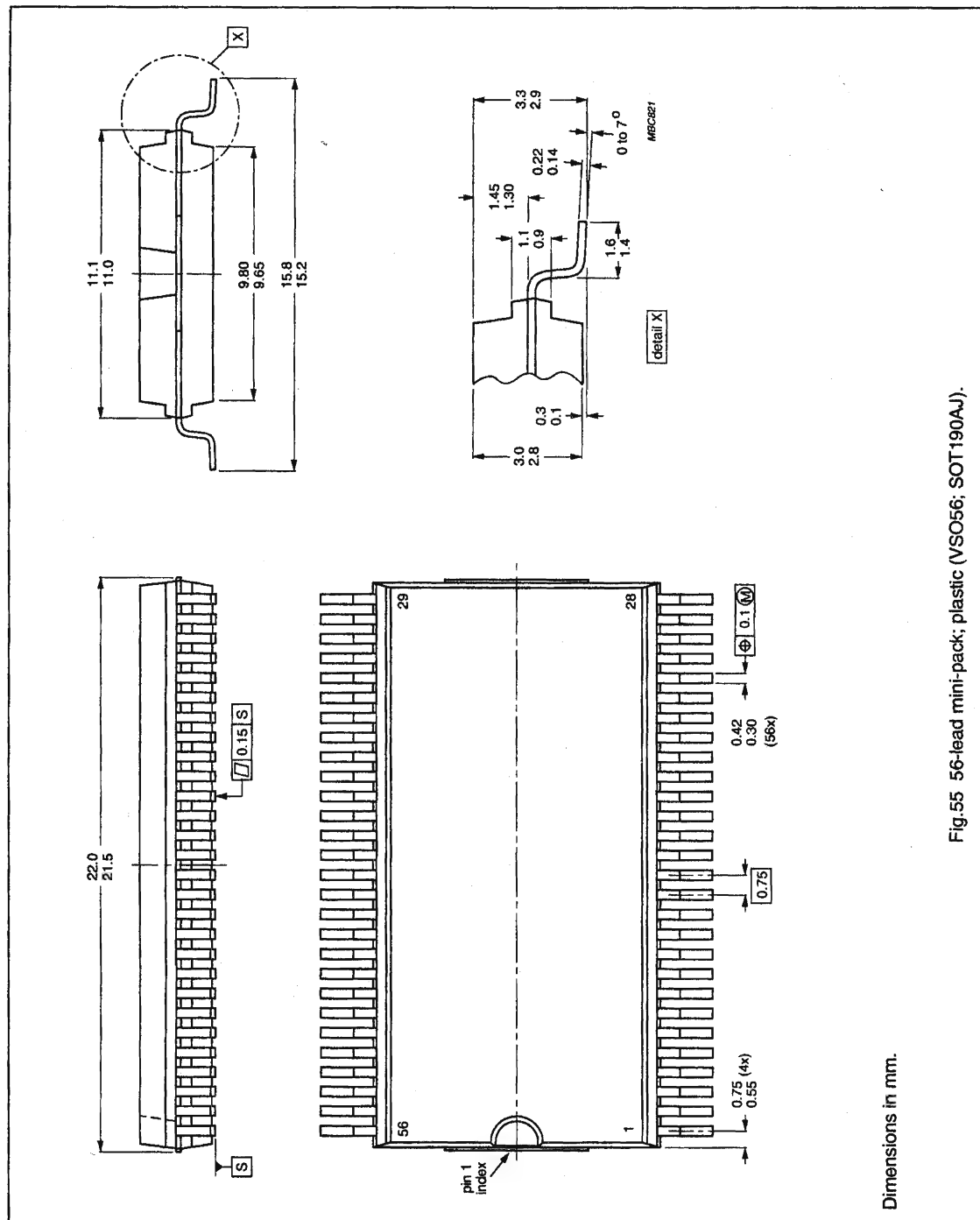
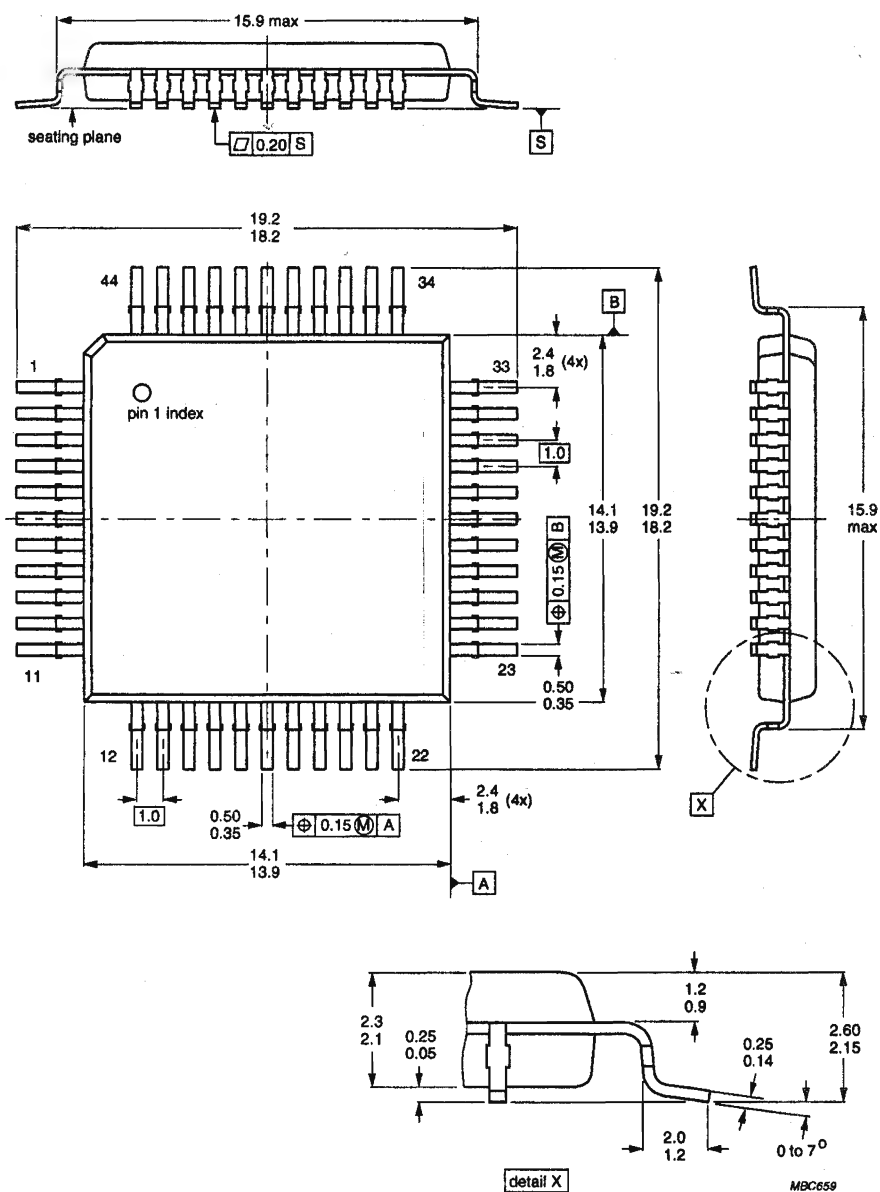


Fig.55 56-lead mini-pack; plastic (VSO56; SOT190A).

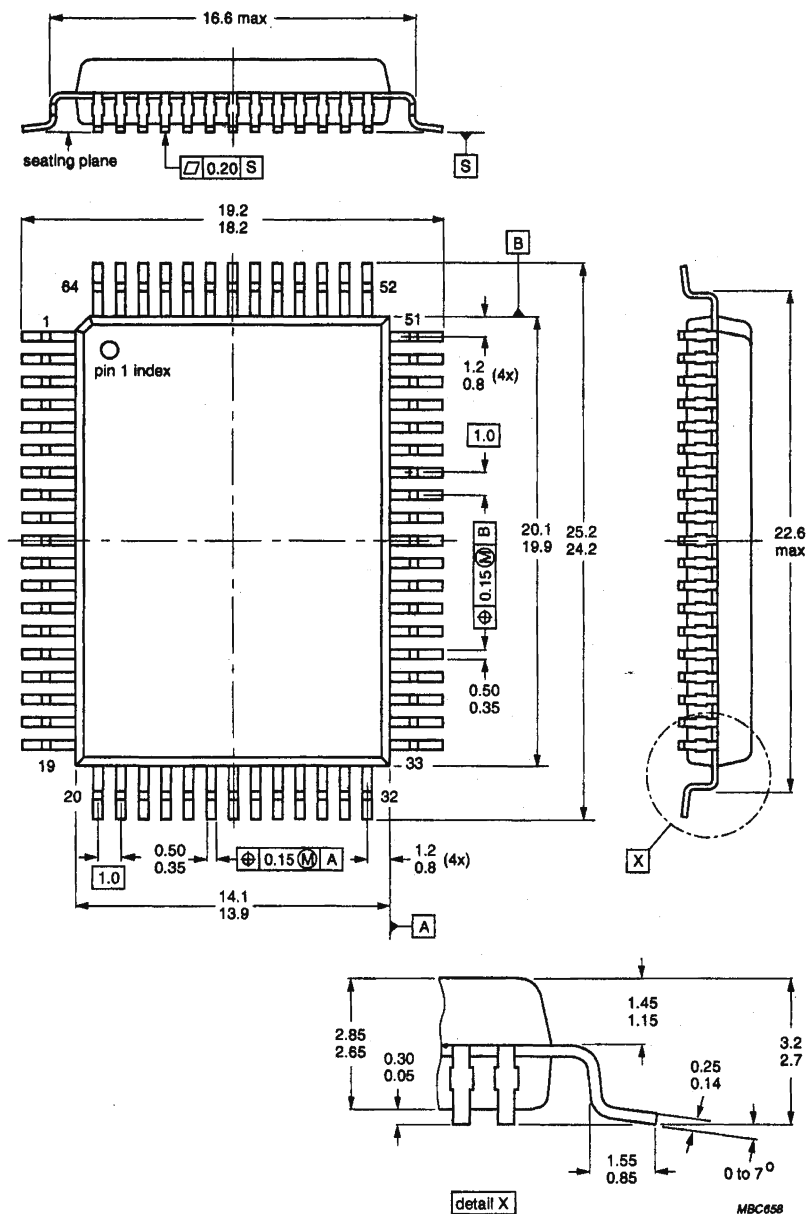
Package outlines



Dimensions in mm.

Fig.56 44-lead quad flat-pack 14 mm square; plastic (SOT205AG).

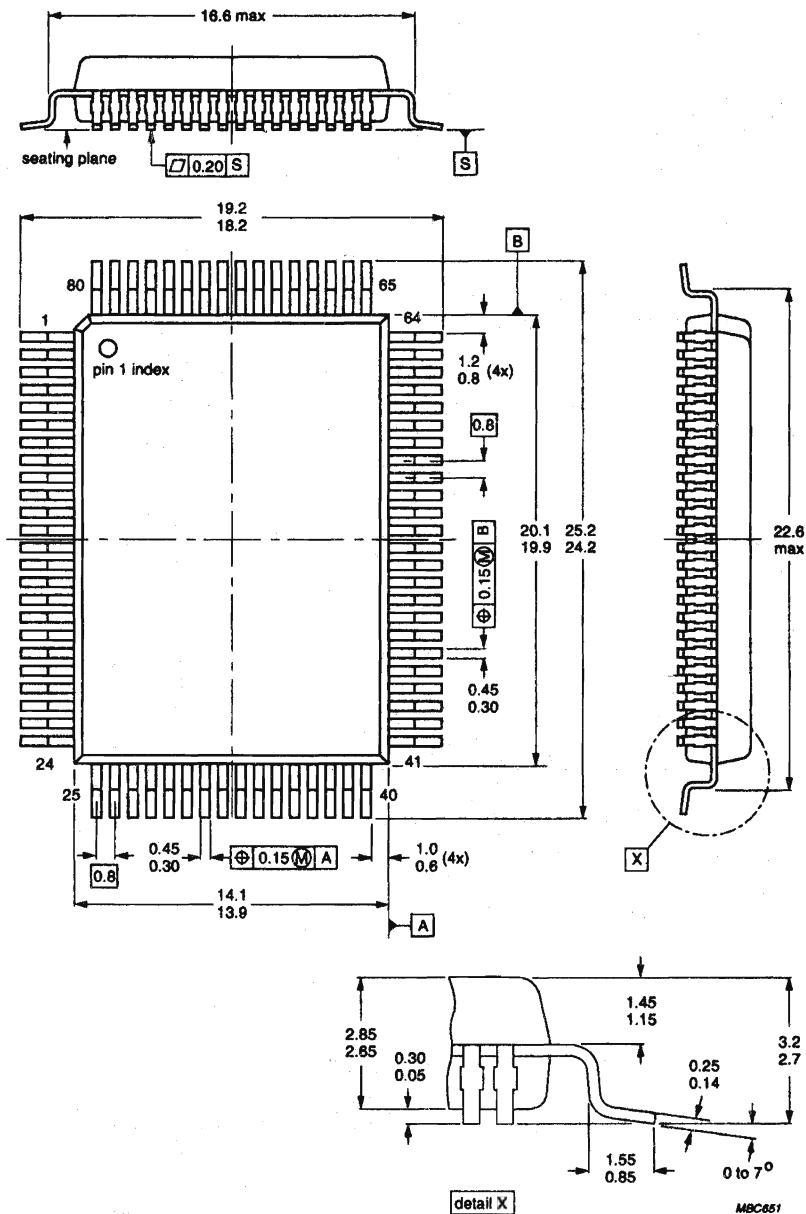
Package outlines



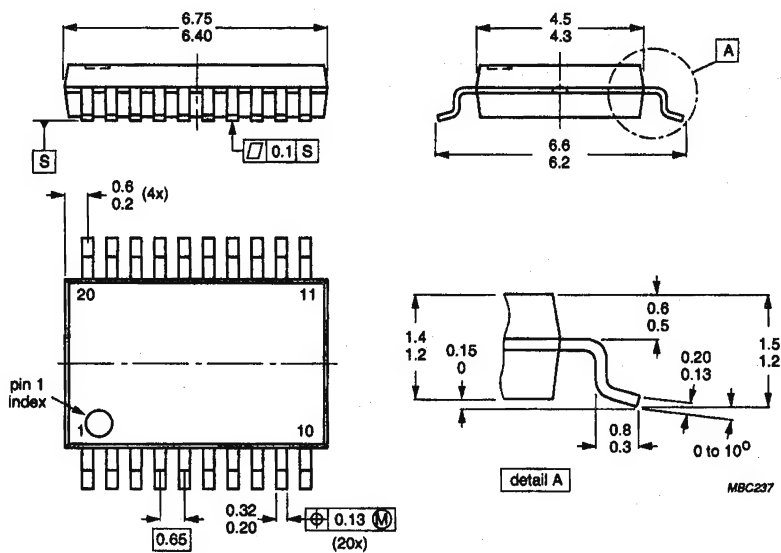
Dimensions in mm.

Fig.57 64-lead quad flat-pack rectangular; plastic (SOT208A).

Package outlines



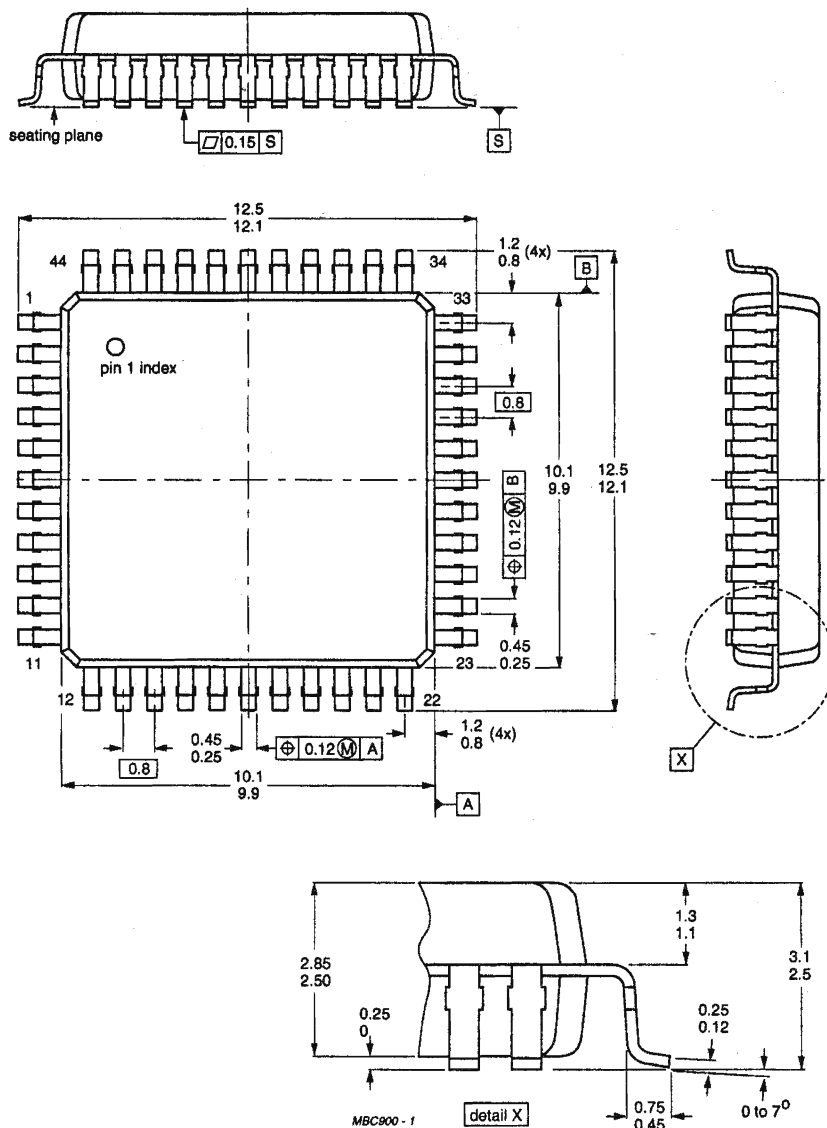
Package outlines



Dimensions in mm.

Fig.59 20-lead shrink dual in-line; plastic (SSOP20; SOT266A).

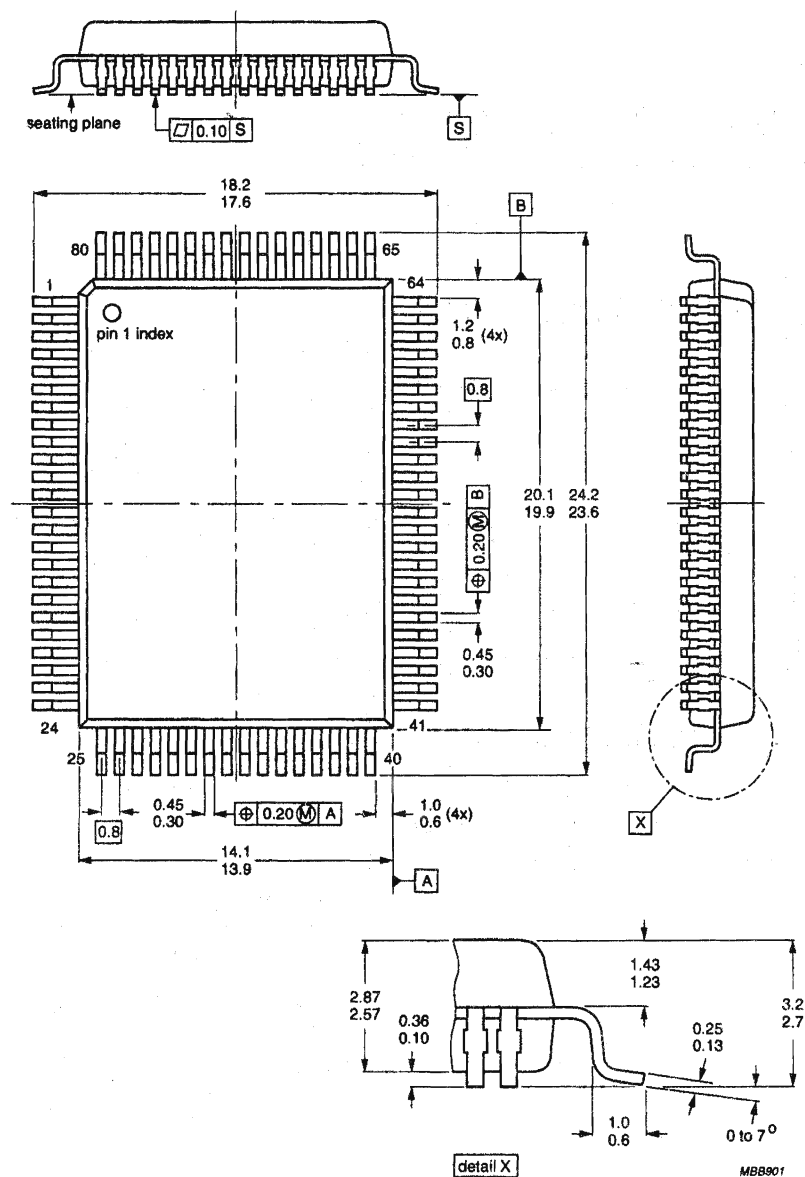
Package outlines



Dimensions in mm.

Fig.60 44-lead quad flat-pack 10 mm square; plastic (QFP44S10; SOT311A).

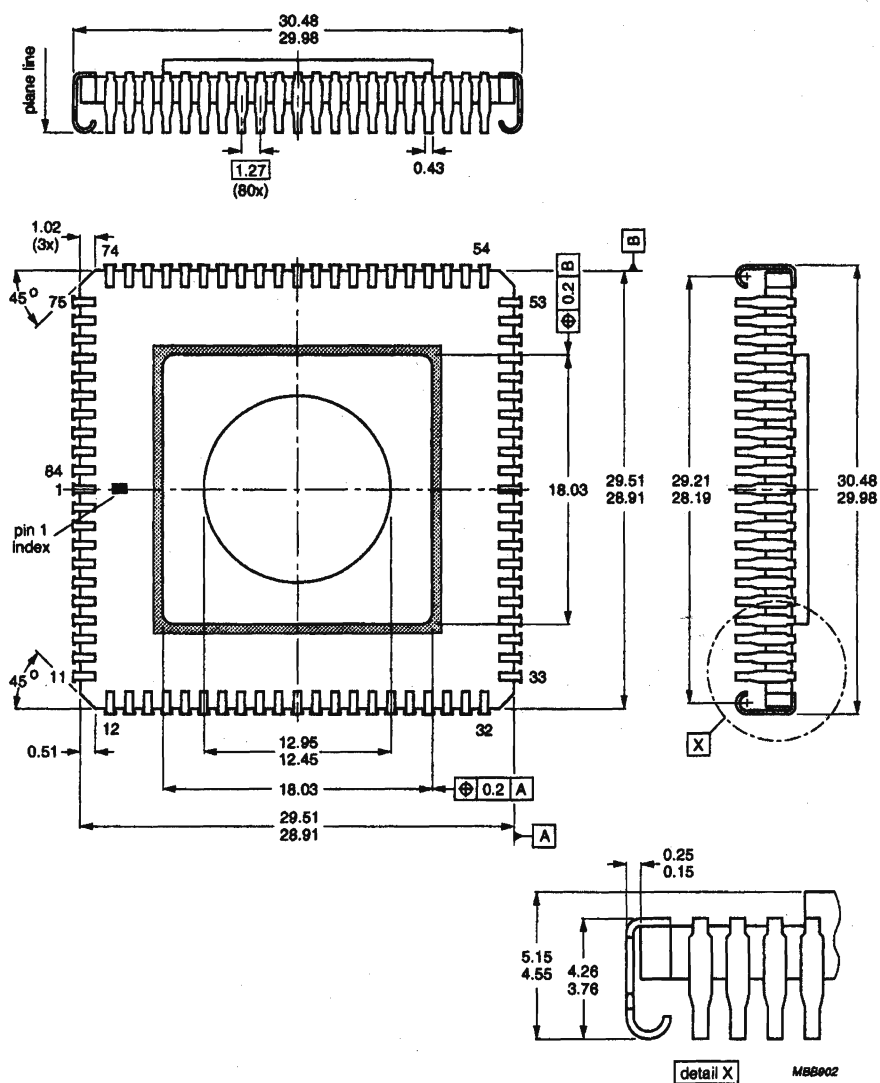
Package outlines



Dimensions in mm.

Fig.61 80-lead quad flat-pack; plastic (QFP80; SOT318).

Package outlines



Dimensions in mm.

Fig.62 80-lead ceramic quad K-pack (N0331B).

CHAPTER 10

SOLDERING INFORMATION

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Soldering information

SOLDERING

Plastic mini-packs, PLCC and QFP

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if

between 300 and 400 °C, for not more than 5 s.

SOLDERING

Tab modules

FLUXING

Use a flux that does not have to be removed, or a water-soluble flux.

SOLDERING

The reflow soldering method using pulse-heated tool is usually suitable. Limit the soldering operation to 3 s at 250 °C at the leads.

CLEANING

Avoid cleaning if possible. If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do not use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do not use solvents.

CHAPTER 11

DATA HANDBOOK SYSTEM

page

Data handbook system

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Data handbook system

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publications and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogues are available for selected product ranges (some catalogues are also on floppy discs).

Our data handbook titles are listed here.

Integrated circuits

Book Title

IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC06	High-speed CMOS Logic Family
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontrollers Peripherals (planned)
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications (planned)
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fibre Optics
IC20	851-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers (planned)
IC22	ICs for Multi-media Systems
IC23	QUBIC Advanced BiCMOS Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS Logic

Discrete semiconductors

Book Title

SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Transistors
SC13	PowerMOS Transistors
SC14	RF Wideband Transistors, Video Transistors and Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Professional components

PC01	High-power Klystrons and Accessories
PC06	Circulators and Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?

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Data handbook system

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOK

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display components

Book	Title
DC01	Colour Display components Colour TV Picture tubes and Assemblies Colour Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

Liquid Crystal displays

LCD01	Liquid Crystal Displays and Driver ICs for LCDs
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Magnetic products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites

Passive components

PA01	Electrolytic Capacitors
PA02	Varsities, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Application
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

Professional components

PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC09	Dry-reed Switches
PC12	Electron Multipliers

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